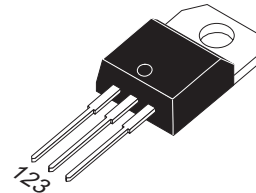


## Simplified outline TO-220AB

### Description

Standard gate triggering SCR is fully isolated package suitable for the application where requiring high bidirectional blocking voltage capability and also suitable for over voltage protection, motor control circuit in power tool, inrush current limit circuit and heating control system.



### Features

- Blocking voltage to 800 V
- On-state RMS current to 20 A
- Ultra low gate trigger current

### Symbol



### Applications

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

Pin	Description
1	cathode
2	anode
3	gate
TAB	anode

SYMBOL	PARAMETER	Value	Unit
$V_{DRM}$	Repetitive peak off-state voltages	400RG 600RG 800RG	V
$V_{RRM}$	Voltages		
$I_{TR (MS)}$	RMS on-state current	20	A
$I_{TSM}$	Non-repetitive peak on-state current	200	A

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{th j-mb}$	Thermal resistance Junction to mounting base		-	-	1.1	K/W
$R_{th j-a}$	Thermal resistance Junction to ambient	In free air	-	60	-	K/W

**Limiting values in accordance with the Maximum system(IEC 134)**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{DRM}$ $V_{RRM}$	Repetitive peak off-state Voltages	500RG 650RG 800RG	-	500 650 800	V
$I_{TAV}$	Average on-state current	Half sine wave; $T_{mb} \leq 103$ °C	-	13	A
$I_{T(RMS)}$	RMS on-state current	All conduction angles	-	20	A
$I_{TSM}$	Non-repetitive peak On-state current	half sine wave; $T_j = 25$ °C prior to surge	-	200	A
			-	220	A
$I^2t$	$I^2t$ for fusing	$T = 10ms$	-	200	A <sup>2</sup> S
$DI_T/dt$	Repetitive rate of rise of on-state current after trigering	$I_{TM} = 50A$ ; $I_G = 0.2A$ ; $DI_G/dt = 0.2A/\mu s$	-	200	A/ $\mu s$
$I_{GM}$	Peak gate current		-	5	A
$V_{GM}$	Peak gate voltage		-	5	V
$P_{GM}$	Peak gate power		-	20	W
$P_{G(AV)}$	Average gate power	Over any 20 ms period	-	0.5	W
$T_{stg}$	Storage temperature		-40	150	°C
$T_j$	Operating junction Temperature		-	125	°C

 **$T_j = 25$  °C unless otherwise stated**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
$I_{GT}$	Gate trigger current	$V_{DG} = 12V$ ; $I_T = 0.1A$	-	3	32	mA
$I_L$	Latching current	$V_{DG} = 12V$ ; $I_T = 0.1A$	-	25	80	mA
$I_H$	Holding current	$V_{DG} = 12V$ ; $I_T = 0.1A$	-	15	60	mA
$V_T$	On-state voltage	$I_T = 40A$	-	1.4	1.75	v
$V_{GT}$	Gate trigger voltage	$V_{DG} = 12V$ ; $I_T = 0.1A$	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$ ; $I_T = 0.1A$ ; $T_j = 125$ °C	0.25	0.4	-	V
$I_D$	Off-state leakage current	$V_D = V_{DRM(max)}$ ; $V_R = V_{RRM(max)}$ ; $T_j = 125$ °C	-	0.2	1.0	mA

**Dynamic Characteristics**

$D/V_D dt$	Critical rate of rise of Off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 125$ °C; exponential wave form; gate open circuit	200	300	-	V/ $\mu s$
$t_{gt}$	Gate controlled turn-on time	$I_{TM} = 40A$ ; $V_D = V_{DRM(max)}$ ; $I_G = 0.1A$ ; $DI_G/dt = 5A/\mu s$	-	2	-	$\mu s$
$t_g$	Crcuit commutated tum- off time	$V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 125$ °C; $I_{TM} = 50A$ $V_R = 25V$ ; $dI_M/dt = 30A/\mu s$ $DI_G/dt = 50V/\mu s$ ; $R_{GK} = 100 \Omega$	-	70	-	$\mu s$

## Description

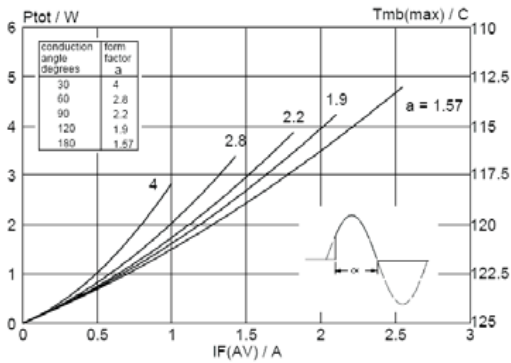


Fig. 1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$ .

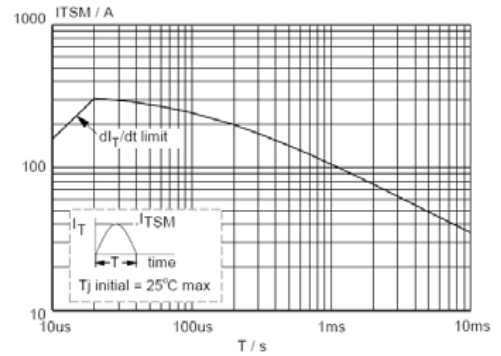


Fig. 2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10\text{ms}$ .

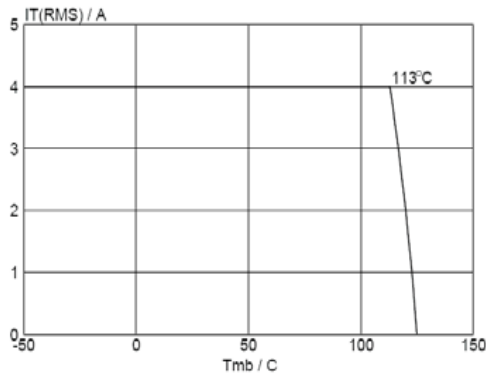


Fig. 3. Maximum permissible rms current  $I_{T(RMS)}$ , versus mounting base temperature  $T_{mb}$ .

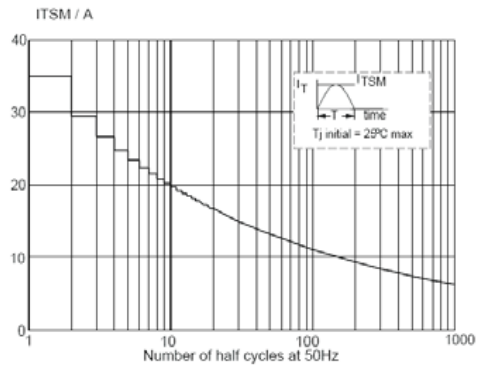


Fig. 4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50\text{ Hz}$ .

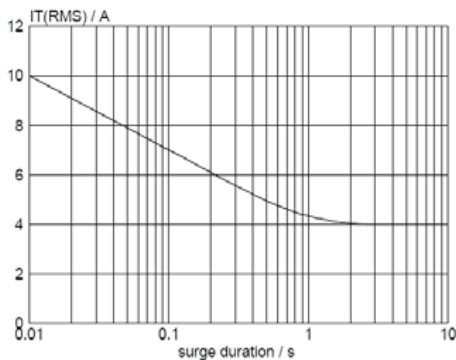


Fig. 5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50\text{ Hz}$ ;  $T_{mb} \leq 113^\circ\text{C}$ .

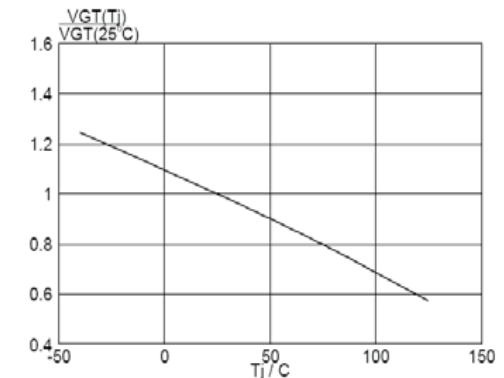


Fig. 6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

## Description

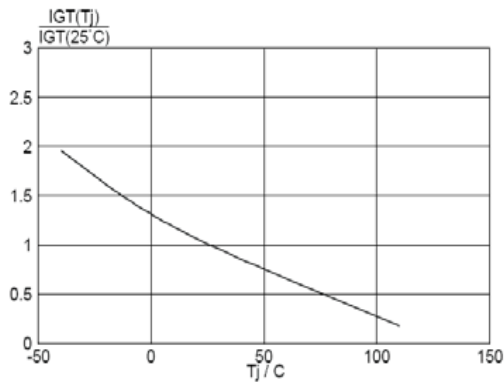


Fig. 7. Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

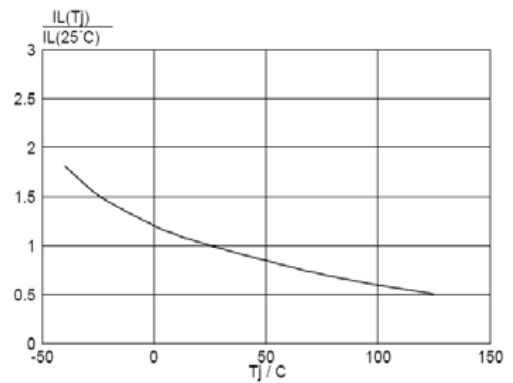


Fig. 8. Normalised latching current  $I_L(T_j)/I_L(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

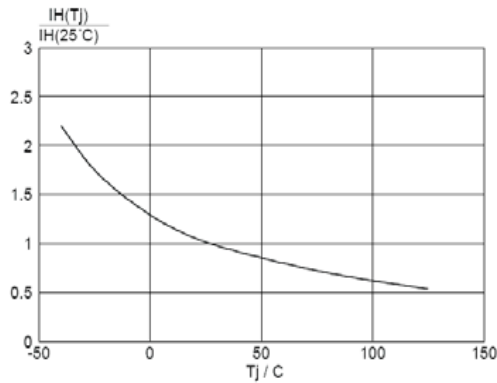


Fig. 9. Normalised holding current  $I_H(T_j)/I_H(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

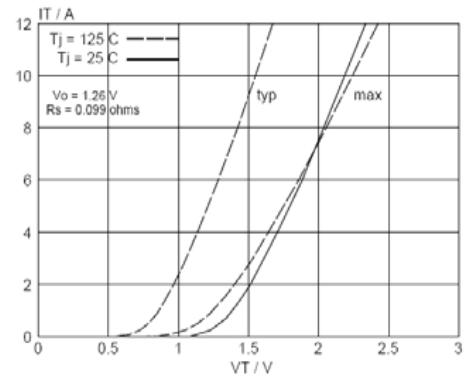


Fig. 10. Typical and maximum on-state characteristic.

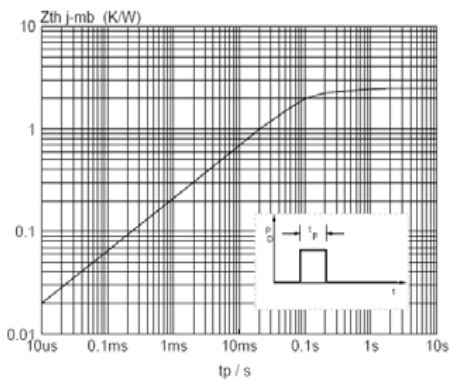


Fig. 11. Transient thermal impedance  $Z_{th\ j-mb}$ , versus pulse width  $t_p$ .

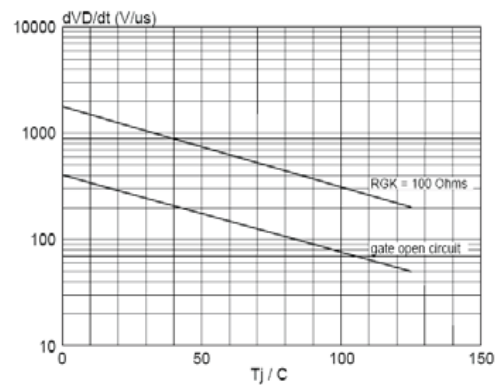
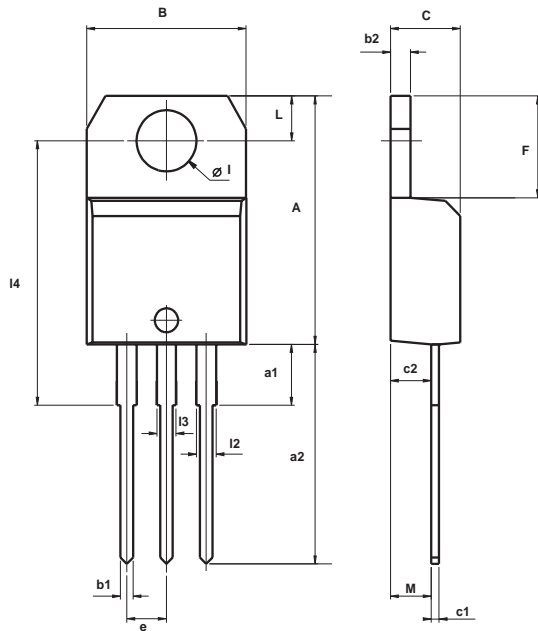


Fig. 12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$ .

**Package Mechanical Data**
**TO-220AB (Plastic)**


REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
B	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
C	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
e	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
I	3.75		3.85	0.147		0.151
I4	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
I2	1.14		1.70	0.044		0.066
I3	1.14		1.70	0.044		0.066
M		2.60			0.102	