Bt424

250 MHz 40-bit Multitap TTL/ECL-Compatible Video Shift Register

Distinguishing Features

- 250 MHz Operation
- Overlay Support
- TTL Pixel Inputs
- TTL MPU Address Interface
- ECL Shift Register Outputs
- Shift-Enable and Output-Enable Controls
- Optional Single +5 V Operation
- 68-pin PGA Package with Alignment Pin
- Typical Power Dissipation: 1.25 W

Customer Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplifies PCB Layout
- Reduces PCB Interconnect
- Low Bus Loading
- Increases System Reliability

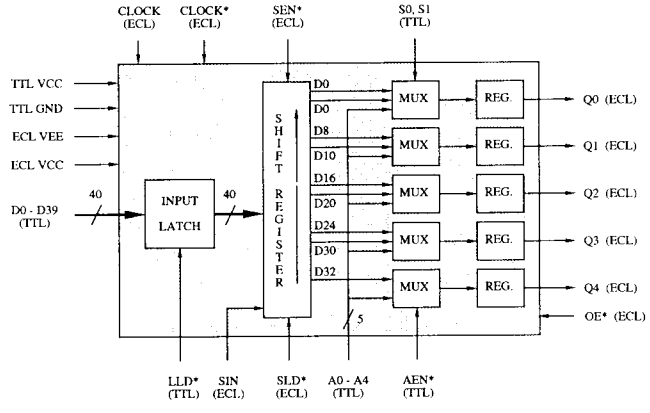
Configurations

- One 40-bit Shift Register
- Two 16-bit or 20-bit Shift Registers
- Five 8-bit Shift Registers
- Four 10-bit Shift Registers

Related Products

- Bt401/403
- Bt109
- Bt107
- Bt492

Functional Block Diagram



Product Description

The Bt424 is a 40-bit multitap shift register. It is designed specifically for high-resolution graphics systems.

TTL pixel data from the frame buffer is typically loaded at either one eighth or one tenth the clock rate (up to about 32 MHz) with the TTL-compatible LLD* signal. Data is then transferred from the input latch to the shift register using the ECL-compatible load signal (SLD*). The double-buffering of incoming pixel data simplifies system timing.

The shift register is clocked by the ECL-compatible CLOCK and CLOCK* inputs, and features ECL-compatible serial input (SIN) and shift-enable (SEN*) controls.

The Bt424 performs TTL-to-ECL translation of the MPU address (A0–A4), eliminating external address translators. The MPU address interface enables output of the MPU address (A0–A4) onto the Q0–Q4 pins, overriding the shift register data. This interface is controlled by the TTL-compatible address-enable (AEN*) signal.

The Bt424 has separate TTL and ECL supply pins, enabling operation from a single +5 V supply, or a +5 V and –5.2 V supply.

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Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) 843.3642 • TLX: 383 596 • FAX: (619) 452-1249
L424001 Rev. H

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt424 contains a 40-bit input latch, a 40-bit shift register, and control logic.

General Shift Register Operation

The 40-bit shift register has multiple taps, as illustrated in the functional block diagram. As illustrated in Figure 3 (Figures 3, 4, 5, 6, and 7 appear in the Timing Waveforms section, following AC characteristics), on the rising edge of LLD*, D0–D39 are latched into the input latch. Data is transferred from the input latch to the shift register synchronously on the rising edge of CLOCK while SLD* is a logical zero. While LLD* is a logical zero, the input latch is transparent, as illustrated in Figure 4.

The multiplexers select one of two taps from the 40-bit shift register or an MPU address input. The output of the multiplexers is registered synchronously to CLOCK and output onto the Q0–Q4 pins.

The SEN* input may be used to synchronously enable (logical zero) or disable (logical one) clocking of the shift register. This is useful for implementing hardware zooming in a graphics application. Figure 5 shows the shift timing and SEN* timing.

The OE* input is used to enable (logical zero) or disable (logical one) the outputs asynchronously to CLOCK, as shown in Figure 6.

Single 40-bit Shift Register Operation

When the Bt424 is used as a 40-bit shift register, only the Q0 output is used. The Q1–Q4 outputs are ignored. D0 is the first bit output, followed by D1, then D2, then D3, etc. SLD* and LLD* should occur once every 40 clock cycles. The state of the S0 and S1 inputs is not important, and they may be connected to TTL GND.

Single shift registers of any length (up to 40 bits) may be implemented by loading the parallel data at the appropriate time. For example, a 32-bit shift register may be implemented by loading parallel data once every 32 clock cycles.

Dual 20-bit Shift Register Operation

When the Bt424 is used as a dual 20-bit shift register, only the Q0 and Q2 outputs are used. The Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, then D2, then D3, etc. For Q2, D20 is the first bit output, followed by D21, then D22, etc. SLD* and LLD* should occur once every 20 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Dual 16-bit Shift Register Operation

When used as a dual 16-bit shift register, only the Q0 and Q2 outputs are used, and the Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, etc. For Q2, D16 is the first bit output, followed by D17, etc. SLD* and LLD* should occur once every 16 clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

Quad 10-bit Shift Register Operation

When the Bt424 is used as a quad 10-bit shift register, all output except Q4 (which is ignored) are used. For Q0, D0 is the first bit output, followed by D1, then D2, etc. For Q1, D10 is the first bit output, followed by D11, then D12, etc. For Q2, D20 is the first bit output, followed by D21, then D22, etc. For Q3, D30 is the first bit output, followed by D31, then D32, etc. SLD* and LLD* should occur once every 10 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Quint 8-bit Shift Register Operation

When the Bt424 is used as a quint 8-bit shift register, all outputs are used. For Q0, D0 is the first bit output, followed by D1, then D2, etc. For Q1, D8 is the first bit output, followed by D9, then D10, etc. For Q2, D16 is the first bit output, followed by D17, then D18, etc. For Q3, D24 is the first bit output, followed by D25, then D26, etc. For Q4, D32 is the first bit output, followed by D33, then D34, etc. SLD* and LLD* should occur once every eight clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

MPU Address Interface

The Bt424 accepts TTL-compatible MPU addresses (A0–A4) and translates them to ECL-compatible levels, eliminating the need for external TTL/ECL translators along the address path.

While AEN* is a logical one, pixel data from the shift register is output onto the Q0–Q4 pins. While AEN* is a logical zero, A0–A4 are output onto the Q0–Q4 pins. Figure 7 illustrates the MPU address timing. Q0–Q4 are always output following the rising edge of CLOCK regardless of the value of AEN*.

S0, S1 Select Inputs

S0 and S1 specify the configuration of the Bt424 as shown in Table 1.

S1	S0	Function
0	0	quad 10-bit
x	1	quint 8-bit
1	0	quad 8-bit, 8-bit overlay port

Table 1. S0, S1 Control Inputs.

Figure 1 shows use of the Bt424 in a typical graphics system. In this instance, the RAMDAC has separate (nonmultiplexed) pixel and overlay data inputs. Therefore, all three Bt424s are configured for the same mode of operation (either quad 10 bit or quint 8 bit, depending on the specific application).

Figure 2 shows a basic configuration of the Bt424 used with a RAMDAC that has multiplexed pixel and overlay inputs. The OL input of the RAMDAC specifies whether pixel (OL = 0) or overlay (OL = 1) data is present on P0–P7.

The Bt424s interfaced to bit planes 0–7 are configured to support overlays (S1 = 1 and S0 = 0). D0–D7, D8–D15, D16–D23, and D24–D31 are configured as four 8-bit pixel input ports, while D32–D39 are configured as an 8-bit overlay active input port. If D32–D39 contain a logical one on any bit, the Q0–Q3 outputs are disabled and forced to a logical zero. This enables overlay information to be wire-ORed onto the Q0–Q3 outputs.

The Bt424 interfaced to the overlay bit planes is configured as a quint 8-bit shifter and serializes the overlay information. The Q0–Q3 outputs are wire-ORed onto the pixel data bus to the RAMDAC. The D32–D39 inputs are serialized to generate the overlay enable (OL) control signal for the RAMDAC. If no overlay information is being displayed, the Q0–Q4 outputs are a logical zero, allowing normal pixel data to be displayed.

Eight four-input TTL OR gates are required to generate the overlay active signals to the Bt424s. D0, D8, D16, and D24 are ORed together to generate D32, D33, D34, etc.

Power Supply Operation

The Bt424 may operate from a +5 V and –5.2 V power supply, or from a single +5 V power supply, as called out in Table 2.

	Nominal Voltages Applied	
Supply Pin	Single Supply System	Dual Supply System
TTL VCC	+5.0 V	+5.0 V
TTL GND	0 V	0 V
ECL VCC	+5.0 V	0 V
ECL VEE	0 V	–5.2 V

Table 2. Power Supply Operation.

Inputs and outputs are temperature and voltage compensated.

Circuit Description *(continued)*

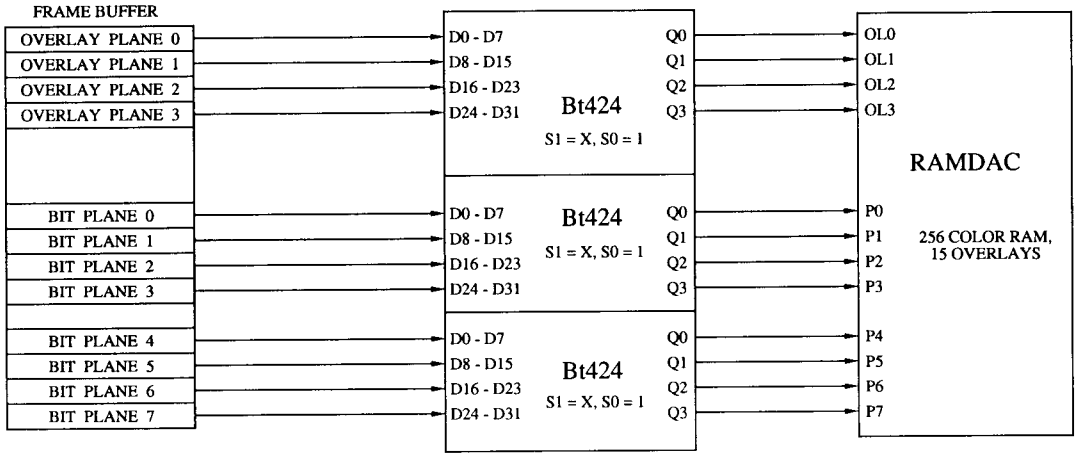


Figure 1. Using the Bt424 with Separate Pixel and Overlay Inputs (256 Colors, 15 Overlays).

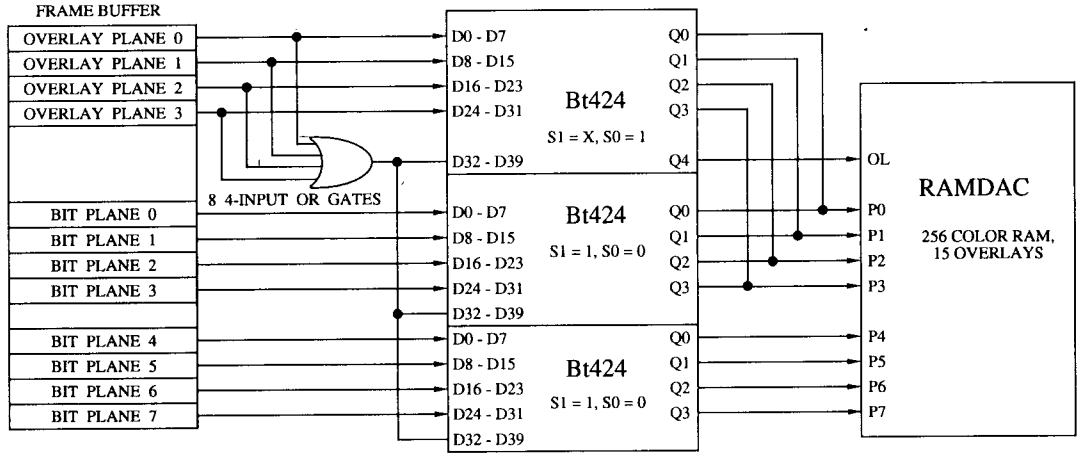


Figure 2. Using the Bt424 with Multiplexed Pixel/Overlay Inputs (256 Colors, 15 Overlays).

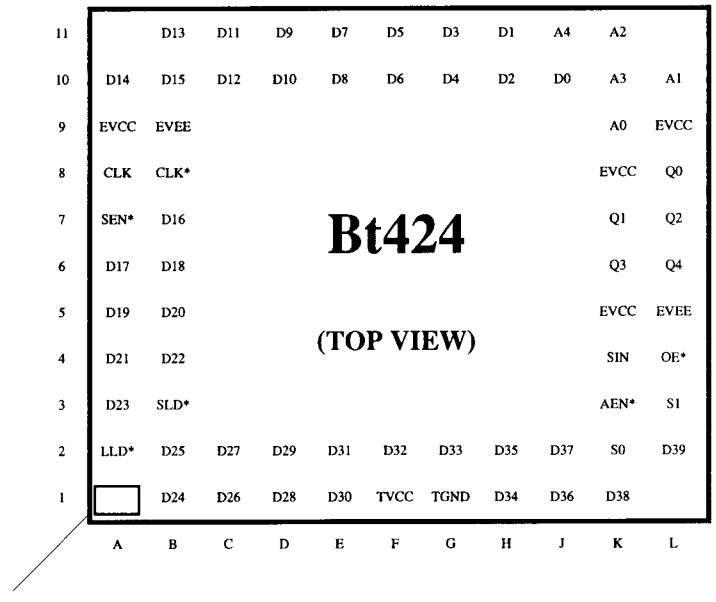
Pin Descriptions

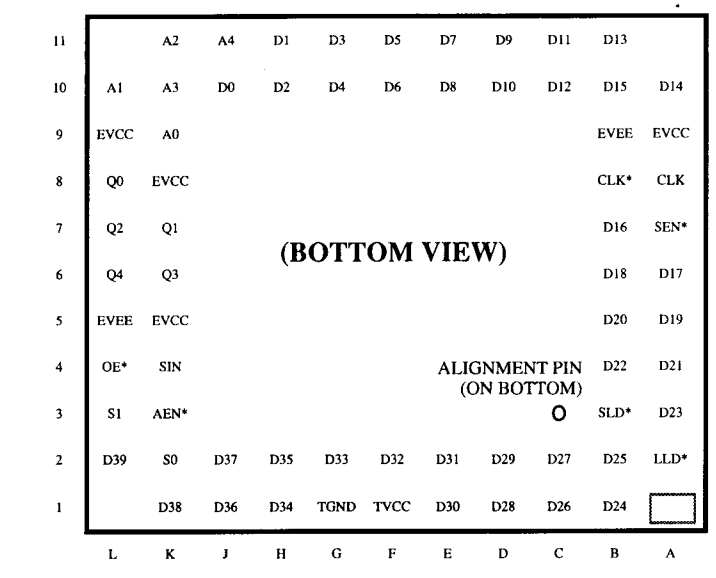
Pin Name	Description
D0–D39	Parallel data inputs (TTL compatible). These inputs are latched into the input latch on the rising edge of LLD*, asynchronous to CLOCK.
SIN	Shift data input (ECL compatible). This input is latched on the rising edge of CLOCK and may be used to serially load the shift register. If not used, it should be connected to ECL GND.
SEN*	Shift enable control input (ECL compatible). This input may be used to synchronously start or stop the shift register from clocking. A logical zero enables shifting, and a logical one disables shifting.
LLD*	Input latch load control input (TTL compatible). The rising edge of LLD* is used to latch D0–D39 into the input latch. While LLD* is a logical zero, the input latch is transparent.
SLD*	Shift register load control input (ECL compatible). SLD* is used to transfer data from the input latch to the shift register synchronously to CLOCK. Data is transferred on the rising edge of CLOCK while SLD* is a logical zero.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The clock rate is typically the pixel clock rate of the video system. The Bt424 may be used with a single-ended clock by connecting CLOCK* to VBB (–1.3 V)
Q0–Q4	Shift register outputs (ECL compatible). These pins output either D0–D39 data (AEN* = logical one) or A0–A4 data (AEN* = logical zero). Data is output following the rising edge of CLOCK.
OE*	Output enable control input (ECL compatible). A logical one forces the Q0–Q4 outputs to a logical zero, while a logical zero enables data to be output onto Q0–Q4. The Q0–Q4 outputs are enabled and disabled asynchronously to CLOCK.
S0, S1	Select control inputs (TTL compatible). These inputs control the operation of the device as specified in Table 1.
A0–A4	Address inputs (TTL compatible). These address inputs from the MPU are used to address the color palette RAM during MPU read/write cycles to the color palette RAM.
AEN*	Address enable control input (TTL compatible). While AEN* is a logical zero, A0–A4 are output onto Q0–Q4 following the rising edge of CLOCK. If AEN* is a logical one, A0–A4 are ignored.
TTL VCC	Power supply pins for the TTL-compatible circuitry.
TTL GND	Ground pins for the TTL-compatible circuitry.
ECL VEE	Power supply pins for the ECL-compatible circuitry.
ECL VCC	Ground pins for the ECL-compatible circuitry.

Pin Descriptions *(continued)*

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
CLOCK	A8	D0	J10	D25	B2
CLOCK*	B8	D1	H11	D26	C1
		D2	H10	D27	C2
LLD*	A2	D3	G11	D28	D1
SLD*	B3	D4	G10	D29	D2
SEN*	A7				
SIN	K4	D5	F11	D30	E1
S0	K2	D6	F10	D31	E2
S1	L3	D7	E11	D32	F2
		D8	E10	D33	G2
AEN*	K3	D9	D11	D34	H1
A0	K9				
A1	L10	D10	D10	D35	H2
A2	K11	D11	C11	D36	J1
A3	K10	D12	C10	D37	J2
A4	J11	D13	B11	D38	K1
		D14	A10	D39	L2
Q0	L8				
Q1	K7	D15	B10	TTL VCC	F1
Q2	L7	D16	B7		
Q3	K6	D17	A6	TTL GND	G1
Q4	L6	D18	B6		
		D19	A5	ECL VEE	B9
OE*	L4			ECL VEE	L5
		D20	B5		
		D21	A4	ECL VCC	A9
		D22	B4	ECL VCC	K5
		D23	A3	ECL VCC	K8
		D24	B1	ECL VCC	L9

Pin Descriptions *(continued)*





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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	V
ECL Device Ground	ECL VCC	0	0	0	V
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	V
ECL Power Supply	ECL VEE	–4.2	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+70	°C

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	V
TTL VCC (measured to TTL GND)				+7.0	V
Voltage on Any ECL Pin		0		ECL VEE	V
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	V
Q0–Q4 Output Current				–30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 1) Input Low Voltage (Note 1)	VIH VIL	–1165 –1810		–880 –1475	mV mV
Output High Voltage (Note 1) Output Low Voltage (Note 1)	VOH VOL	–1025 –1810		–880 –1620	mV mV
Input High Current (Vin = VIHmax) Input Low Current (Vin = VILmin)	IIH IIL			500 400	µA µA
ECL VEE Supply Current	IEE			240	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Note 1: Relative to ECL VCC.

TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (Note 1)	VIH	2.0		TTL VCC +0.5	V
Input Low Voltage (Note 1)	VIL	TTL GND –0.5		0.8	V
Input High Current (Vin = 2.4 V) Input Low Current (Vin = 0.4 V)	IIH IIL			70 –0.7	µA mA
TTL VCC Supply Current	ICC			100	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Relative to TTL GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			250	MHz
Clock Cycle Time	1	4			ns
Clock Pulse Width High Time	2	1.5			ns
Clock Pulse Width Low Time	3	1.5			ns
LLD* Pulse Width Low Time	4	7			ns
LLD* Setup Time	5	8			ns
SLD Setup Time	6	2			ns
SLD Hold Time	7	0.5			ns
D0–D39 Setup Time to LLD*	8	7			ns
D0–D39 Setup Time to Clock	9	10			ns
D0–D39 Hold Time to LLD*	10	0			ns
D0–D39 Hold Time to Clock	11	0			ns
Q0–Q4 Output Delay	12	1.5		4	ns
SEN* Setup Time	13	2			ns
SEN* Hold Time	14	1			ns
SIN Setup Time	15	2.5			ns
SIN Hold Time	16	1.5			ns
OE* Pulse Width Low Time	17	4			ns
OE* Enable Time	18			3.5	ns
OE* Disable Time	19			4	ns
A0–A4 Setup Time	20	12			ns
A0–A4 Hold Time	21	0			ns
AEN* Setup Time	22	5			ns
AEN* Hold Time	23	0			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are –0.89 to –1.69 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Timing Waveforms

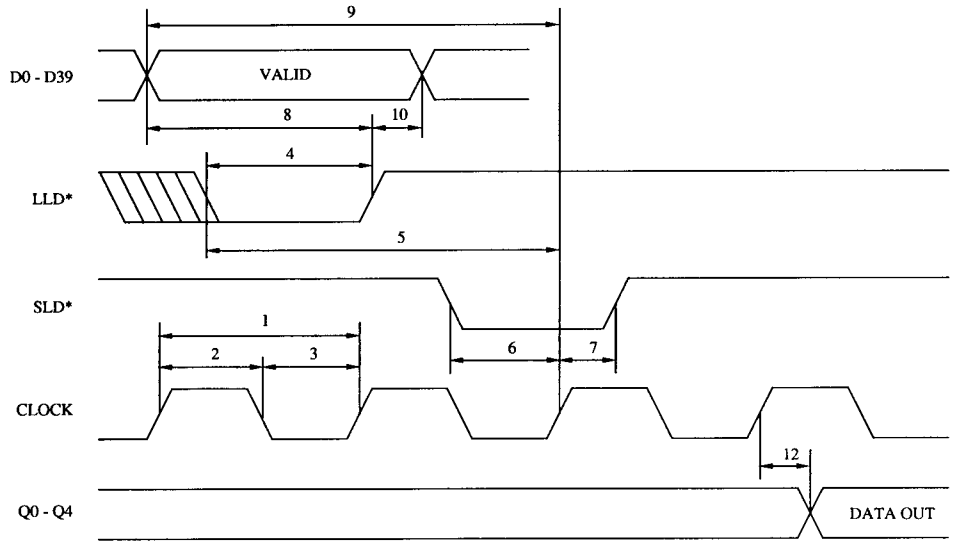

Figure 3. Load Latch and Register Timing.

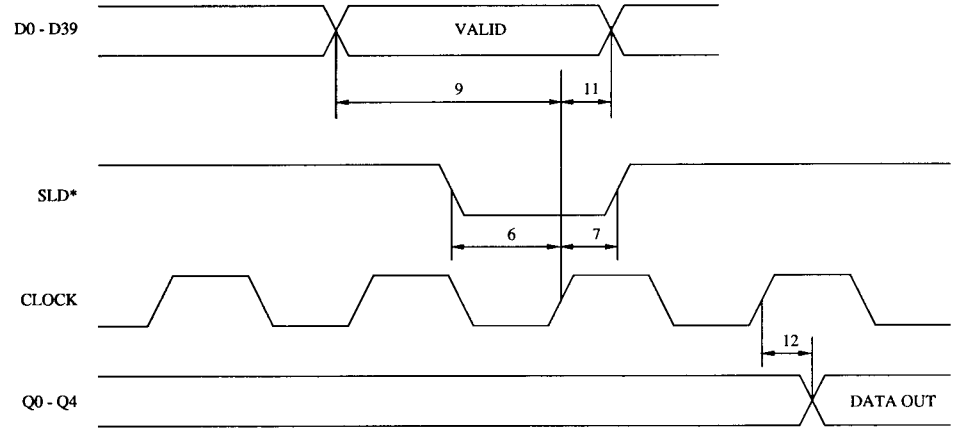

Figure 4. Transparent Latch Timing (LLD = Logical Zero).*

Timing Waveforms *(continued)*

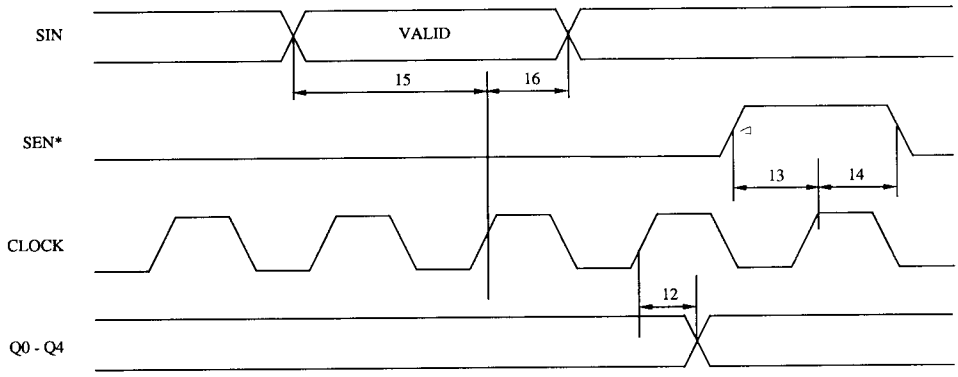

Figure 5. Shift Timing (SLD = Logical One).*

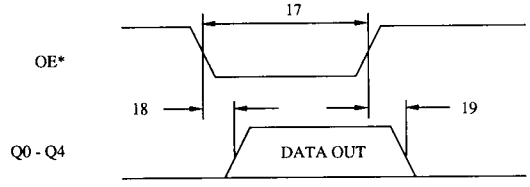

Figure 6. Output Enable Timing.

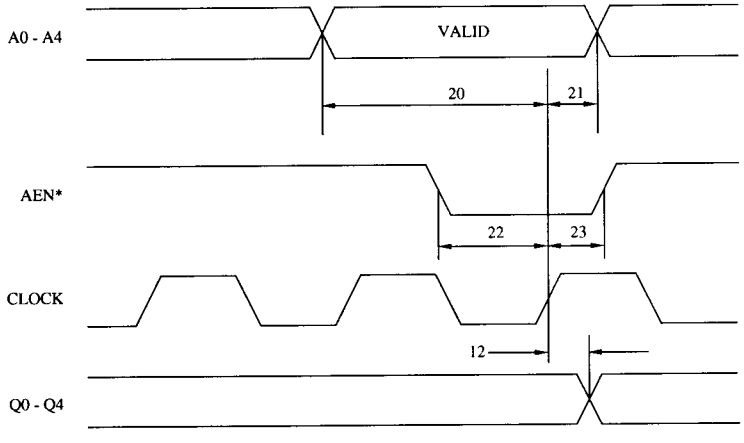

Figure 7. Address Enable Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt424KG	68-pin Ceramic PGA with Alignment Pin	0° to +70° C