Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice. Please consult Brooktree for the most recent datasheet before design.

Bt440

275 MHz PLL Clock Generator for CMOS RAMDACs™

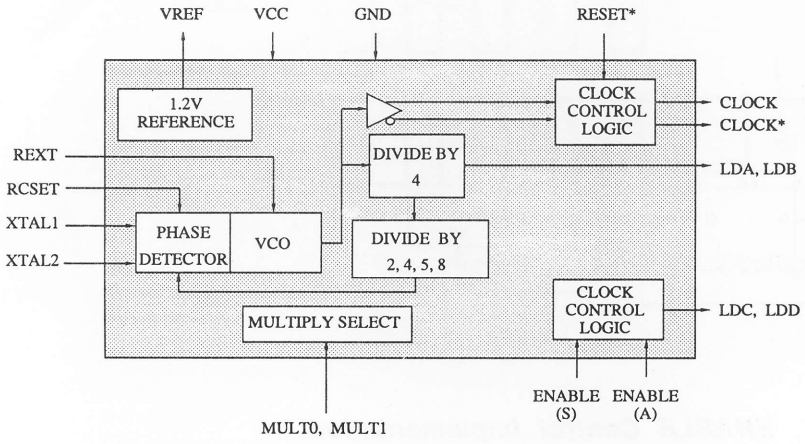
Distinguishing Features

- 275 MHz Operation
- Phase Lock Loop (PLL) Capability
- Pixel Clock 8x, 16x, 20x, 32x Crystal
- Differential ECL Clock Generation
- Divide by 4 of the Clock
- Resets Pipeline Delay of the RAMDAC
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 28-pin PLCC Package
- Typical Power Dissipation: 800 mW

Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability
- Easy to Implement

Functional Block Diagram



Product Description

The Bt440 is a clock generator for the high-speed Brooktree CMOS RAMDACs. It interfaces to a low-frequency quartz crystal and multiplies the crystal frequency by 8x, 16x, 20x, and 32x to generate the pixel clock signals that drive the RAMDAC.

The Bt440 requires no coils or variable capacitors for operation. Frequency range is set through an external resistor. The Bt440 loop filter utilizes standard RC components.

The pixel clock output is divided by four to generate the load signal.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt440 can also configure the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2 V voltage reference is also provided, and may be used to provide the reference voltage for one to four RAMDACs.

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Circuit Description

The Bt440 is designed to interface to low-frequency crystal and generate the clock signals required by the RAMDACs. The XTAL1 and XTAL2 inputs interface to a quartz crystal, yielding a cost-effective clock generation system.

The CLOCK and CLOCK* outputs interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5 V power supply.

MULT0 and MULT1 determine the multiplication factor for the pixel clock. The input oscillator frequency is multiplied by 8, 16, 20, or 32, depending on the MULT0 and MULT1 settings. See Table 1.

When using the MULT0 and MULT1 to change to a different multiplication factor, RESET is not required. A phase lock loop will lock into the new frequency after a minimum time.

The LDA and LDB signals are generated by the pixel clock divided by 4. The LDA signal will interface directly to the LD* signal of the RAMDAC. The LDB, LDC, and LDD interface to the VRAMs. For all frequencies, LDA, LDB, LDC, and LDD maintain the same CLOCK/4 relationship.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero.

ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the same state.

While both ENABLE (S) and ENABLE (A) are a logical one, LDC and LDD will be free-running and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally non-clocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt440, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt440 to set the pipeline delay of the RAMDACs to a specified number of clock cycles (the exact number is dependent on the RAMDAC). Following the first rising edge of XTAL1 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of XTAL1, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt440 also generates a 1.2 V (typical) voltage reference, which may be used to drive the VREF input of one to four RAMDACs.

MULT1	MULT0	Pixel Clock
0	0	x8
0	1	x16
1	0	x20
1	1	x32

Table 1. Pixel Clock Multiplication Frequency.

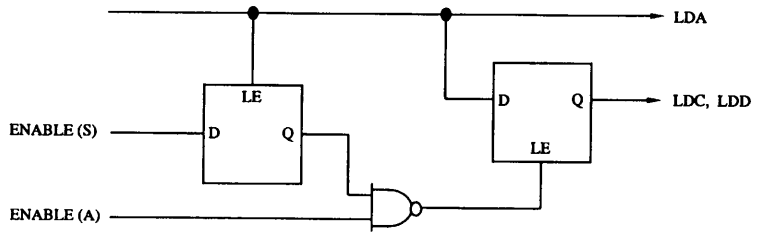


Figure 1. ENABLE Control Implementation.

Circuit Description *(continued)*

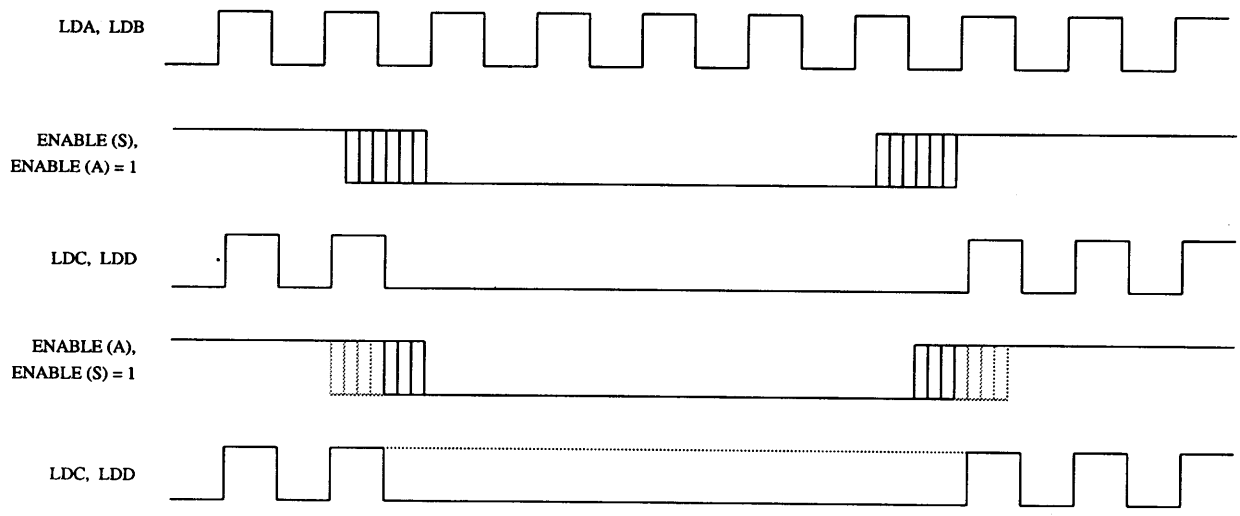


Figure 2. Load Output Timing.

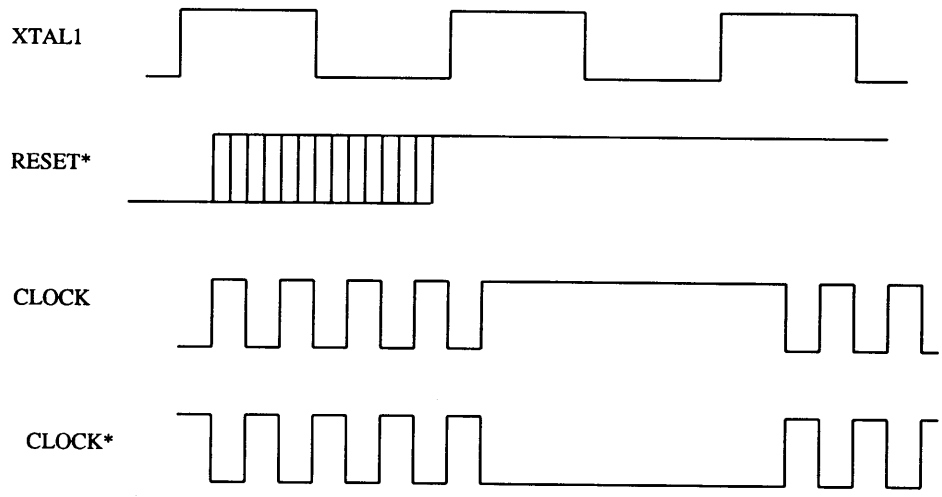


Figure 3. RESET* Timing.

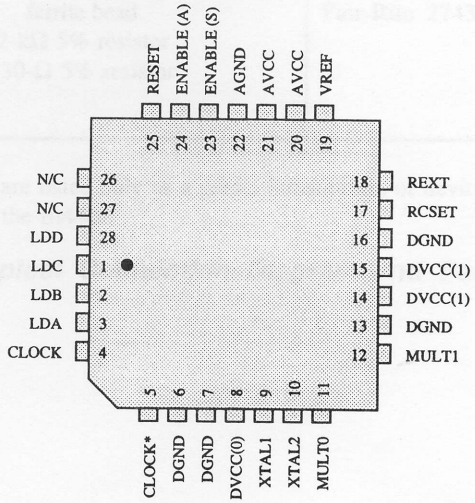
Pin Descriptions

Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be used to drive the VREF input of one to four RAMDACs.
XTAL1	Quartz crystal input. This input provides the base frequency for multiplication by the PLL circuitry.
XTAL2	Quartz crystal output.
CLOCK, CLOCK*	Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the crystal oscillator input rate times the multiplication factor. The multiplication factor is determined by MULT0 and MULT1. CLOCK AND CLOCK* are capable of driving up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply.
MULT0, MULT1	Multiply control inputs (TTL compatible). These inputs determine the multiplication factors for the pixel clock.
LDA, LDB	Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by 4. Each output may drive up to 20 pF without external buffering.
LDC, LDD	Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs. Each output may drive up to 20 pF without external buffering.
REXT	External Resistor. Sets the frequency range of the voltage control oscillator (VCO).
RCSET	RC Network. Filters the control voltage to the VCO. Consists of two capacitors and one resistor.

Pin Descriptions *(continued)*

Pin Name	Description
ENABLE (S)	Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs.
ENABLE (A)	Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the same state. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs.
RESET*	Reset control input (TTL compatible). Following the first rising edge of XTAL1 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of XTAL1, the CLOCK and CLOCK* outputs are set to be free-running. Care must be taken to avoid glitches on this edge-triggered input.
AVCC	Analog Device power. All AVCC pins must be connected.
DVCC(0), DVCC(1)	Digital Device power. All DVCC pins must be connected.
AGND	Analog Device ground. All AGND pins must be connected.
DGND	Digital Device ground. All DGND pins must be connected.

28-pin Plastic J-Lead (PLCC) Package with Internal Heatspreader



PC Board Layout Considerations

Power Planes

A single heavy ground plane should be used.

All of the VCC pins should be decoupled on the top PCB layer next to the device. A parallel 0.1 and 0.01 uF chip capacitor is recommended. See Figure 4.

Due to the large transient response of the TTL outputs, the DVCC(0), should be isolated through a ferrite bead to the PCB power plane.

External Loop Components

All of the external loop components (REXT and RCSET) should be placed on the top PCB layer in close proximity of the device. See Table 2 for REXT versus Pixel Clock rates.

High stability and ultra low-leakage components should be used (chip capacitors and chip resistors are recommended).

Pixel Clock Outputs

The CLOCK and CLOCK* outputs should be terminated on the top PCB layer at the Bt440 with 220 Ω chip resistors and then cross-terminated with 150 Ω as close as possible to the RAMDAC. See Figure 5.

The clock traces should be of equal length and continuous on one trace layer. Through-holes, 90 degree angles, and stubs should be avoided to reduce any signal reflections.

General

Unused TTL outputs should be left floating.

The Bt440 should not be located on the board where large transient currents, or large electric or magnetic fields are expected.

The Bt440 should not be socketed.

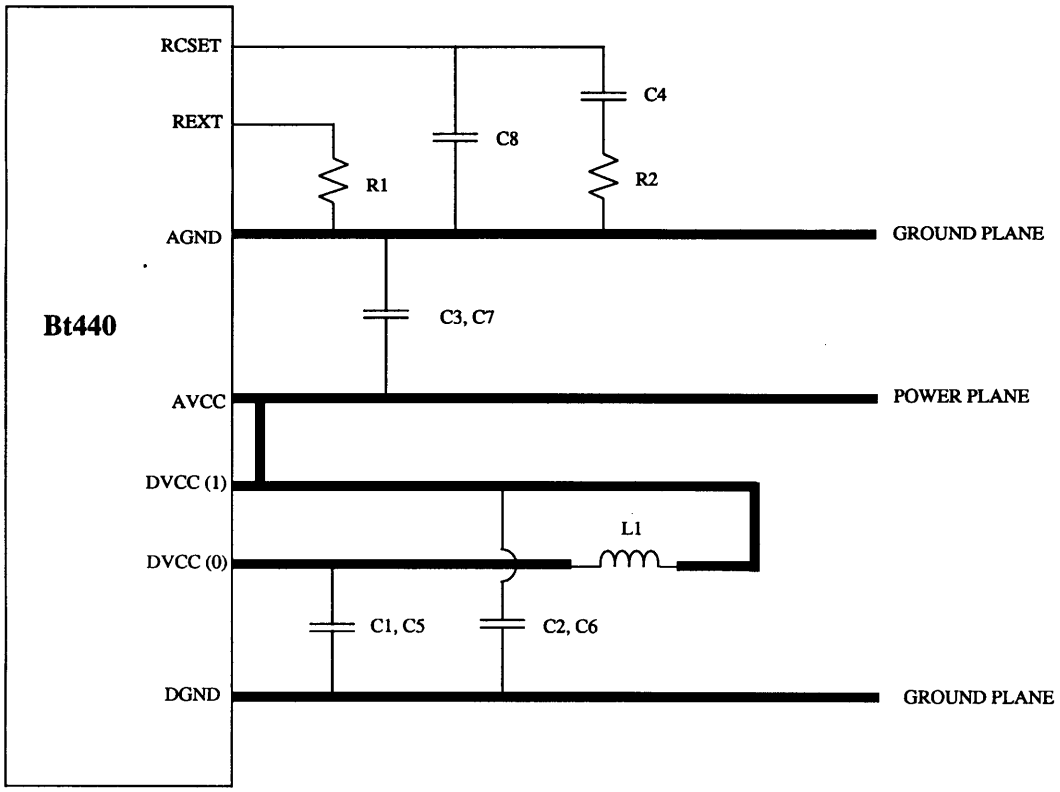
Wire-wrapped boards will not work.

If the LDC and LDD TTL outputs are not used, they should be disabled by tying E(s) to GND. This will reduce the CLOCK jitter and increase the stability of the Bt440.

REXT	Minimum Crystal Frequency	Maximum Crystal Frequency	Minimum Pixel Clock Rate	Maximum Pixel Clock Rate
2 kΩ	5 MHz	15 MHz	80 MHz	275 MHz

Table 2. REXT versus Pixel Clock Rates.

PC Board Layout Considerations *(continued)*



Note: Connect the decoupling capacitors as close as possible to the power pins.

Location	Description	Vendor Part Number
C1–C4	0.1 uF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C5–C8	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
L1	ferrite bead	Fair-Rite 2743001111
R1	2-kΩ 5% resistor	
R2	330-Ω 5% resistor	

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt440.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

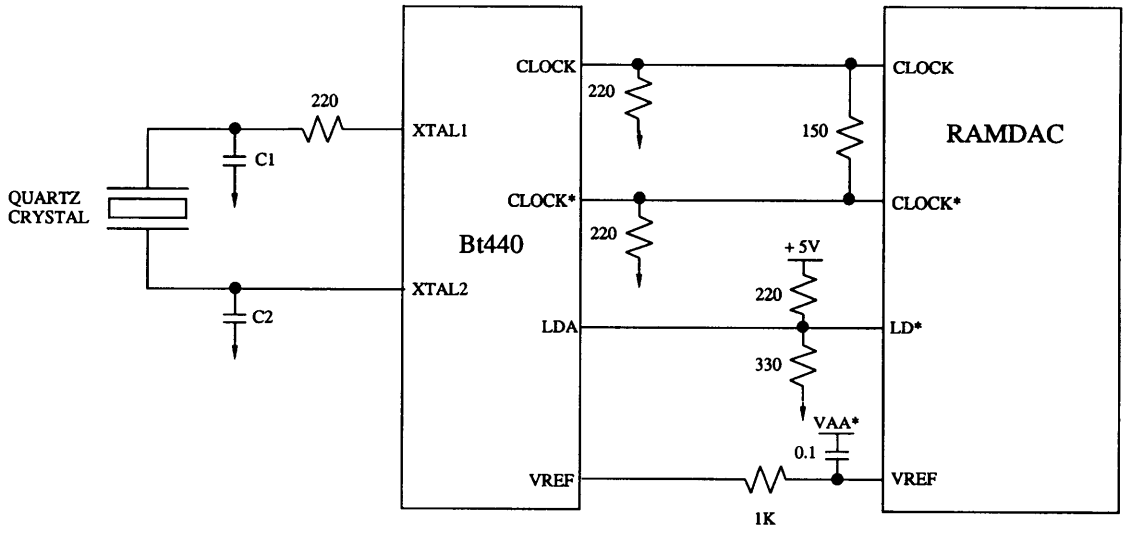
Interfacing to the RAMDAC

Figure 5 illustrates the interfacing of the Bt440 to the RAMDAC when using a quartz crystal oscillator. Figure 6 illustrates the interfacing of the Bt440 to a TTL clock oscillator. The Bt440 should be located as close as possible to the RAMDAC.

Termination resistors are required on the CLOCK and CLOCK* lines, located as close as possible to the Bt440.

The Bt440 may drive the CLOCK and CLOCK* inputs of one to four RAMDACs if they are located as close as possible to each other. Due to the inability to ensure proper synchronization between Bt440s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1k-Ω (typical) resistor must be used to isolate the VREF output of the Bt440 from the VREF input of the RAMDAC. This isolates Bt440 voltage reference noise from being coupled onto the RAMDAC VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor, as specified in its datasheet.



*Decoupling capacitor may require connection to ground, depending on VAA noise level.

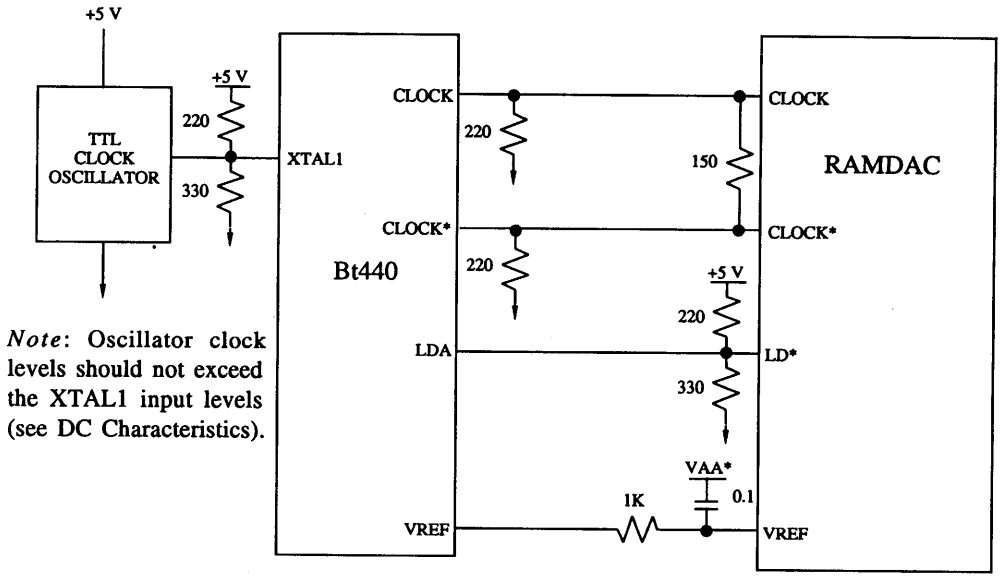
C1 min = 20 pf
C2 min = 100 pf

C2 > C1 by 30 pf

High stability and ultra low-leakage components should be used (chip capacitors and chip resistors are recommended).

Figure 5. Interfacing to a Quartz Crystal.

Application Information *(continued)*



Note: Oscillator clock levels should not exceed the XTAL1 input levels (see DC Characteristics).

*Decoupling capacitor may require connection to ground, depending on VAA noise level.

Figure 6. Interfacing to a TTL Clock Oscillator.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+ 70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Pin		GND–0.5		VCC + 0.5	V
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+ 125	°C
Storage Temperature	TS	–65		+ 150	°C
Junction Temperature	TJ			+ 175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4		pF
XTAL1 (at 25 °C)					
Input Voltage	VIH	2		4	V
	VIL	GND–0.5		0.8	V
Load Outputs					
Output High Voltage (IOH = –2 mA)	VOH	2.4			V
Output Low Voltage (IOL = 24 mA)	VOL			0.5	V
Output Capacitance			10		pF
Clock Outputs (at 25° C)					
Differential Output Voltage	ΔVOUT	.6			V
Output Capacitance	COUT		7		pF
Voltage Reference					
Output Voltage	VREF	1.2	1.235	1.26	V
Output Current	IREF		100		µA
VCC Supply Current	ICC		150	185	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC – 2 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Pixel Clock Rate	Fmax	80		275	MHz
Crystal Frequency	XTALmax	5		15	MHz
LDA, LDB, LDC, LDD (Note 1)	LDmax			70	MHz
XTAL1 High Time (Note 2)	1	40			%
XTAL1 Low Time (Note 2)	2	40			%
CLOCK to LDA Skew (Note 3)	3		4		ns
LDA, LDB Pulse Width Low		tbd			ns
LDA to LDB Output Skew (Note 3)			tbd		ns
LDA to LDC Output Skew (Note 3)			tbd		ns
LDC to LDD Output Skew (Note 3)			tbd		ns
PLL Acquire time		tbd	tbd	tbd	ms
E(S) Setup	4	tbd			ns
E(S) Hold	5	tbd			ns
E(A) Setup	6	tbd			ns
E(A) Hold	7	tbd			ns
RESET* Active Low Time	8	tbd			ns
RESET* Setup Time	9	tbd			ns
Pixel Clock Jitter (Note 4)				1	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤3 ns, measured between 10 percent and 90 percent points. ECL input values are 3.2–4.2 V, with input rise/fall times ≤1 ns, measured between 20 percent and 80 percent points. Timing reference points at 50 percent for inputs and outputs.

Note 1: For load frequencies greater than 35 MHz, a termination scheme of 220 Ω pull-up to VCC and 330 Ω pull-down to ground is required.

Note 2: Applies to the use of TTL clock oscillators

Note 3: LD outputs equally loaded with 20 pF. Unequal loading may result in additional output skew.

Note 4: Jitter is measured as the worst case spread from shortest to longest cycle time after sampling at 30 MHz for 10,000 pixel clocks.

Timing Waveforms

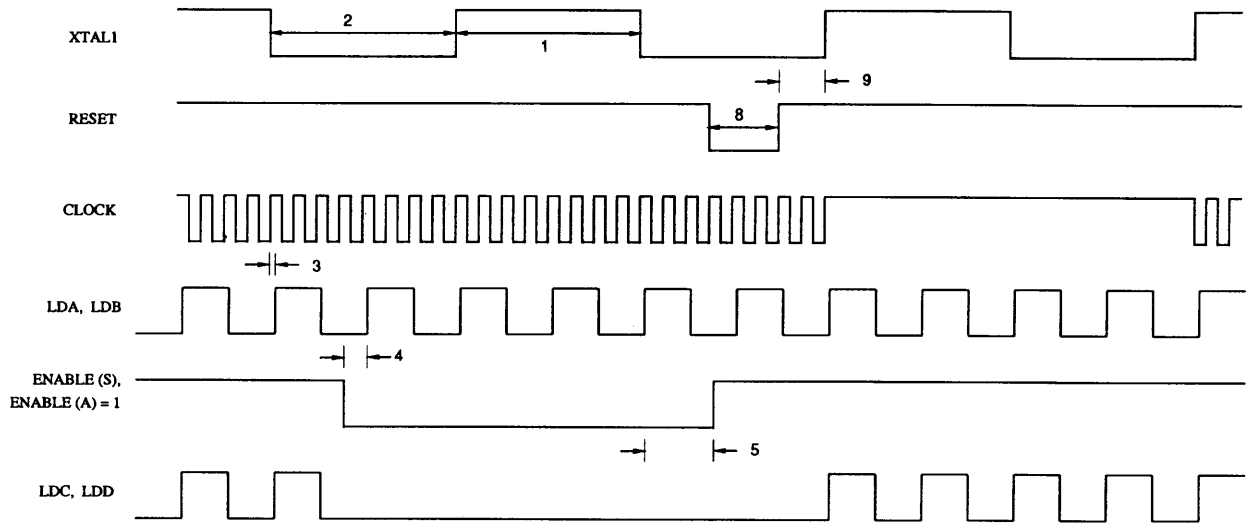


Figure 7. Synchronous Enable Operation.

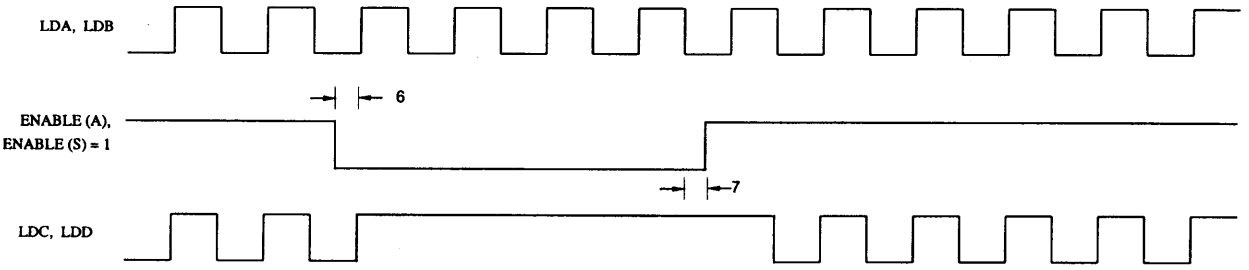


Figure 8. Asynchronous Enable Operation (16x Mode). Enable (A) Operation Pulled High Coincident When LDA and LDB are Low.

Timing Waveforms *(continued)*

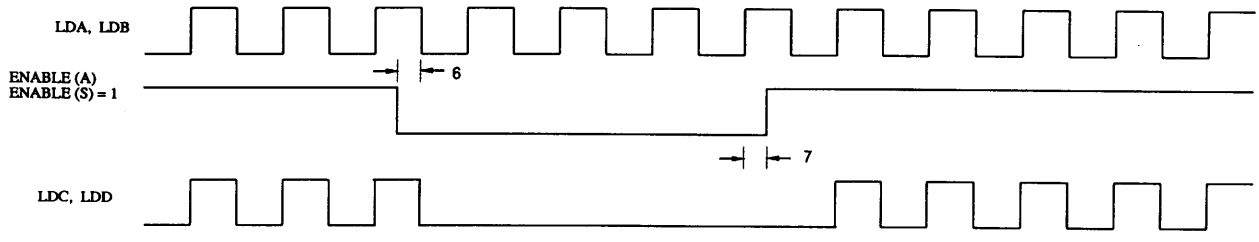
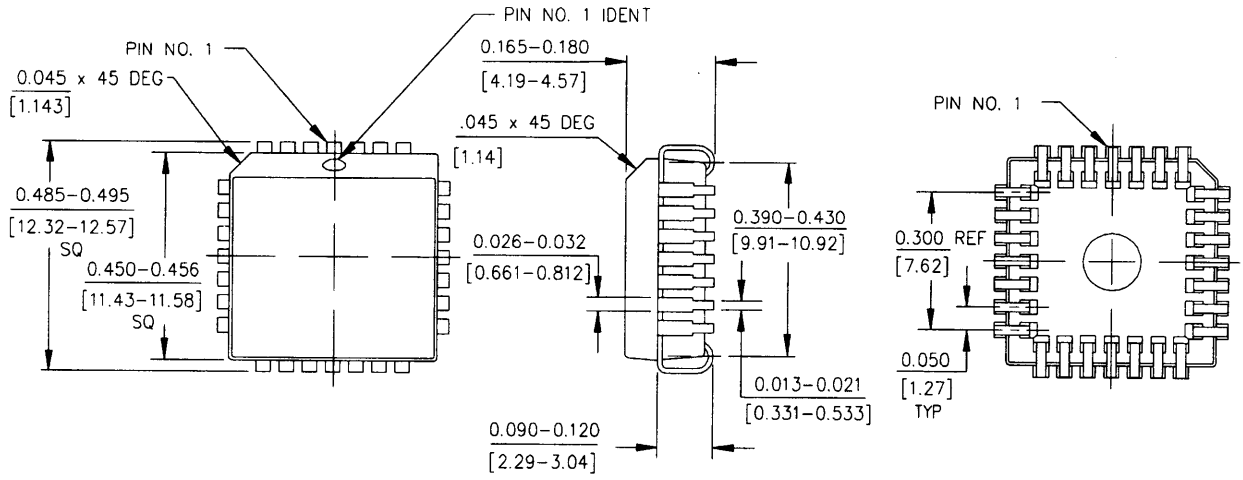


Figure 9. Asynchronous Enable Operation (16x Mode). Enable (A) Operation Pulled High Coincident When LDA and LDB are High.

Package Drawing—28-pin Plastic J-Lead (PLCC) with Internal Heat Spreader



NOTES—Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt440KHJ	28-pin PLCC with internal heat spreader	0° to +70° C

Revision History

Revision	*Change from Previous Revision*
A	Advance Release.

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Print date 2/18/92

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CAUTION

ESD-sensitive device. Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.

Do not insert this device into powered sockets.

Remove power before insertion or removal.

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