Datasheet

BT860-Sx

Bluetooth v5.0 Dual-Mode UART HCI Module

Version 3.0

Revision History

Version	Date	Notes	Contributor	Approver
1.0	12 Jan 2018	Initial Version	Jacky Kuo Raj Khatri	Jonathan Kaye
1.1	05 Feb 2018	Updated moisture sensitivity level from 4 to 3	Connie Lin	Jonathan Kaye
1.2	18 Feb 2019	Update BT SIG info with v5.0; Added KC certification info	Sue White	Jonathan Kaye
1.3	21 April 2020	Fixed Japan certification number	Sue White	Jonathan Kaye
1.4	04 Sept 2020	Updated EU regulatory section with new standards	Ryan Urness	Jonathan Kaye
1.5	13 Oct 2020	Removed references to the EN 301 893 EU standard	Miles Chung	Jonathan Kaye
1.6	20 Nov 2020	Updated all regulatory information	Ryan Urness	Jonathan Kaye
1.7	05 Jan 2021	Added Section 8.5 Reset and POR (Power on Reset)	Jacky Kuo	Jonathan Kaye
1.8	05 Feb 2021	Updated mechanical dimension	Jacky Kuo	Jonathan Kaye
1.9	13 Nov 2023	Updated minimum time before re-asserting RESET to 1.6 seconds in 8.5 Reset and POR (Power on Reset)	Andrew Chen	Jonathan Kaye
2.0	1 Nov 2024	Updates to Bluetooth SIG Approvals	Dave Drogowski	Jonathan Kaye
3.0	24 Jan 2025	Ezurio rebranding	Sue White	Dave Drogowski

Contents

1 Scope

This document describes key hardware aspects of the Ezurio BT860-Sx Bluetooth HCI modules. This document is intended to assist device manufacturers and related parties with the integration of this module into their host devices. Data in this document are drawn from several sources including data sheets for the CYW20704A2.
Because the BT860-Sx is currently in development stage, this document is preliminary and the information in this document is subject to change. Please contact Ezurio or visit the Ezurio website at https://www.Ezurio.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bt86x-series to obtain the most recent version of this document.

BT860-SA module

BT860-ST module

2 Operational Description

The BT860-Sx series of UART HCI modules leverage the Cypress CYW20704 A2 chipset to provide exceptionally low power consumption with outstanding range for OEMs needing both Classic Bluetooth and Bluetooth Low Energy support. The Bluetooth v5.0 core specification shortens your development time and provides enhanced throughput, security and privacy.

The BT860-Sx modules are ideal when designers need both performance and minimum size. For maximum flexibility in integration, they support a host UART interface, I²S and PCM audio interfaces, GPIO, and Cypress'GCI coexistence (2-Wire). The modules provide excellent RF performance and identical footprint options for integrated antenna or an external antenna via a trace pin.

These modules present a Bluetooth standard HCI interface with support for Linux / Android and Embedded Bluetooth software stacks for operating system backed devices. Additionally, Ezurio has partnered with Searan for support of their ultra small, flexible 'dotstack' platform for embedded Cortex M3 and M4 implementations.

2.1 Features and Benefits

- Bluetooth v5.0 - Dual mode (Classic Bluetooth and BLE)
- Compact footprint
- 2-wire Cypress Global Coexistence Interface (GCI)
- High antenna radiation gain and efficiency
- Good interference rejection for multi-com system (GSM/WCDMA)
- Class 1 output – 8 dBm
- UART, I²S, and PCM
- Industrial Temperature Range
- 512 Kbits EEPROM support
- Bluetooth Controller subsystem
- FCC, IC, CE, RCM, KC, and Giteki approvals

2.2 Application Areas

- Medical devices
- ePOS terminals
- Barcode scanners
- Industrial Cable Replacement
- IoT PlatformsAutomotive Diagnostic Equipment
- Personal Digital Assistants (PDA)

3 Block Diagram and Descriptions

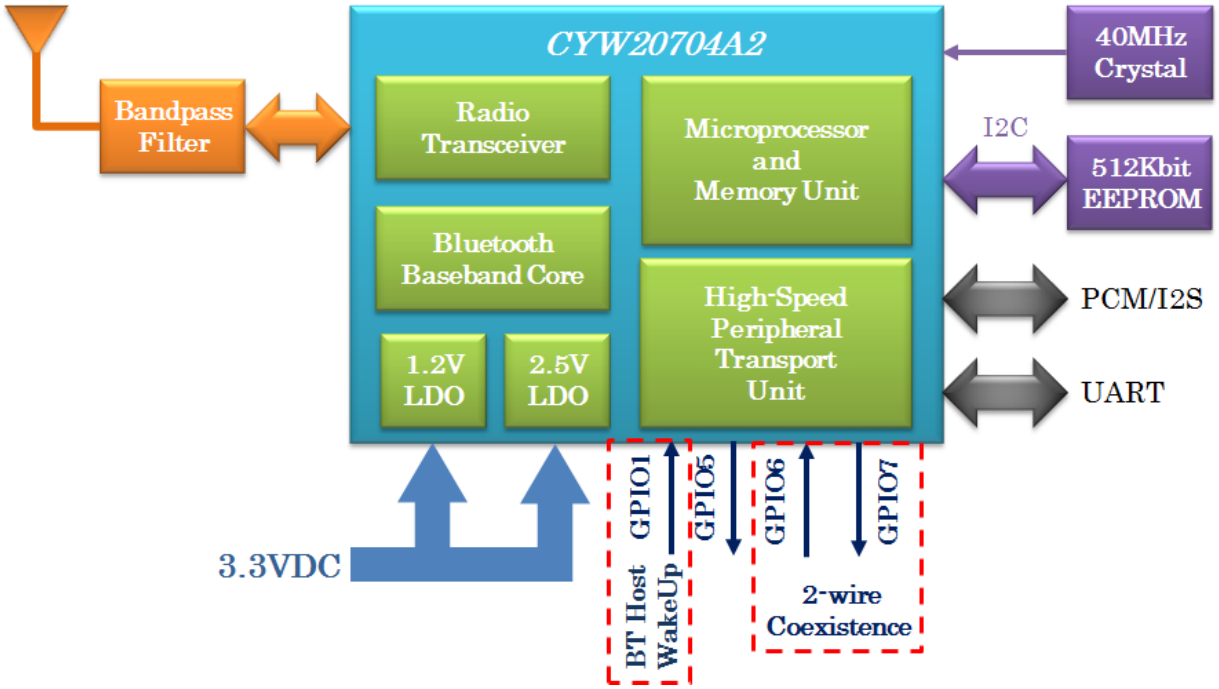

Figure 1: BT860 Module block diagram

CYW20704A2 (Main chip)	The BT860-Sx is based on CYW20704A2 dual mode chip. The chip is a single-chip radio with on-chip LDO regulators and baseband IC for Bluetooth 2.4 GHz systems including EDR to 3 Mbps. Dedicated signal and baseband processing is included for full Bluetooth operation. The chip provides I^2S/PCM and UART interfaces. There are two general purpose I/Os be configured for proprietary of Cypress GCI used and a general purpose I/O can be configured for scan/inquire/paging/data traffic of indicator. These three I/Os pins are controlled by firmware.
Antenna	BT860-SA – The antenna is a ceramic monopole chip antenna. BT860-ST – Trace Pad provision for use with a range of certified External Antennas
Band Pass Filter	The band pass filter filters the out-of-band emissions from the transmitter to meet the specific regulations for type approvals of various countries.
EEPROM	There are 512 Kbits EEPROM embedded on the BT860-Sx module which can be used to store parameters, such as BD_ADDR, maximum TX power, PCM configuration.
Crystal	The embedded 40 MHz crystal is used for generating the clock for the entire module.

4 Specifications

Table 1: BT860 specifications

Categories	Feature	Implementation
Wireless Specification	Bluetooth®	V5.0 Dual Mode (BR / EDR / LE)
	Frequency	2.402 - 2.480 GHz
	Maximum Transmit Power	Class 1 +8 dBm from antenna
	Receive Sensitivity	-94 dBm
	Range	Circa 100 meters
	Data Rates	Up to 3 Mbps (over-the-air)
Host Interface	UART	Up to 4 Mbps
	GPIO	3.3V for all general purpose I/Os
Operational Modes	HCI	Host Controller Interface over UART
EEPROM	2-wire	512 Kbits
Coexistence	802.11 (Wi-Fi)	2-Wire Cypress Global Coexistence Interface (GCI)
Supply Voltage	Supply	3.0V – 3.6V
Power Consumption	Current	Idle Mode ~8 mA File Transfer ~43 mA
Antenna Option	Internal External	Multilayer ceramic antenna Trace Pad
Physical (Width x Length x Height)	Dimensions	8.5 x 12.85 x 2.2 mm (BT860-SA) 8.5 x 12.85 x 1.9 mm (BT860-ST)
Environmental	Operating	-30° C to +85° C
	Storage	-40° C to +85° C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One-Year Warranty
Approvals	Bluetooth®	Controller Subsystem Approved
	FCC/IC/CE/RCM/KC/Giteki	All BT860-Sx series

5 Pin Definitions

Table 2: BT860 pin definitions

Pin No.	Pin Name	I/O	Supply Domain	Description	If Unused
1	NC				NC
2	GND	GND		Ground	GND
3	GPIO_5	Bi-directional	3V3	Programmable input/output line	
4	UART_RTS	Bi-directional	3V3	UART request to send output	NC
5	UART_TXD	Bi-directional	3V3	UART transmit data	NC
6	UART_CTS	Bi-directional	3V3	UART clear to send input	NC
7	UART_RXD	Bi-directional	3V3	UART receive data	NC
8	RESET	Input	3V3	Active-low reset input	N/A
9	3.3V	Input	3V3	Module main DC power supply, Input to internal 1.2V and 2.5V LDO	N/A
10	NC				NC
11	GND	GND		Ground	GND
12	GND	GND		Ground	GND
13	GND	GND		Ground	GND
14	GND	GND		Ground	GND
15	GND	GND		Ground	GND
16	GND	GND		Ground	GND
17	RF			BT860-ST RF signal output (50Ω) BT860-SA No connection	
18	GND	GND		Ground	GND
19	I2S_WS/PCM_SYNC	Bidirectional	3V3	PCM sync/I2S word select	NC
20	I2S_CLK/PCM_CLK	Bidirectional	3V3	PCM/I2S clock	NC
21	I2S_DI/PCM_IN	Bidirectional	3V3	PCM/I2S data input	NC
22	I2S_OUT/PCM_OUT	Bidirectional	3V3	PCM/I2S data output	NC
23	GND	GND		Ground	GND
24	NC				NC
25	BT_SECI_IN	Input	3V3	Coexistence data input	NC
26	BT_SECI_OUT	Output	3V3	Coexistence data output	NC
27	NC				NC
28	NC				NC
29	BT_HOST_WAKE	Output	3V3	BT device to wake up the Host	NC
30	GND	GND		Ground	NC

Pin Definition Note:

Note 1	The GPIO_5 controlled by the default firmware for the status of BT860 indications.

Operational Description

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These modules present a Bluetooth standard HCI interface with support for Linux / Android and Embedded Bluetooth software stacks for operating system backed devices. Additionally, Ezurio has partnered with Searan for support of their ultra small, flexible 'dotstack' platform.

6 DC Electrical Characteristics

Table 3: Absolute maximum rating

Rating	Min	Max	Unit
Storage temperature	-40	+150	^{0}C
Operating Temperature	-30	+85	^{0}C
ESD Contact Discharge	-4	+4	KV
ESD Air Discharge	-8	+8	KV
Moisture Sensitivity Level	3	-	-
3V3 Input	3.0	3.6	V

Table 4: Recommended operating conditions

Rating	Min	Max	Unit
Storage temperature	-40	+150	^{0}C
Operating Temperature	-30	+85	^{0}C
3V3 Input	3.0	3.6	V

Table 5: Digital I/O characteristics

Normal Operation	Min	Typ.	Max	Unit
V_{IL} Input Low Voltage (VDDO * = 3V3)	-	-	0.8	V
V_{IH} Input High Voltage (VDDO * = 3V3)	2.0	-	-	V
V_{OL} Output Low Voltage	-	-	0.4	V
V_{OH} Output High Voltage	3V3-0.4	-	-	V
I_{IL} Input Low Current	-	-	1.0	µA
I_{IH} Input High Current	-	-	1.0	µA
I_{OL} Output Low Current (VDDO * = 3V3, V_{OL} = 0.4V)	-	-	2.0	mA
I_{OH} Output Low Current (VDDO * = 3V3, V_{OH} = 2.9V)	-	-	2.0	mA
C_{IN} Input Capacitance	-	-	0.4	pF

*: The VDDO is denoted the digital I/O voltage and it's depended on the Pin9 (3V3) input of module.

Table 6: Current consumption

Normal Operation	Peak (8 dBm)	Unit
Idle	8	mA
Inquiry	23	mA
File Transfer	43	mA
BLE Connected (Master)	26	mA
BLE Scan (Master)	26	mA
BLE File Transfer	27	mA

7 RF Characteristics

Table 7: BDR/EDR/BLE transmitter characteristics (Input = 3V3 @ 25° C)

Parameter		Min	Typ.	Max	BT. Spec.	Unit
Classic BT (BDR) - GFSK Maximum RF Transmit Power		6	8	10	20	dBm
Classic BT - EDR Maximum RF Transmit Power		2	4	6	20	dBm
BLE Maximum RF Transmit Power		6	8	10	20	dBm
RF power variation over temperature range		-	2.0	-	-	dB
RF power variation over BT band		-	2	-	-	dB
RF power control step		2	4	8	-	dB
Initial Carrier Frequency Tolerance		-	10	-	±75	kHz
BLE Frequency Accuracy			10		±150	kHz
20 dB Bandwidth		-	920	-	1000	kHz
In-Band Spurious Emissions	1.0 MHz < IM-NI < 1.5 MHz	-	-	-39	-26	dBc
	1.5 MHz < IM-NI < 2.5 MHz	-	-	-39	-20	dBm
	IM-NI ≧ 2.5 MHz	-	-	-47	-40	dBm
BLE In-Band Emission	$f_{TX} \pm 2$ MHz	-	-	-48	-20	dBm
	$f_{TX} \pm [3 + n]$ MHz	-	-	-47	-30	dBm
Drift rate		-	10	-	+/-25	kHz
ΔF_{1Avg}		-	152	-	140< >175	kHz
ΔF_{2Max}		100	-	-	99.9	%
$\Delta F_{2Avg} / \Delta F_{1Avg}$		-	1.0	-	≧ 0.8	
BLE ΔF_{1Avg}		-	245	-	225< >275	kHz
BLE ΔF_{2Max}		100	-	-	99.9	%
BLE $\Delta F_{2Avg} / \Delta F_{1Avg}$		-	1.0	-	≧ 0.8	

Table 8: BDR/EDR/BLE receiver sensitivity (Input = 3V3 @ 25° C)

Parameter	Conditions	Min	Typ.	Max	BT. Spec.	Unit
Sensitivity	GFSK, 0.1% BER, 1Mbps	-	-90	-	-70	dBm
	π/4-DQPSK, 0.01% BER, 2Mbps	-	-94	-	-70	dBm
	8-DPSK, 0.01% BER, 3Mbps	-	-87	-	-70	dBm
	BLE GFSK, 30.8% PER, 1Mbps	-	-94	-	-70	dBm
Sensitivity variation	All Modulations (Over BT band)	-	2	-	-	dB

8 Interface

8.1 Global Coexistence Interface

The BT860-Sx supports the proprietary Cypress Global Coexistence Interface (GCI) which is a 2-wire interface.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over GCI_SECI_IN and GCI_SECI_OUT a two-wire interface, one serial input (GCI_SECI_IN), and one serial output (GCI_SECI_OUT). The both pins are controlled by the configuration file that is stored in EEPROM from the host.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

Table 9 shows the two-wire BT coexistence interface assignments.

Table 9: BT GCI Two-Wire Coexistence

Coexistence Signal Name	Signal Assignment
BT_SECI_IN	GPIO_6
BT_SECI_OUT	GPIO_7

8.2 UART Interface

The BT860-Sx has a single UART for Bluetooth. The UART is a standard four-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and 1040-byte transmits FIFO to support EDR. Access to the FIFO is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, and a custom Extended H4. The default baud rate is 115.2 Kbaud.

The BT860-Sx UART can perform XON/XOFF flow control and includes hardware support for Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For the BT860-Sx is supported BT to wake-up Host.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BT860-Sx UART operates correctly with the host UART if the combined baud rate error of the two devices is within ±2%.

Table 10: Example of common baud rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00

Table 11 and Figure 2 show UART timing of specifications.

Table 11: UART timing specifications

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time UART_CTS_N low to UART TXD valid	-	-	1.50	Bit periods
2	Setup time UART_CTS_N high before midpoint of stop bit	-	-	0.67	Bit periods
3	Delay time Midpoint of stop bit to UART_CTS_N high	-	-	1.33	Bit periods

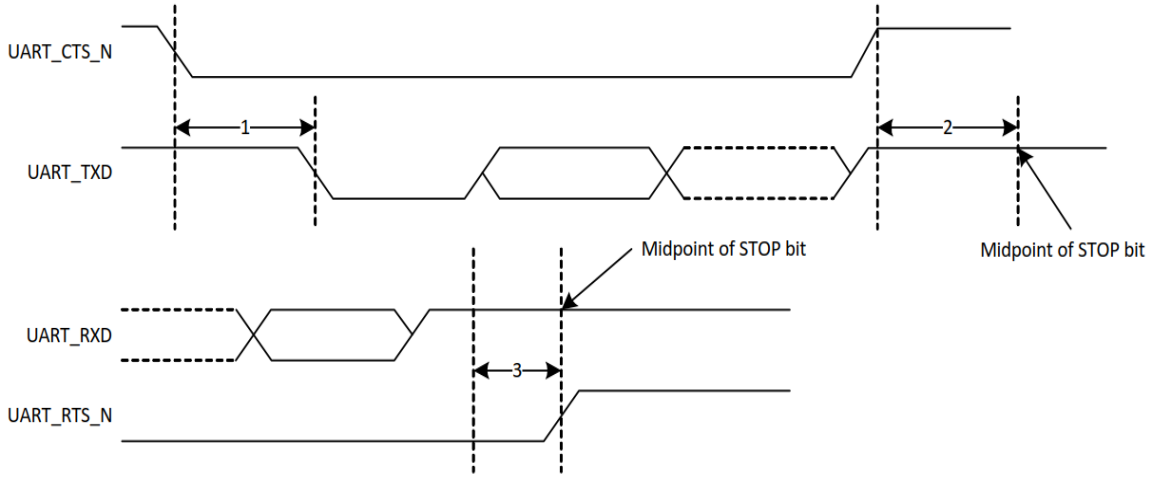


Figure 2: UART timing

8.3 PCM Interface

The BT860-Sx supports two independent PCM interfaces that share the pins with I2S interfaces. The PCM interface on the BT860-Sx can connect to linear PCM Codec devices in master or slave mode. In master mode, the BT860 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BT860.

The configuration of the PCM interface may be adjusted by the host using vendor-specific HCI commands.

For additional information, refer to the DVK-BT86x User Guide available from the BT86x product page of the Ezurio website.

8.3.1 Slot Mapping

The BT860-Sx supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rates is 1, 2, 4, 8 and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

8.3.2 Frame Synchronization

The BT860-Sx supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal uses an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock.

Figure 3 and Table 12 shows PCM Timing Diagram and Specifications for the master mode of short-frame.

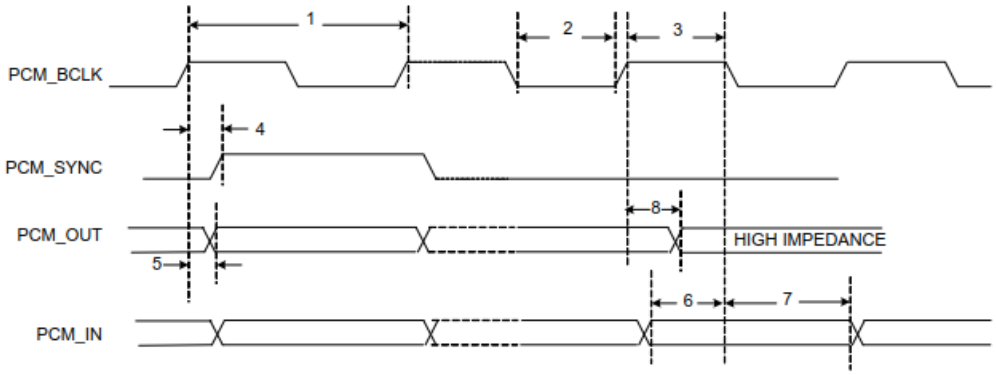


Figure 3: PCM timing diagram (Short-Frame Sync, Master Mode)

Table 12: PCM Interface timing specifications (Short-Frame Sync, Master Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Figure 4 and Table 13 shows PCM Timing Diagram and Specifications for the slave mode of short-frame.

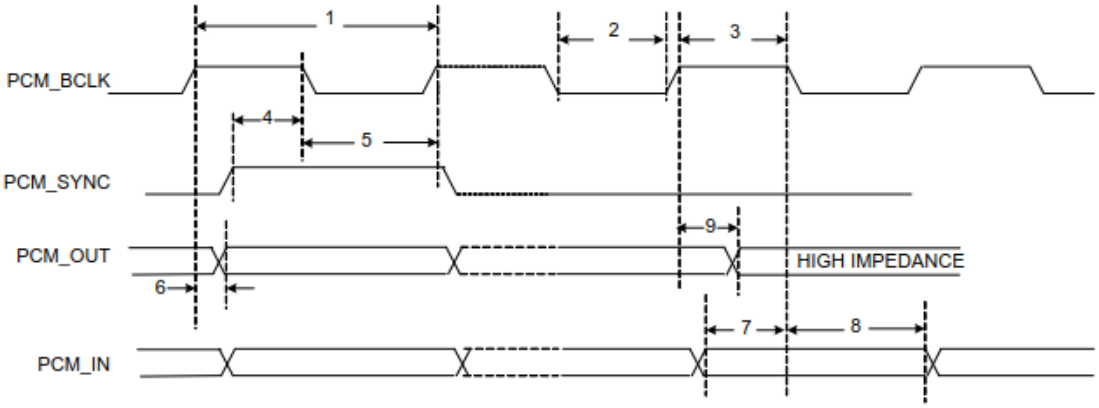


Figure 4: PCM timing diagram (Short-Frame Sync, Slave Mode)

Table 13: PCM Interface timing specifications (Short-Frame Sync, Slave Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC_hold	8	-	-	ns

Reference	Characteristics	Min.	Typ.	Max.	Unit
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Figure 5 through Table 14 shows PCM Timing Diagram and Specifications for the master mode of long-frame.

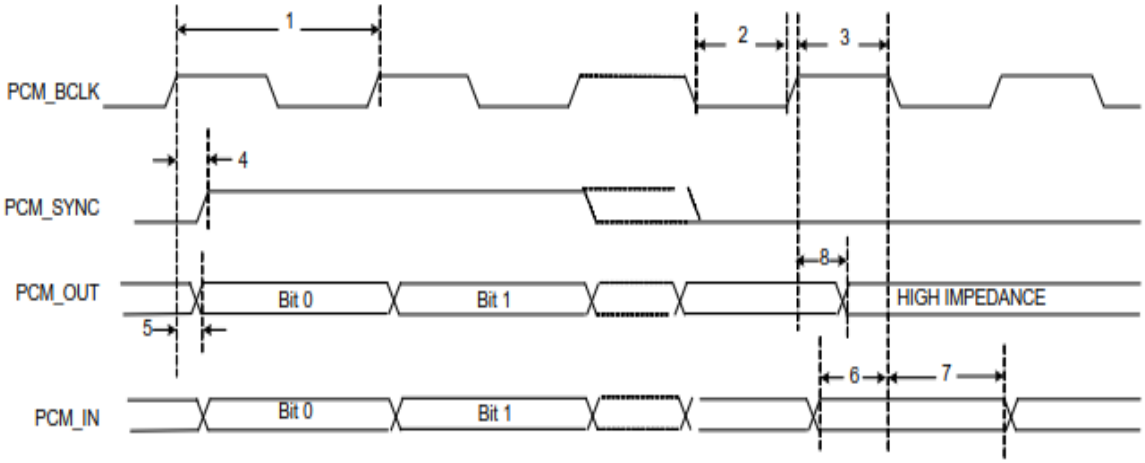


Figure 5: PCM timing diagram (Long-Frame Sync, Master Mode)

Table 14: PCM Interface timing specifications (Long-Frame Sync, Master Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Figure 6 and Table 15: PCM Interface timing specifications (Long-Frame Sync, Slave Mode) shows PCM Timing Diagram and Specifications for the slave mode of long-frame

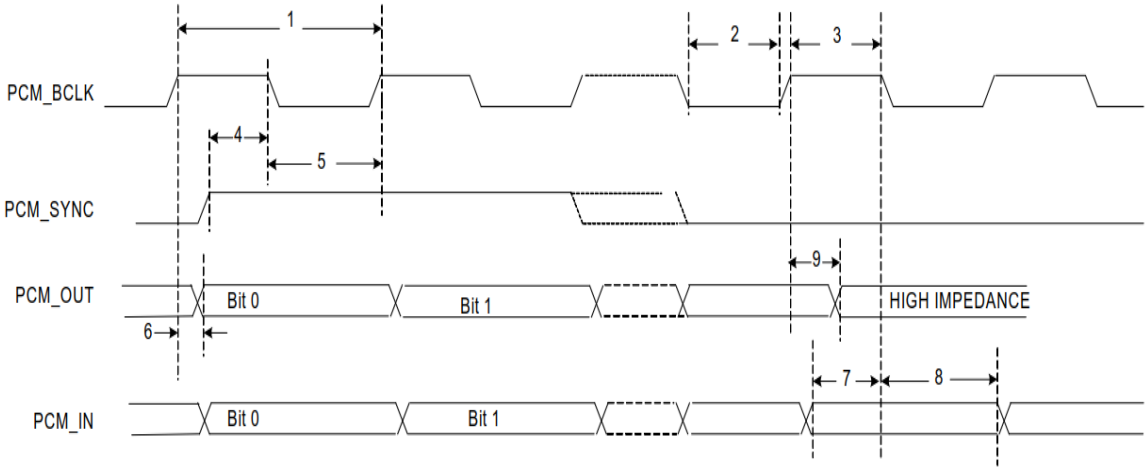


Figure 6: PCM timing diagram (Long-Frame Sync, Slave Mode)

Table 15: PCM Interface timing specifications (Long-Frame Sync, Slave Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC_hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

8.3.3 Data Formatting

The BT860-Sx may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BT860-Sx uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

8.3.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The BT860-Sx also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256Kbps rate) is transferred over the PCM bus.

8.3.5 Multiplexed Bluetooth Over PCM

Bluetooth supports multiple audio streams within the Bluetooth channel and both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. Figure7 shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

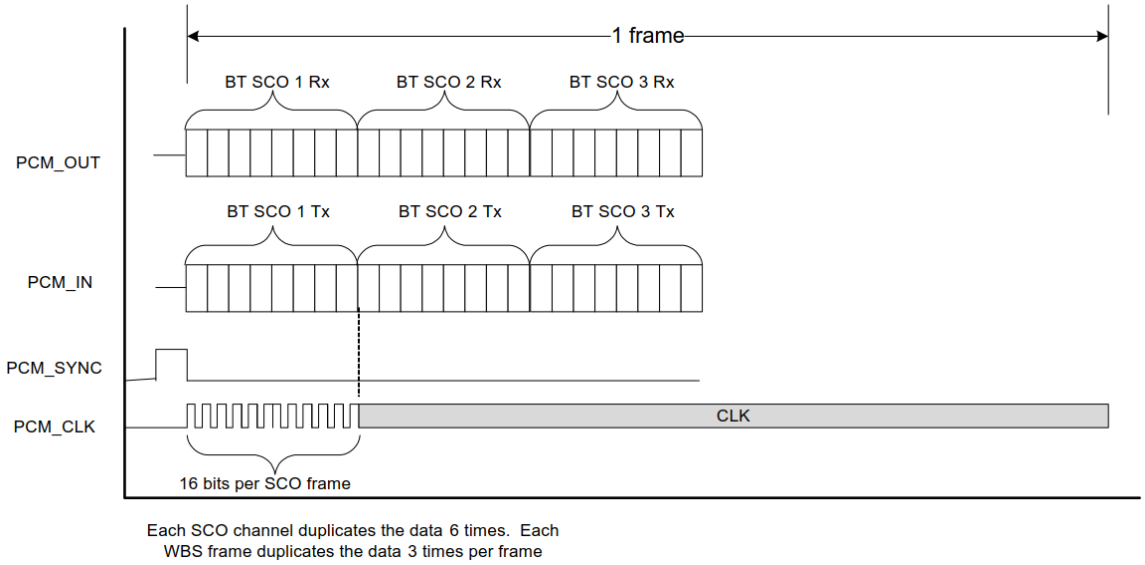


Figure 7: Functional Multiples Data diagram

8.3.6 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

Figure 8 and Table 15 shows PCM Burst mode timing diagram and specifications for the receive-only mode of short-frame sync.

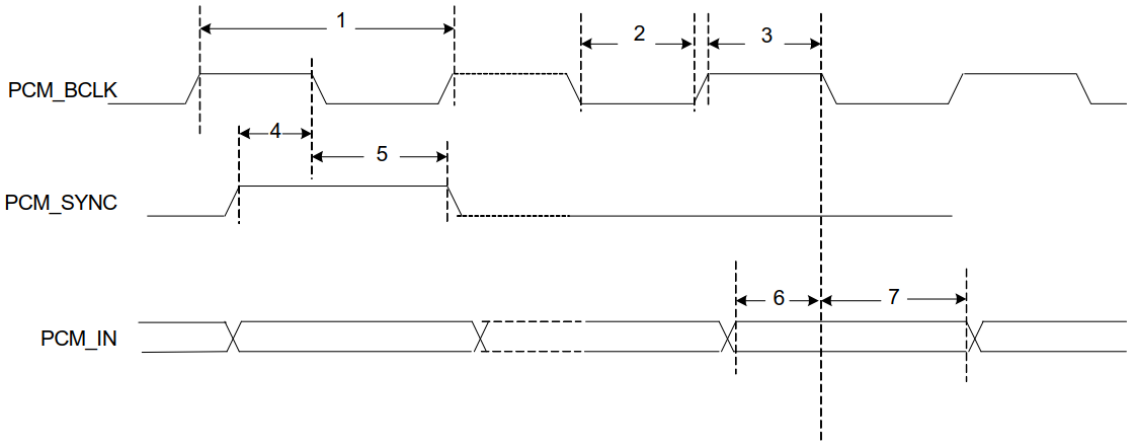


Figure 8: PCM Burst Mode timing (Receive Only, Short Frame Sync)

Table 15: PCM Burst Mode Specifications (Receive Only, Short-Frame Sync)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC_hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

Figure 9 and Table 16 shows PCM Burst mode timing diagram and specifications for the receive-only mode of long-frame sync.

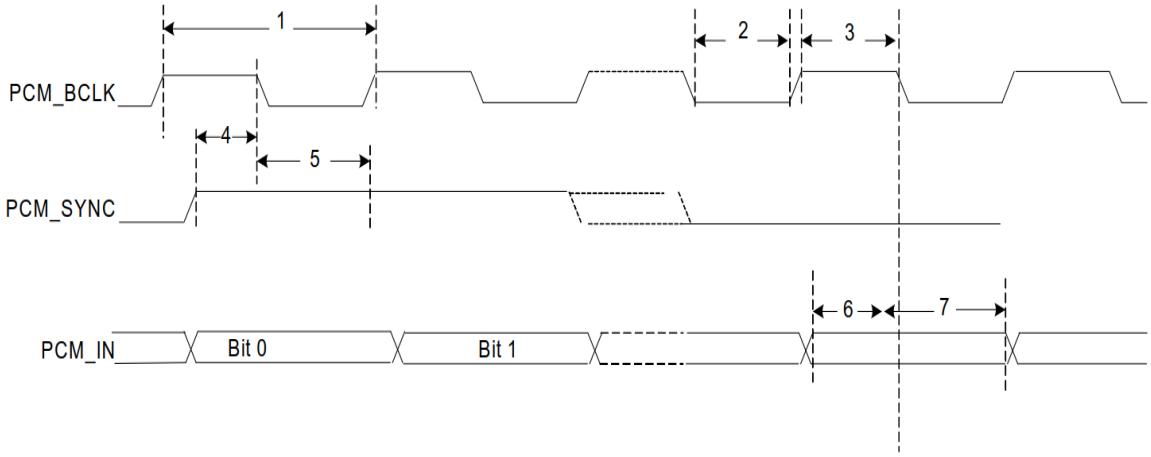


Figure 9: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Table 16: PCM Burst Mode Specifications (Receive Only, Long-Frame Sync)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC_hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

8.4 I²S Interface

The BT860-Sx supports two independent I²S digital audio ports. The I²S interface supports both master and slave modes. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the BT860 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

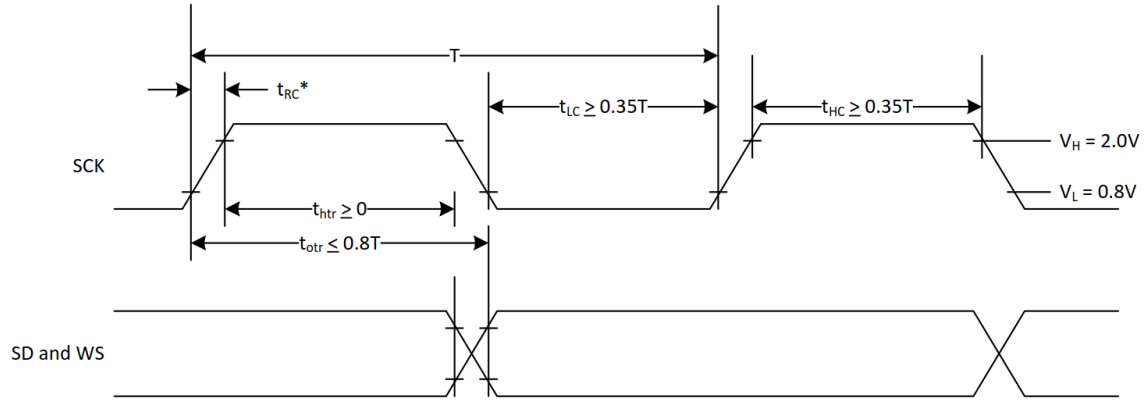
8.4.1 I²S Timing

Timing values specified in Table 17 are relative to high and low threshold levels.

Table 17: Timing for I2S Transmitters and Receivers

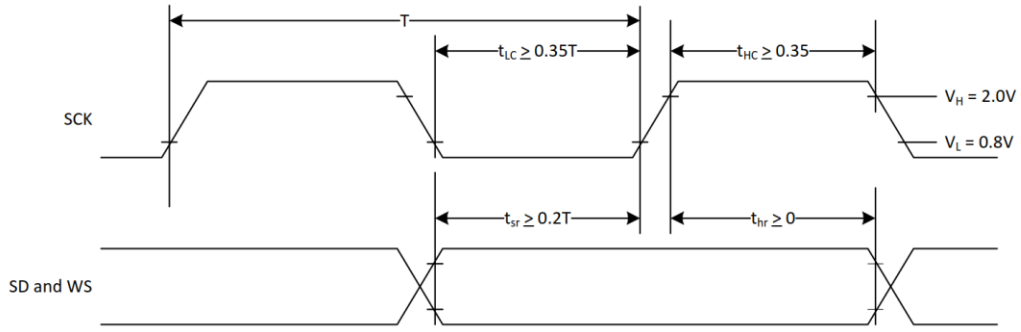
	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	-	-	-	T_r	-	-	-	
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	-	
LOW t_{LC}	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	-	
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	-	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	
LOW t_{LC}	-	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	
Rise time t_{RC}	-	-	$0.15T_{tr}$	-	-	-	-	-	
Transmitter									
Delay t_{dtr}	-	-	-	0.8T	-	-	-	-	
Hold time t_{htr}	0	-	-	-	-	-	-	-	
Receiver									
Setup time t_{sr}	-	-	-	-	-	$0.2T_r$	-	-	
Hold time t_{hr}	-	-	-	-	-	0	-	-	

The time periods specified in Figure 10 and Figure 11 are defined by the transmitter speed. The receiver specifications must match transmitter performance.



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 10: I²S Transmitter timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Figure 11: I²S Receiver Timing

8.5 Reset and POR (Power on Reset)

A power on reset (POR) timing requirement is shown in Figure 12.

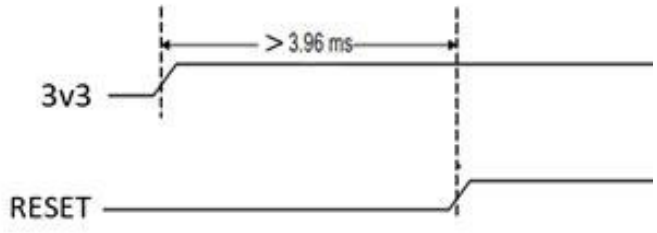


Figure 12: Power on reset (POR) timing

When the system requires a reset, you must hold the rest line in low state for longer than 3.96 milliseconds to complete the reset cycle.

WARNING

Asserting reset while the CYW20704 bootloader reads EEPROM contents during its initialization sequence can cause EEPROM corruption. Ensure that reset is not asserted for a minimum of 1.6 seconds after it has been de-asserted to ensure the CYW20704 has completed transferring FW into its local storage.

An improper low state on the reset line (such as a voltage glitch) causes a system error due to a crash on the EEPROM content.

A bypass cap such as 0.1uF placed on the reset line overcomes the issue caused by the glitch.

9 Antenna Performance

Table 18, Figure 13, Figure 14, and Figure 15 show the antenna gain and performance.

Table 18: Antenna gain

Unit in dBi @ 2440MHz	XY-Plane		XZ-Plane		YZ-Plane		Efficiency
AT3216-B2R7HAA	Peak	Avg.	Peak	Avg.	Peak	Avg.	
	0.1	-4.1	1.8	-3.3	-0.2	-6.8	41%

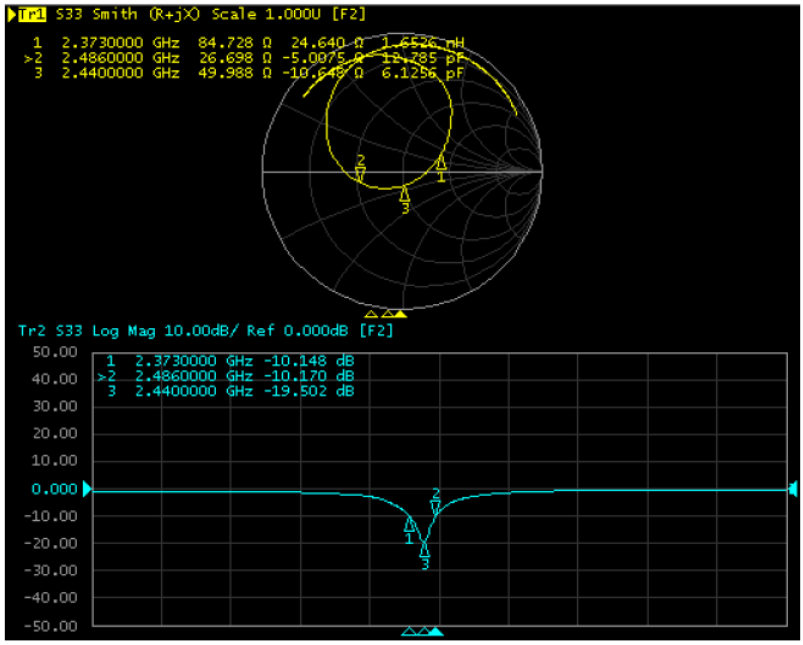


Figure 13: Antenna Return Loss

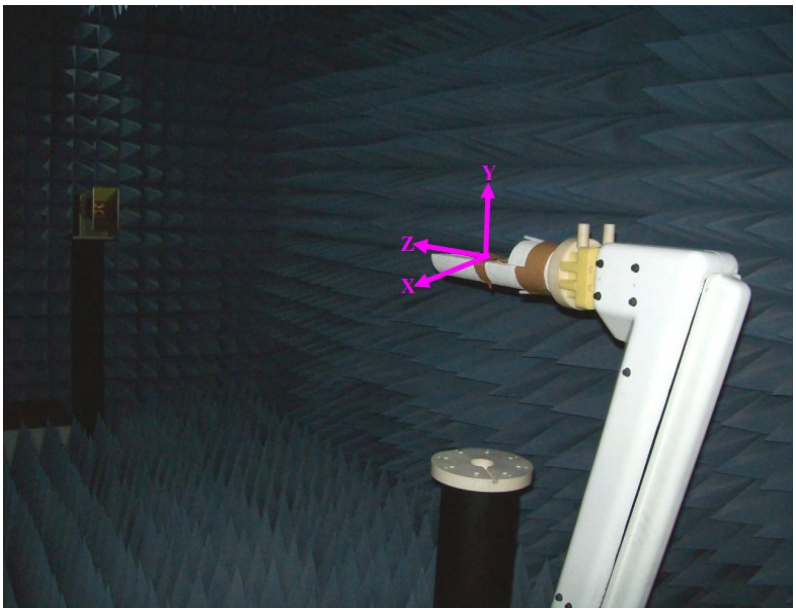
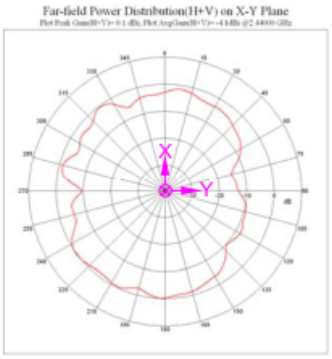


Figure 14: Measurement XYZ polarization

Table 19: Plane definitions

XY-Plane	Theta = 90°
XZ-Plane	Phi = 0°
YZ-Plane	Phi = 90°

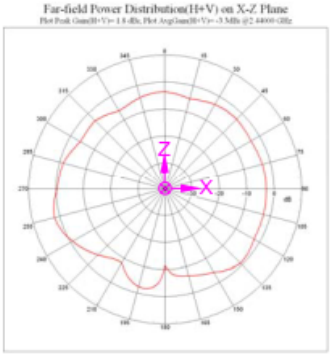
◆XY-plane



Unit : dBi

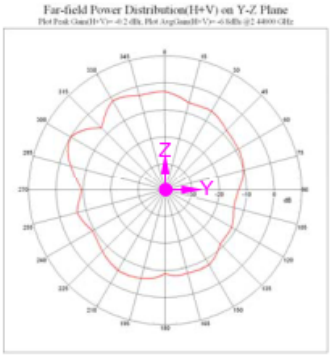
	Peak gain	Avg. gain
XY-plane	0.1	-4.1

◆XZ-plane



	Peak gain	Avg. gain
XZ-plane	1.8	-3.3

◆YZ-plane



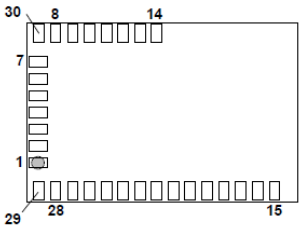
	Peak gain	Avg. gain
YZ-plane	-0.2	-6.8

Figure 15: Antenna pattern

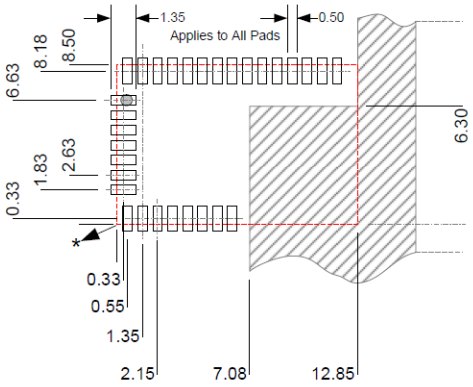
10 Mechanical Dimensions and Land Pattern

10.1 BT860 Mechanical Drawing

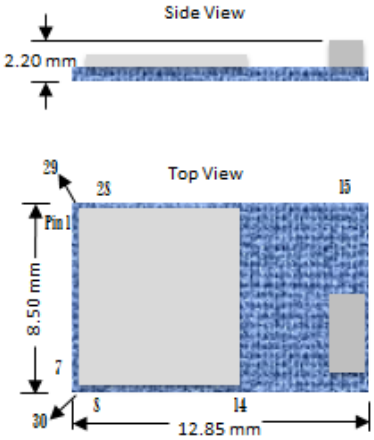
Bottom View Device Pads



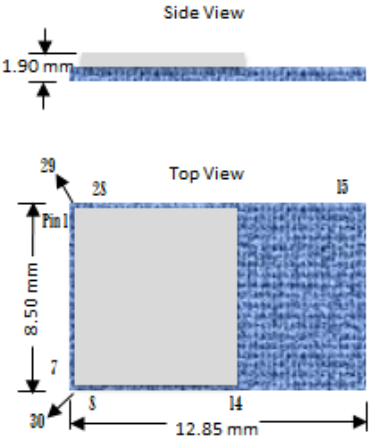
Top View
Recommended PCB Layout



SA Type



ST Type



* Dimensions from corner of BT860

Pin1

No Copper in this area!

Note: Dimensions are in millimetres.
Tolerances: .xx ±0.03 mm for PCB PAD; ±0.15 mm for module size
.x ±1.3 mm

11 Implementation Note

11.1 PCB Layout on Host PCB

Checklist (for PCB):

- **MUST** locate the BT860 module close to the edge of PCB.
- Use solid GND plane on inner layer (for best EMC and RF performance).
- Place GND vias close to module GND pads as possible
- Route traces to avoid noise being picked up on VCC supply.
- Antenna Keep-out area:
  - Ensure there is no copper in the antenna keep-out area on any layers of the host PCB.
  - Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
  - For best antenna performance, place the BT860 module on the edge of the host PCB, preferably in the corner with the antenna facing the corner.
  - A different host PCB thickness dielectric will have small effect on antenna.

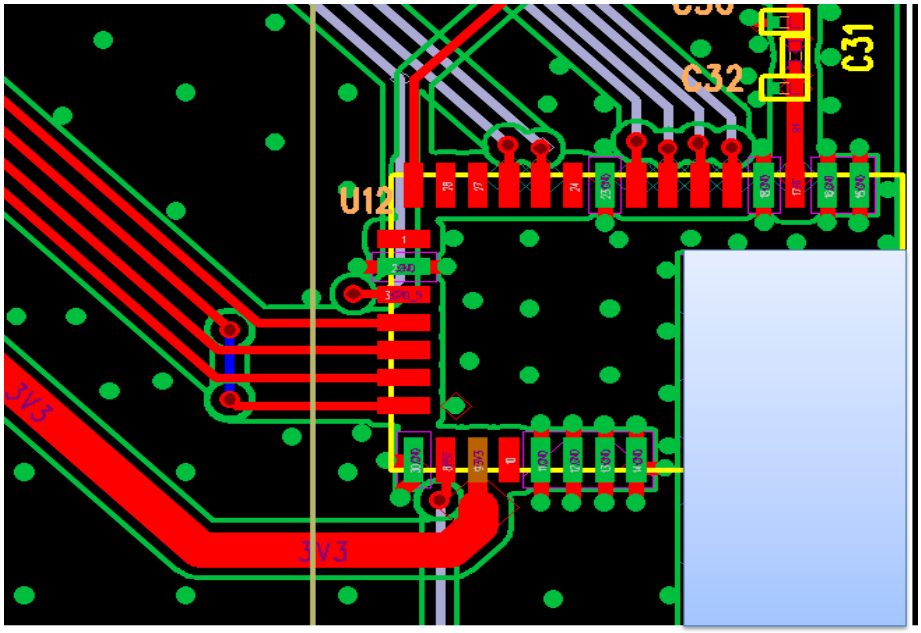


Figure 16: Recommend Antenna keep-out area (in Blue) used on the BT860

11.1.1 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the BT860-SA chip monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of degradation is entirely system dependent which means some testing by customers is required (in their host application).
- Any metal closer than 20 mm starts to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that the customer tests the range with mock-up (or actual prototype) of the product to assess effects of enclosure height (and material whether metal or plastic).

12 Application Note for Surface Mount Modules

12.1 Introduction

Ezurio surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and is updated as new information is presented.

The modules are designed to meet the needs of a number of commercial and industrial applications. They are easy to manufacture and they conform to current automated manufacturing processes.

12.2 Shipping

12.2.1 Tape and Reel Package Information

Note: Ordering information for Tape and Reel packaging is an addition of T/R to the end of the full module part number. For example, BT860 becomes BT860-Sx-xx-T/R.

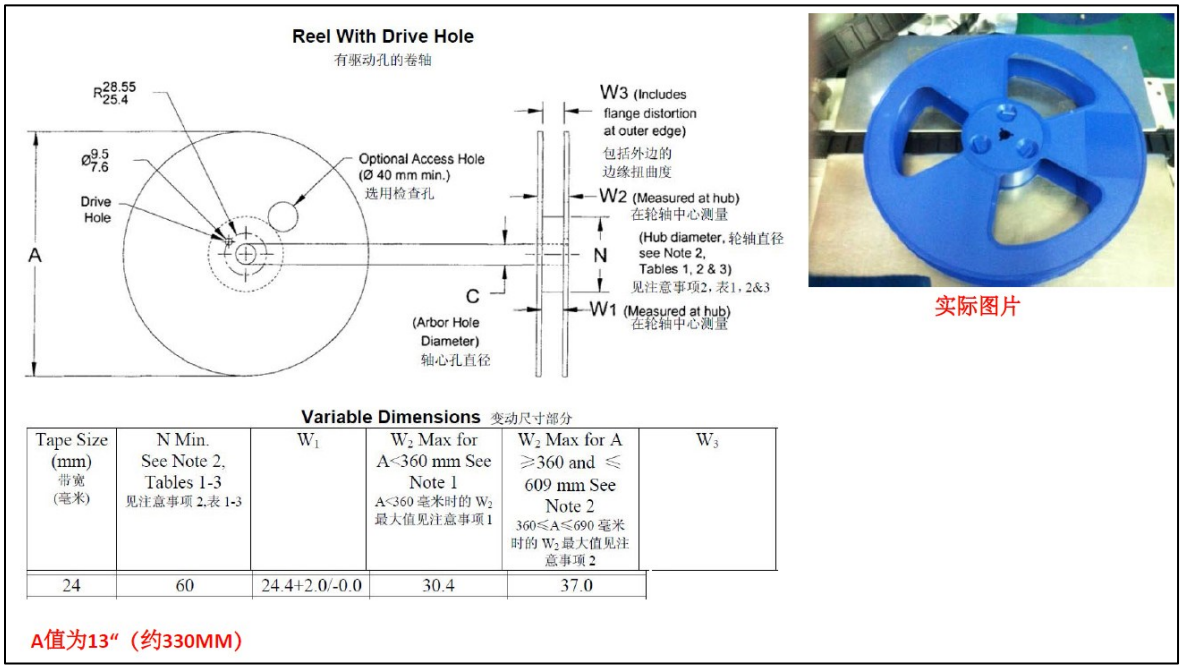


Figure 17: Reel specifications

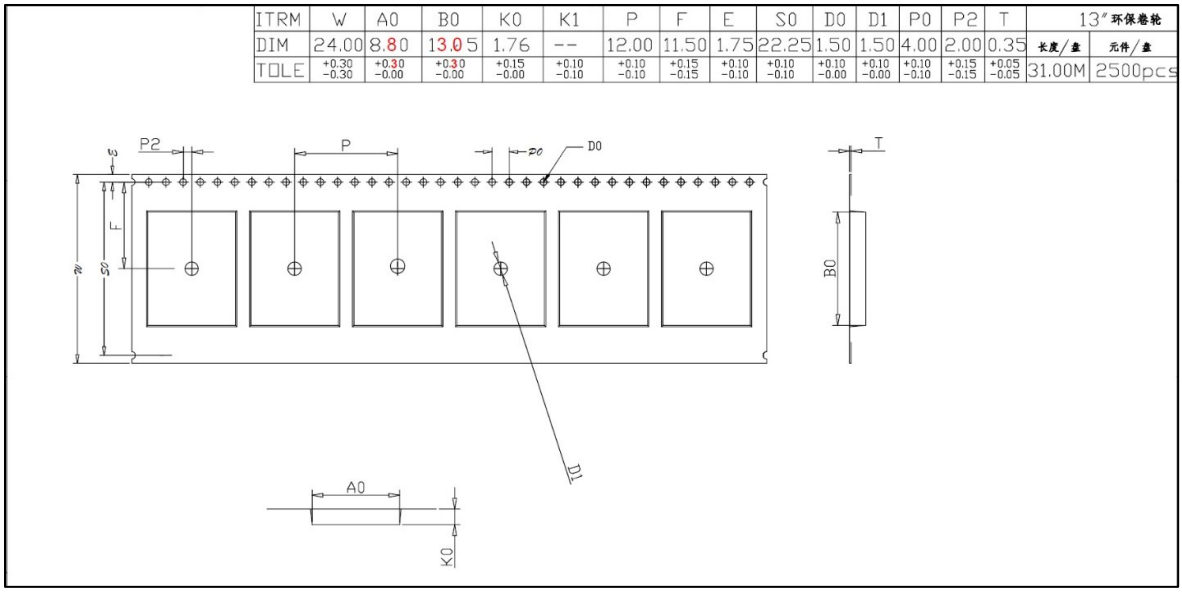


Figure 18: Tape specifications

There are 2500 x BT860-Sx modules taped in a reel (and packaged in a pizza box) and five boxes per carton (12,500 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels. See Figure 19.

12.2.2 Packaging Process

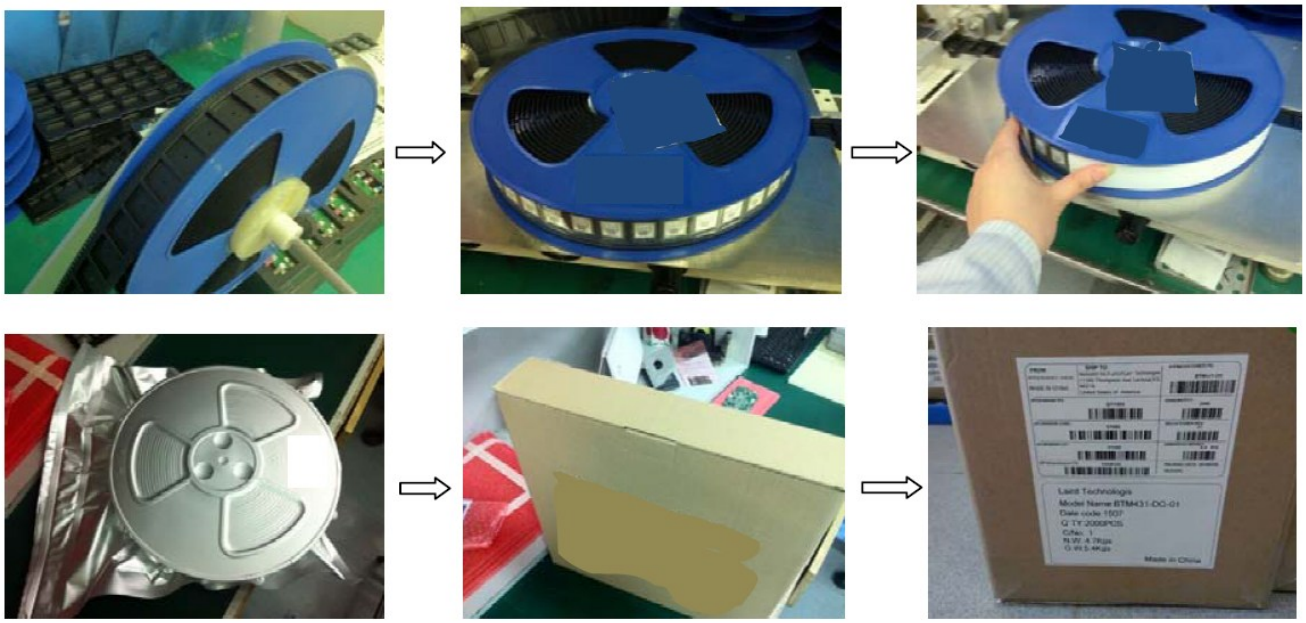


Figure 19: BT860 packaging process

12.3 Reflow Parameters

Ezurio surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Ezurio's surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds. In addition, we strongly recommend that you do not put the module through reflow more than once. Otherwise, it impacts the module's soldering.

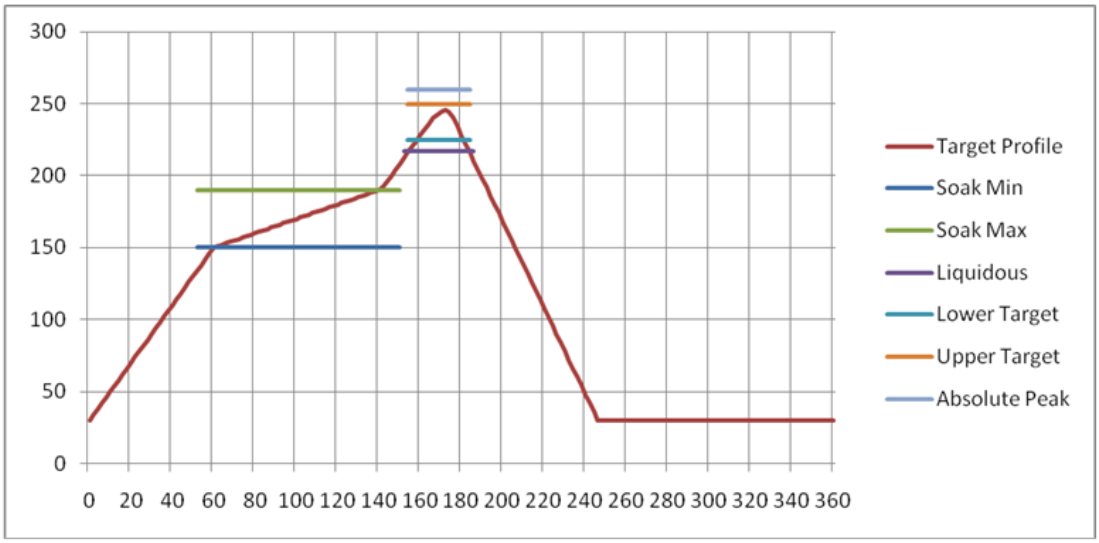


Figure 20: Recommended reflow temperature

Temperatures should not exceed the minimums or maximums presented in Table 202.

Table 202: Recommended maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

13 Regulatory

Regulatory information about the BT860 is found in the BT850/BT851/BT860 Regulatory Information Guide.

14 Ordering Information

Part Number	Description
BT860-SA	BTv5.0 Dual Mode UART HCI Module with integrated Antenna
BT860-ST	BTv5.0 Dual Mode UART HCI Module – Trace Pin
DVK-BT860-SA	Development Kit for BT860-SA Module (Integrated Antenna)
DVK-BT860-ST	Development Kit for BT860-ST Module (Ex. Antenna – Trace Pad)

15 Bluetooth SIG Approvals

15.1 Overview

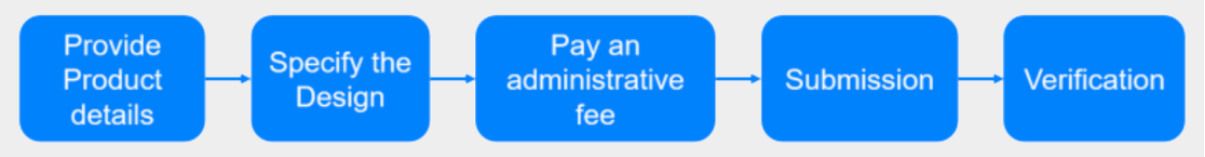
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

15.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

15.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number

- Product Publication Date (the product publication date may not be later than 90 days after submission)
- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
   - Select 'I'm finished entering DN's
   - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
   - What do you want to do next? Answer, 'Combine unmodified Designs'.
   - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
   - An active TCRL will be selected for the design.
   - Perform the Consistency Check, which should result in no inconsistencies
   - If there are any inconsistencies these will need to be resolved before proceeding
   - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
   a. As no modifications have been made to the combined designs the tool should report the following message:
   'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
   b. Save and go to Product Qualification fee
6. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

15.4 Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + BlueZ 5.50 Host Stack (Ezurio BT850/BT860 based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
BT850/BT860	Ezurio	D053988	164479	https://qualification.bluetooth.com/ListingDetails/124936
BlueZ 5.50 Host Stack	Ezurio	D046330	138224	https://qualification.bluetooth.com/ListingDetails/93911

15.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

16 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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