

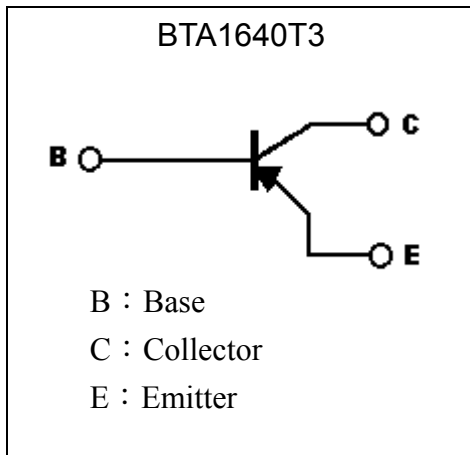
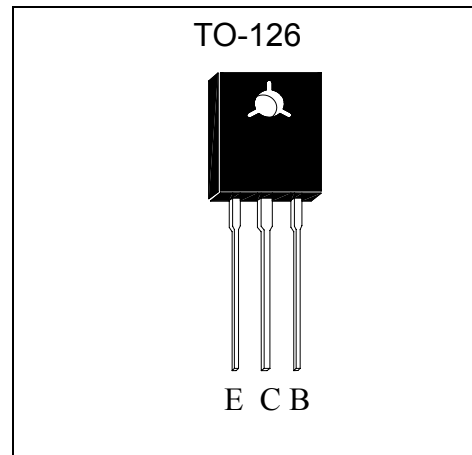
PNP Epitaxial Planar Power Transistor

BTA1640T3

BV_{CEO}	-50V
I_C	-7A
R_{CESAT}	70m Ω (typ.)

Features

- Low collector-emitter saturation voltage, $V_{CE(sat)} = -0.4V(max)$ @ $I_C = -3A$, $I_B = -0.1A$.
- Excellent current gain linearity.
- RoHS compliant package.

Symbol

Outline

Absolute Maximum Ratings ($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-60	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Emitter-Base Voltage	V_{EBO}	-18	V
Collector Current (DC)	I_C	-7	A
Collector Current (Pulse)	I_{CP}	-10 (Note 1)	
Power Dissipation @ $T_A = 25^\circ C$	P_D	1	W
Power Dissipation @ $T_C = 25^\circ C$	P_D	20	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^\circ C/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	$^\circ C/W$
Junction Temperature	T_j	150	$^\circ C$
Storage Temperature	T_{stg}	-55~+150	$^\circ C$

Note : 1. Single Pulse , $P_w \leq 380\mu s$, Duty $\leq 2\%$.

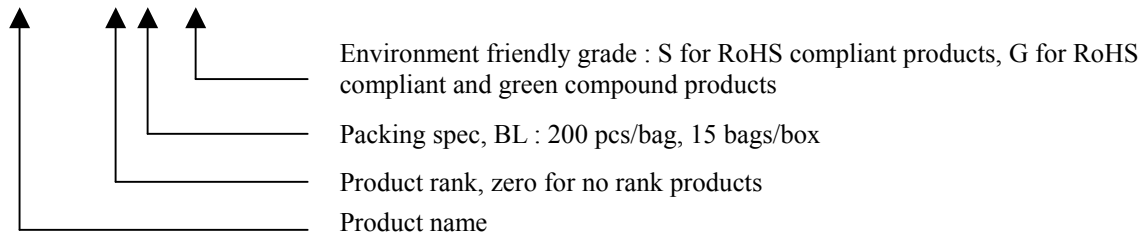
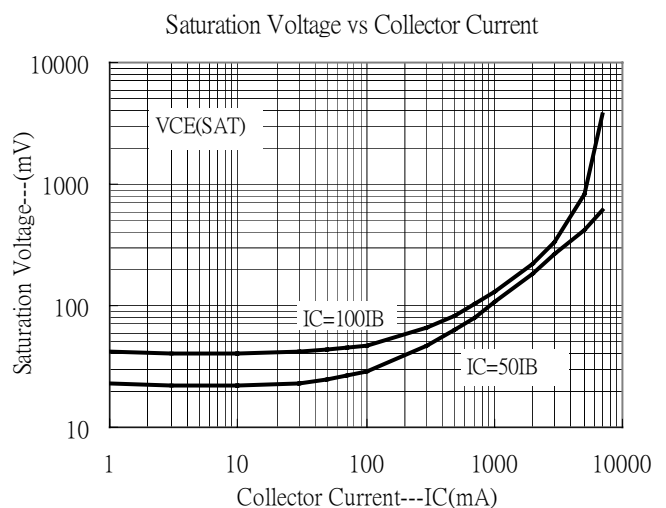
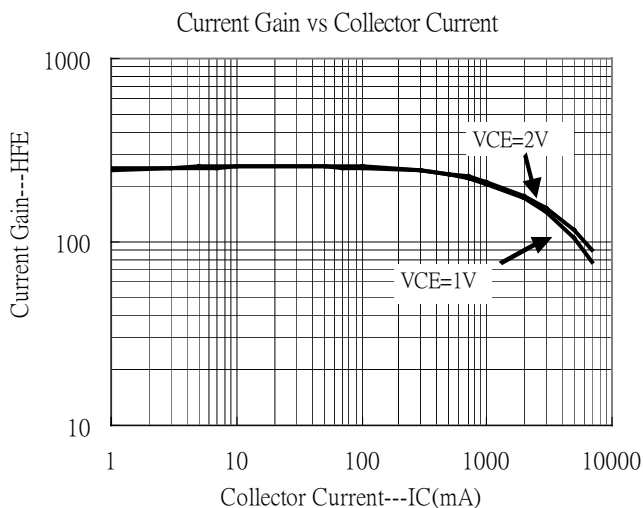
**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
*BV _{CEO}	-50	-	-	V	I _C =-10mA, I _B =0
BV _{CBO}	-60	-	-	V	I _C =-1mA, I _E =0
BV _{EBO}	-18	-	-	V	I _E =-1mA, I _C =0
I _{CEO}	-	-	-10	μA	V _{CE} =-40V, I _B =0
I _{CBO}	-	-	-100	nA	V _{CB} =-60V, I _B =0
I _{EBO}	-	-	-100	nA	V _{EB} =-15V, I _C =0
*V _{CE(sat)}	-	-0.2	-0.4	V	I _C =-3A, I _B =-100mA
*V _{CE(sat)}	-	-0.42	-0.7	V	I _C =-5A, I _B =-100mA
*V _{BE(sat)}	-	-	-1.2	V	I _C =-3A, I _B =-100mA
*h _{FE} 1	200	-	450	-	V _{CE} =-2V, I _C =-500mA
*h _{FE} 2	60	-	-	-	V _{CE} =-2V, I _C =-4A

*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

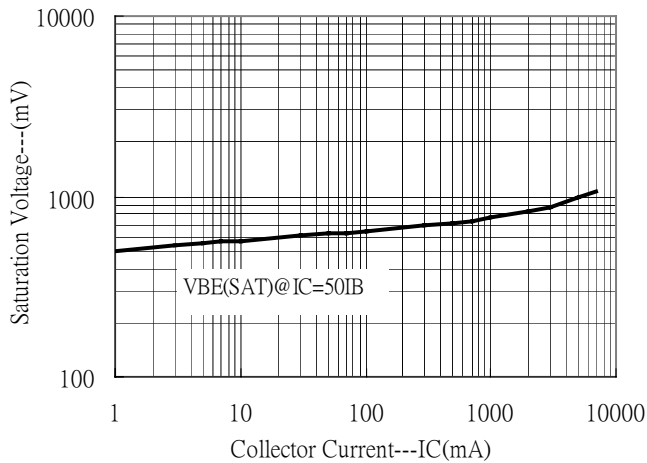
Ordering Information

Device	Package	Shipping
BTA1640T3-0-BL-G	TO-126 (Pb-free lead plating package)	200 pcs / bag, 15 bags/box

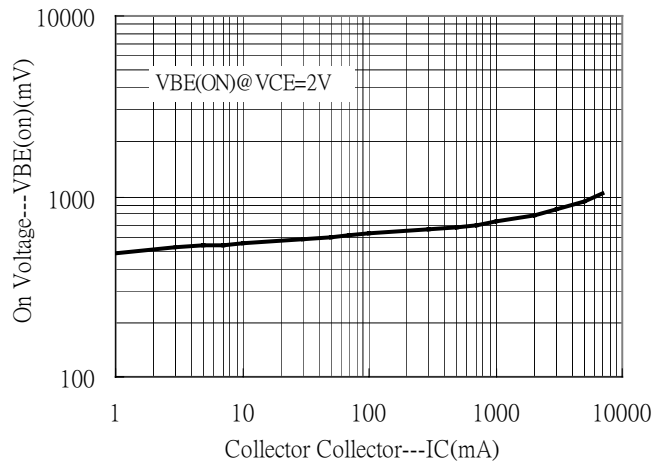
**Typical Characteristics**

Typical Characteristics(Cont.)

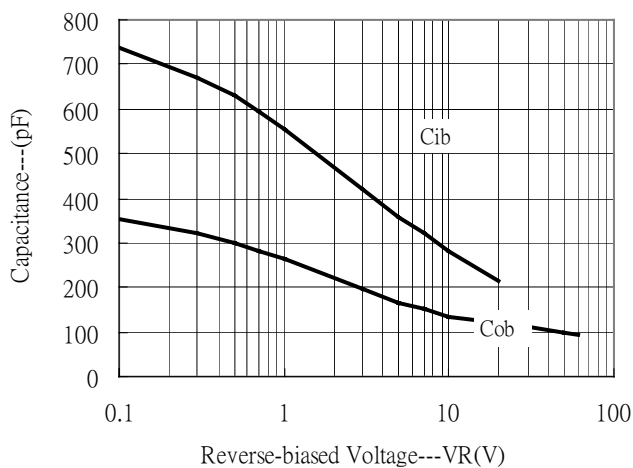
Saturation Voltage vs Collector Current



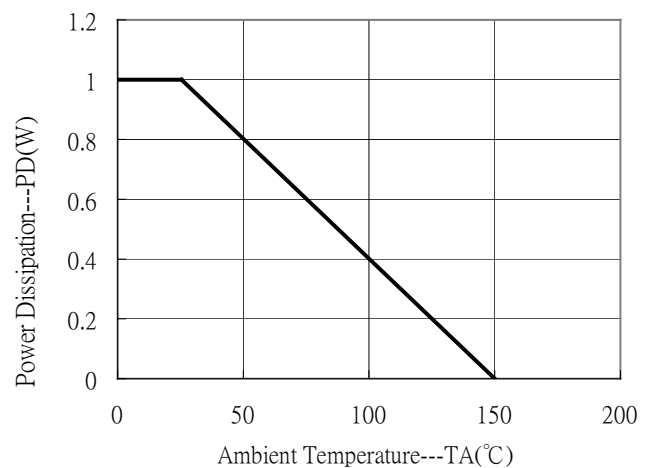
On Voltage vs Collector Current



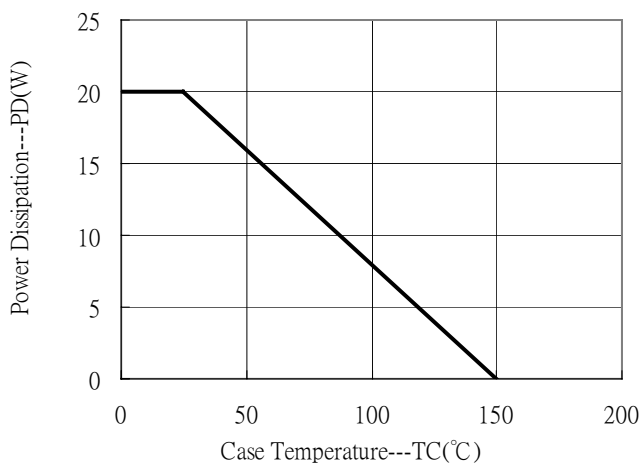
Typical Capacitance Characteristics



Power Derating Curve



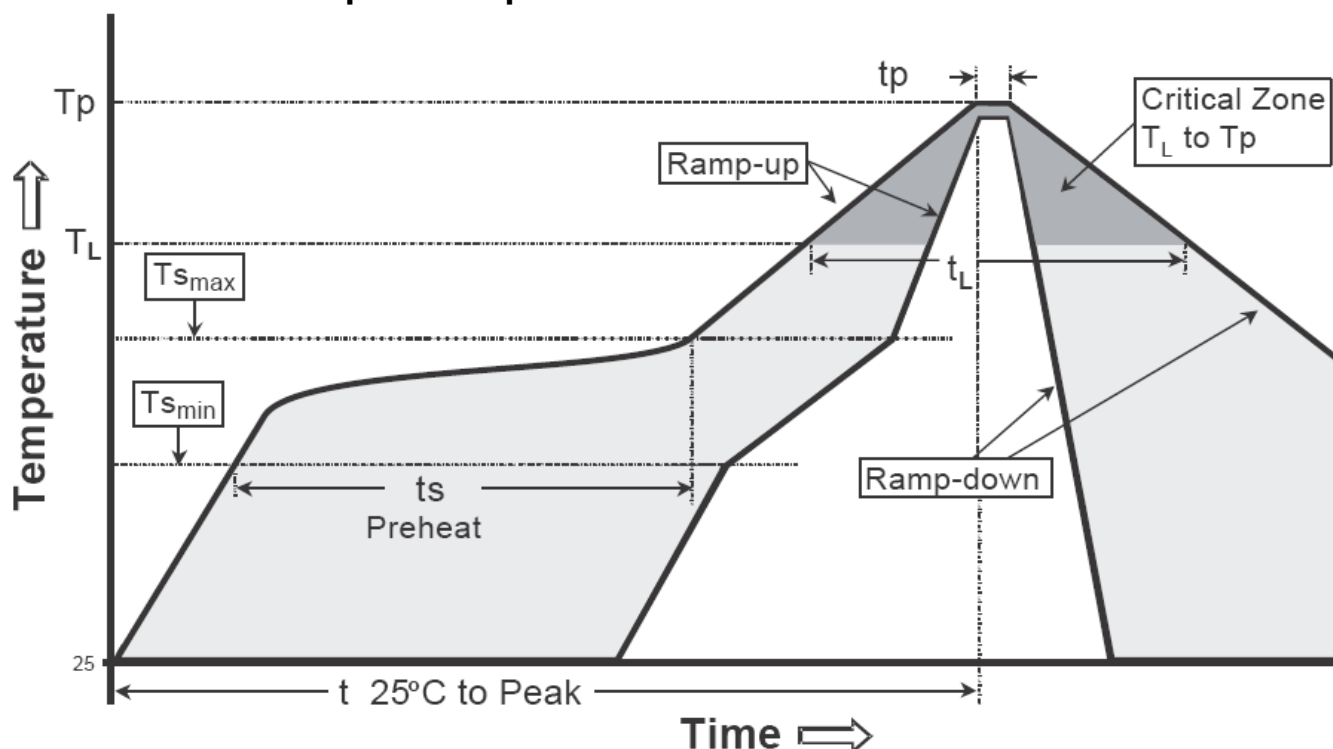
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

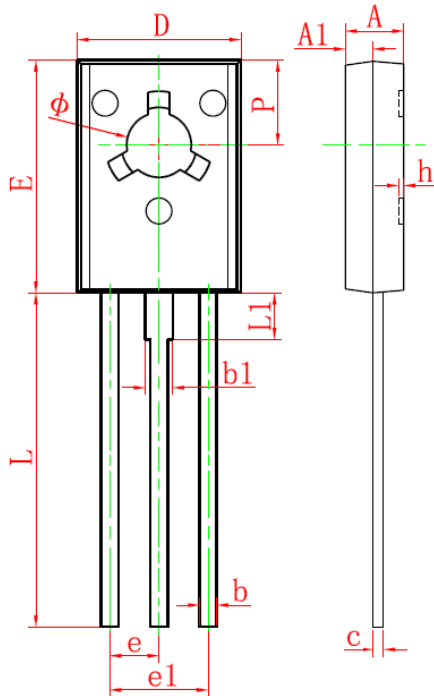
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

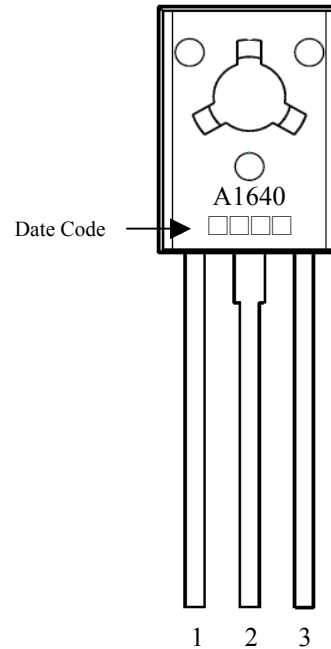
Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126 Dimension



3-Lead TO-126 Plastic Package
 CYStek Package Code: T3

Marking:



Style: Pin 1.Emitter 2.Collector 3.Base

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	Φ	3.000	3.200	0.118	0.126

Notes: 1.Controlling dimension: millimeters.

2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.

3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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