

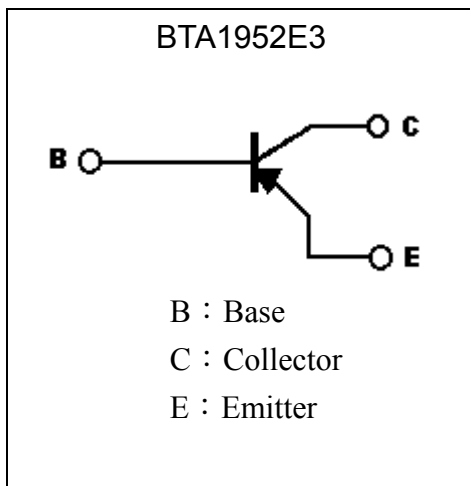
Low Vcesat PNP Epitaxial Planar Transistor

BTA1952E3

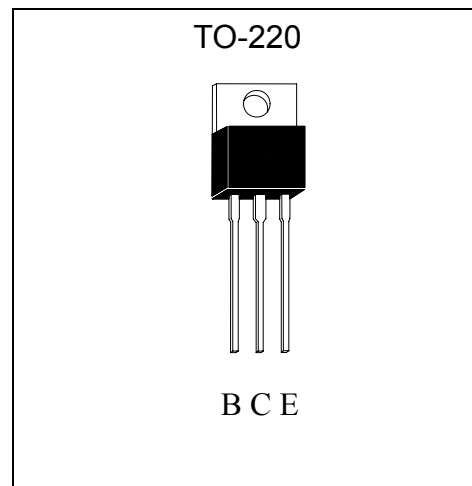
Features

- Low $V_{CE(sat)}$, $V_{CE(sat)} = -0.23$ V (typical), at $I_C / I_B = -3A / -0.15A$
- Excellent DC current gain characteristics
- Wide SOA
- Pb-free lead plating package

Symbol

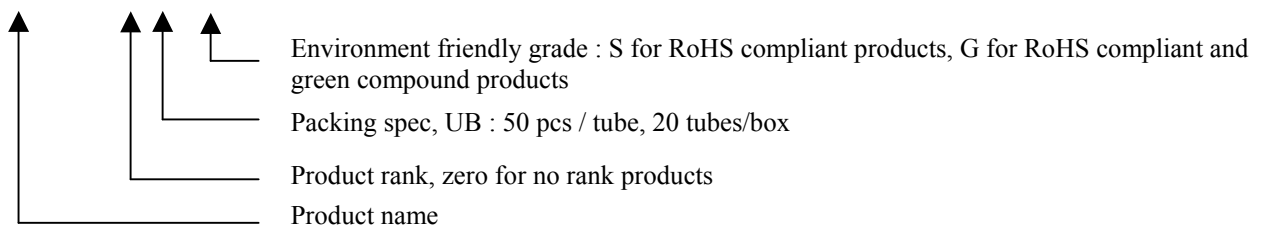


Outline



Ordering Information

Device	Package	Shipping
BTA1952E3-X-UB-X	TO-220 (Pb-free lead plating)	50 pcs / tube, 20 tubes/ box , 4 boxes/carton



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CB0}	-100	V
Collector-Emitter Voltage	V _{CEO}	-70	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current	I _C (DC)	-5	A
	I _C (Pulse)	-8 *1	
Base Current	I _B	-1	A
Power Dissipation	P _d (T _A =25°C)	2	W
	P _d (T _C =25°C)	40	
Operating Junction Temperature Range	T _j	-55~+150	°C
Storage Temperature Range	T _{stg}	-55~+150	°C

Note : *1. Single Pulse Pw=10ms

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient	R _{θJA}	62.5	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	3.1	

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CEO}	-70	-	-	V	I _C =-10mA, I _B =0
I _{CB0}	-	-	-100	nA	V _{CB} =-100V, I _E =0
I _{EBO}	-	-	-100	nA	V _{EB} =-5V, I _C =0
*V _{CE(sat)}	-	-145	-300	mV	I _C =-1A, I _B =-10mA
*V _{CE(sat)}	-	-230	-500	mV	I _C =-3A, I _B =-150mA
*V _{CE(sat)}	-	-300	-600	mV	I _C =-4A, I _B =-200mA
*V _{BE(sat)}	-	-0.93	-1.2	V	I _C =-3A, I _B =-150mA
*h _{FE 1}	100	-	-	-	V _{CE} =-3V, I _C =-500mA
*h _{FE 2}	120	-	390	-	V _{CE} =-2V, I _C =-1A
f _T	-	130	-	MHz	V _{CE} =-10V, I _C =-100mA, f=1MHz
Cob	-	80	-	pF	V _{CB} =-10V, f=1MHz

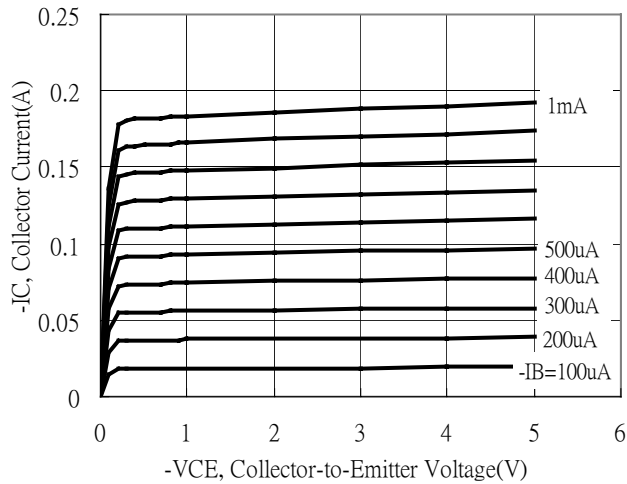
*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Classification of h_{FE 2}

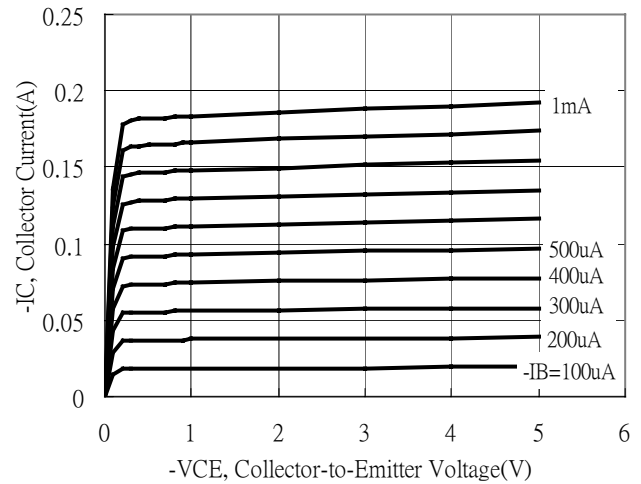
Rank	Q	R
Range	120~270	180~390

Typical Characteristics

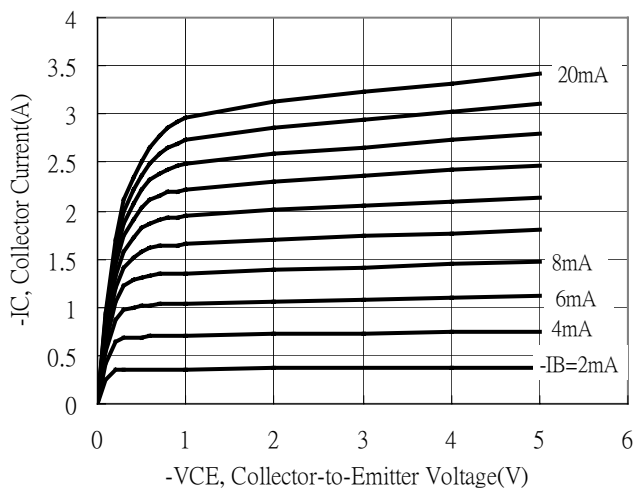
Emitter Grounded Output Characteristics



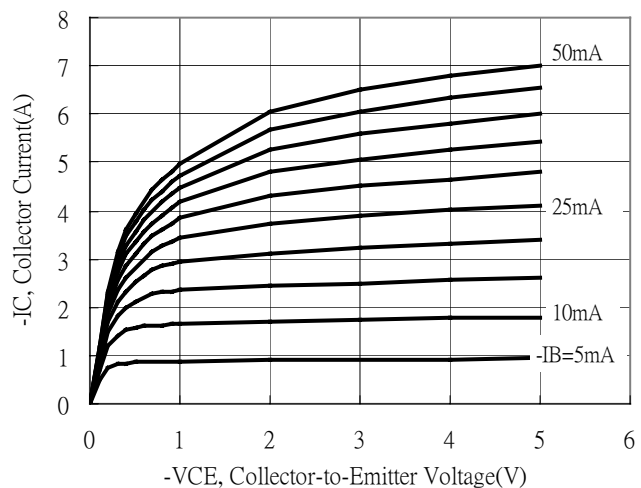
Emitter Grounded Output Characteristics



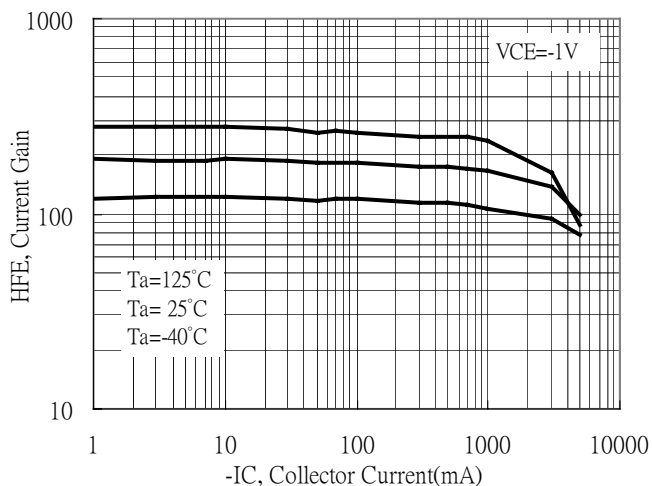
Emitter Grounded Output Characteristics



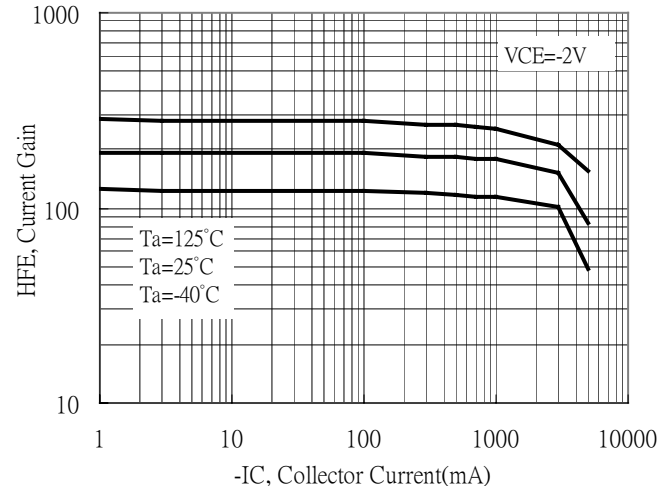
Emitter Grounded Output Characteristics



Current Gain vs Collector Current

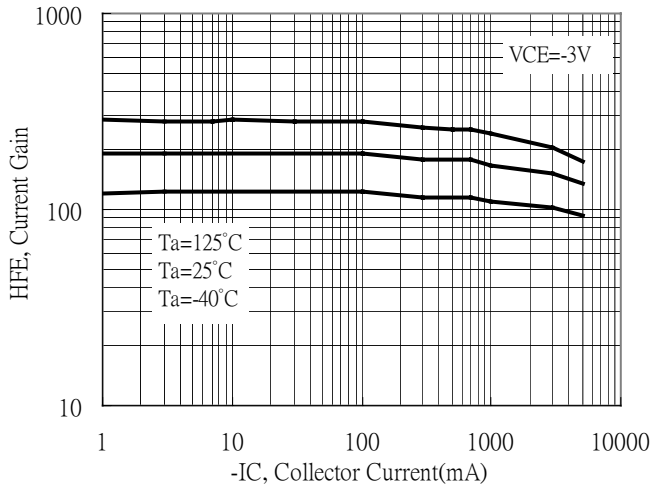


Current Gain vs Collector Current

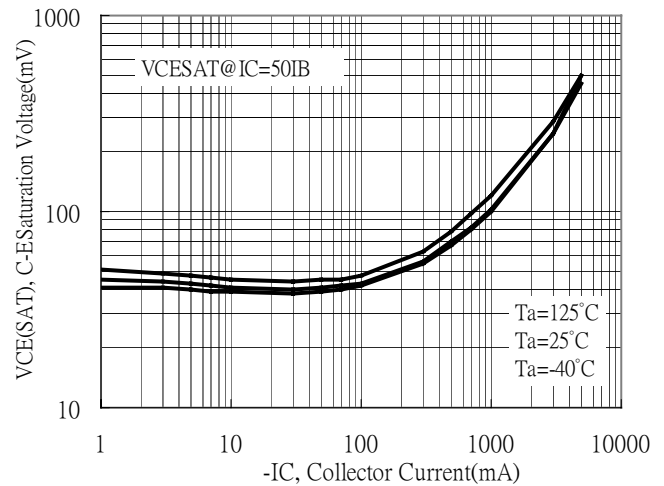


Typical Characteristics(Cont.)

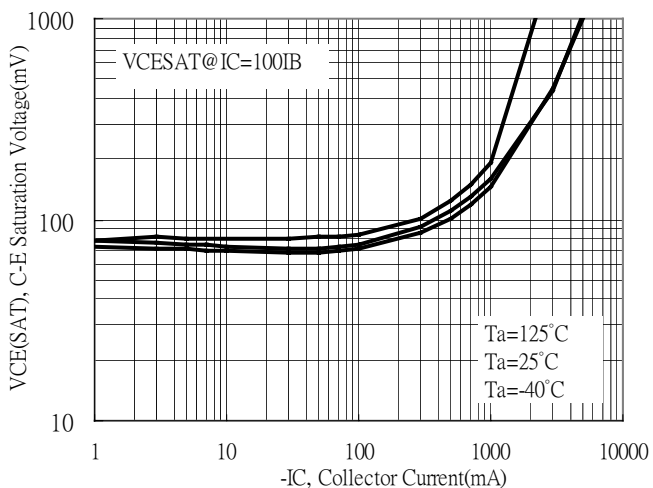
Current Gain vs Collector Current



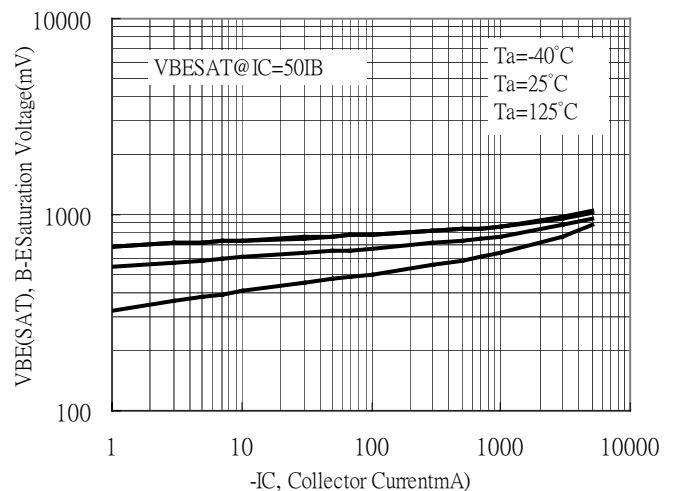
Saturation Voltage vs Collector Current



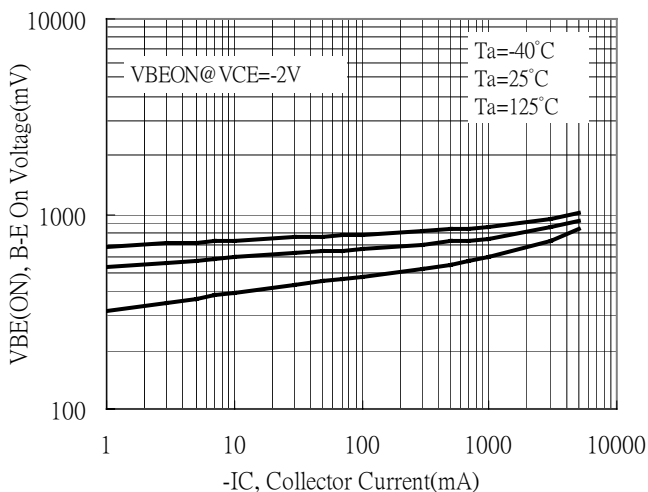
Saturation Voltage vs Collector Current



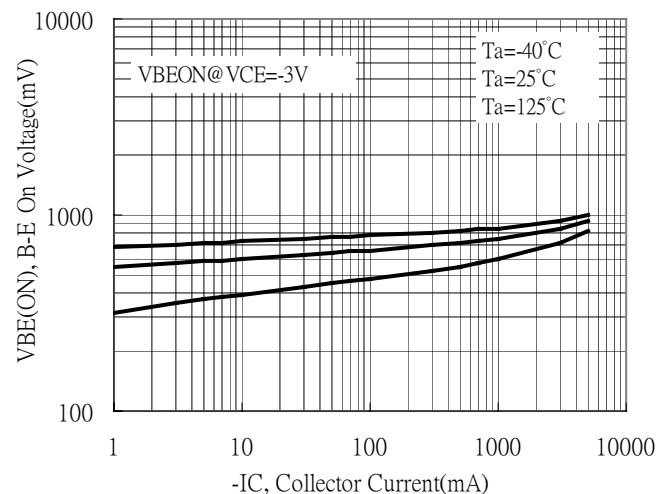
Saturation Voltage vs Collector Current



On Voltage vs Collector Current



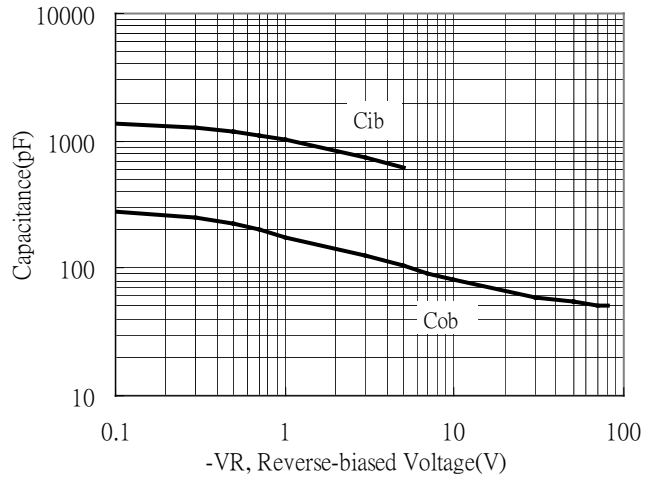
On Voltage vs Collector Current



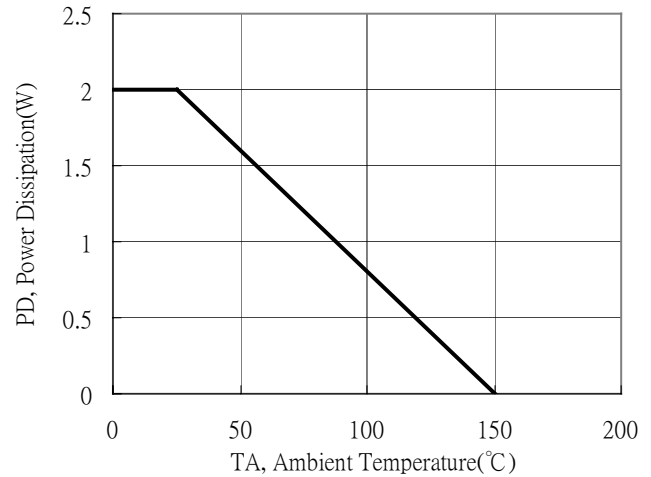


Typical Characteristics(Cont.)

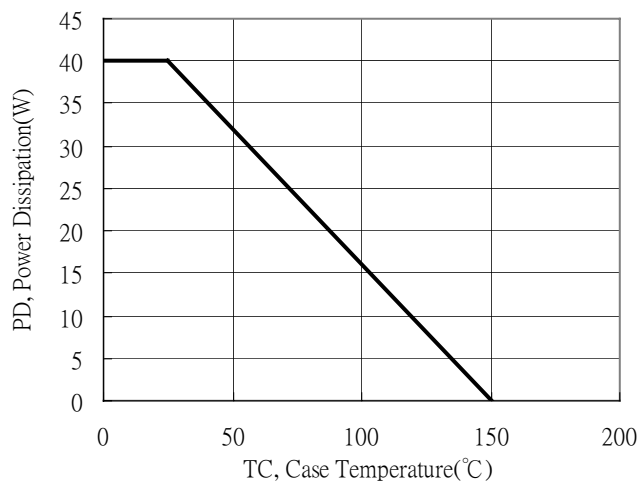
Capacitance vs Reverse-biased Voltage



Power Derating Curve



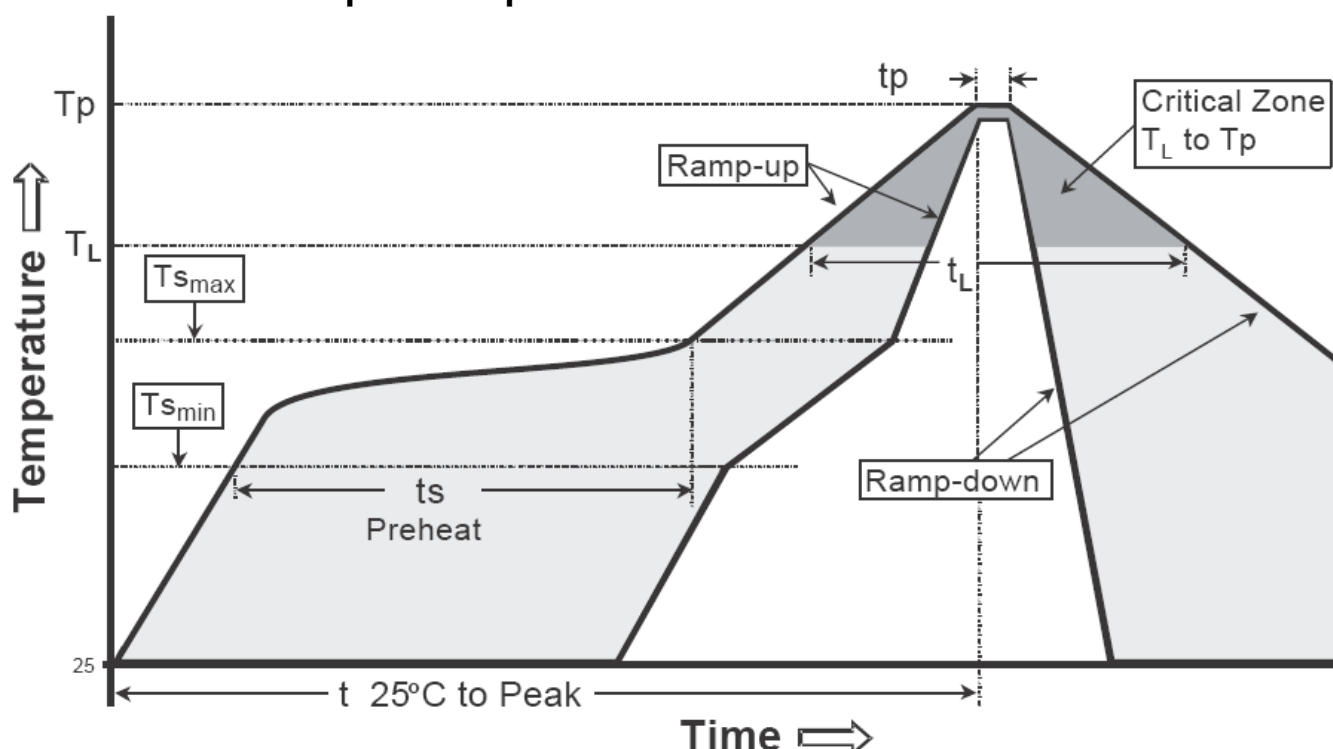
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

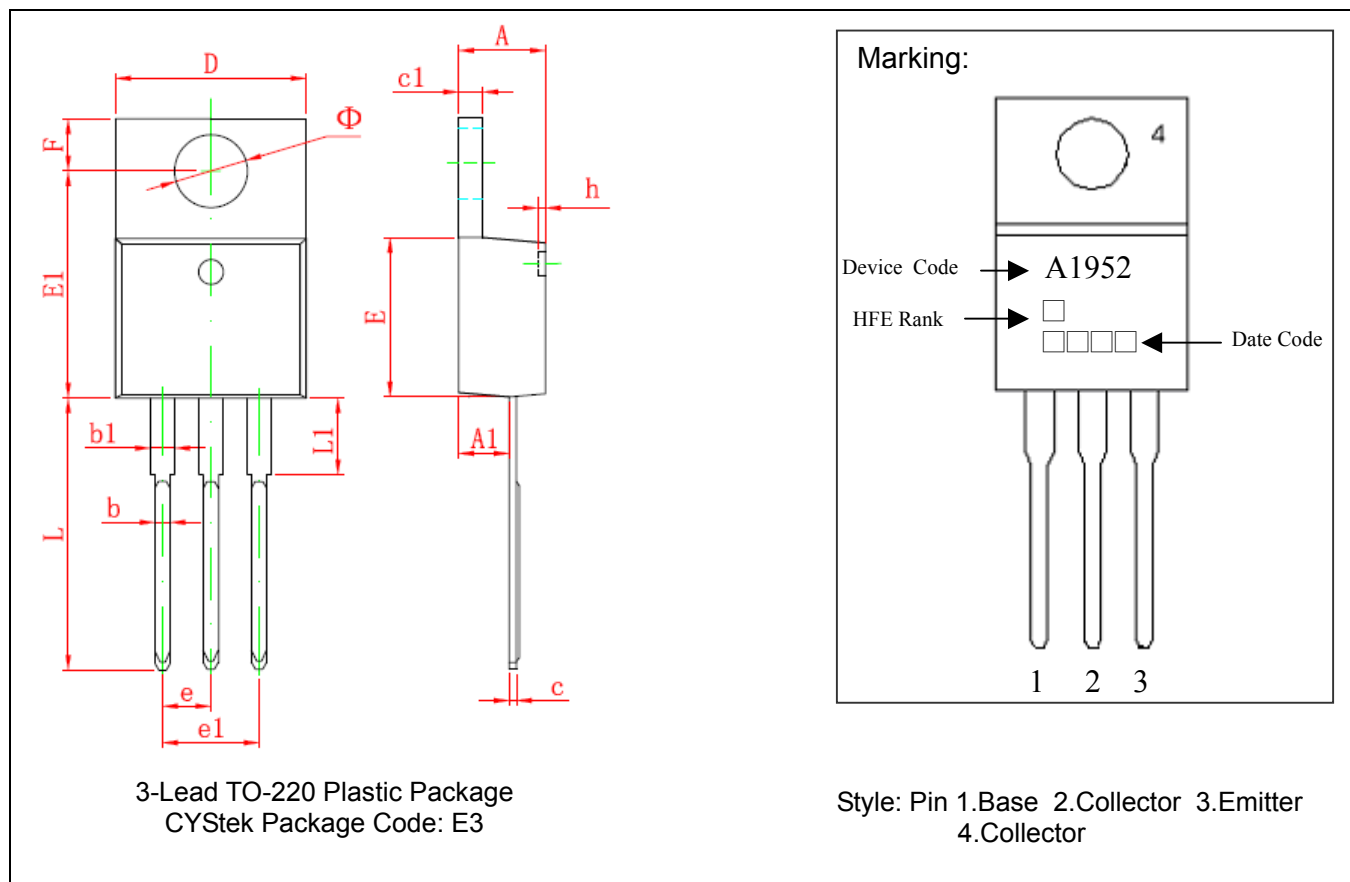
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220 Dimension



*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184	E1	12.060	12.460	0.475	0.491
A1	2.520	2.820	0.099	0.111	e	2.540*		0.100*	
b	0.710	0.910	0.028	0.036	e1	4.980	5.180	0.196	0.204
b1	1.170	1.370	0.046	0.054	F	2.590	2.890	0.102	0.114
c	0.310	0.530	0.012	0.021	h	0.000	0.300	0.000	0.012
c1	1.170	1.370	0.046	0.054	L	13.400	13.800	0.528	0.543
D	10.010	10.310	0.394	0.406	L1	3.560	3.960	0.140	0.156
E	8.500	8.900	0.335	0.350	Φ	3.735	3.935	0.147	0.155

Notes: 1.Controlling dimension: millimeters.

2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.

3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.