Triacs high commutation

BTA216B series B

GENERAL DESCRIPTION

Glass passivated high commutation triacs in a plastic envelope suitable for surface mounting, intended for use in circuits where high static and dynamic dV/dt and high dl/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

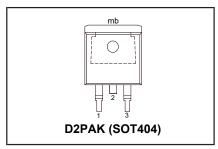
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
V _{DRM} I _{T(RMS)} I _{TSM}	BTA216B- Repetitive peak off-state voltages RMS on-state current Non-repetitive peak on-state current	500B 500 16 140	600B 600 16 140	800B 800 16 140	V A A

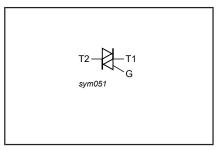
PINNING - SOT404

PIN	DESCRIPTION		
1	main terminal 1		
2	main terminal 2		
3	gate		
mb	main terminal 2		

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.		UNIT
V_{DRM}	Repetitive peak off-state voltages		-	-500 500 ¹	-600 600 ¹	-800 800	\ \
I _{T(RMS)}	RMS on-state current	full sine wave;	-		16		Α
I _{TSM}	Non-repetitive peak on-state current	$T_{mb} \le 99$ °C full sine wave; $T_j = 25$ °C prior to surge $t = 20$ ms	-		140		A
l²t dl _⊤ /dt	I ² t for fusing Repetitive rate of rise of on-state current after triggering	$ \begin{aligned} t &= 16.7 \text{ ms} \\ t &= 10 \text{ ms} \\ I_{TM} &= 20 \text{ A}; I_{G} = 0.2 \text{ A}; \\ dI_{G}/dt &= 0.2 \text{ A}/\mu\text{s} \end{aligned} $	-		150 98 100		A A ² s A/μs
I _{GM} V _{GM} P _{GM} P _{G(AV)}	Peak gate current Peak gate voltage Peak gate power Average gate power	over any 20 ms period	- - -		2 5 5 0.5		A V W W
T _{stg}	Storage temperature Operating junction temperature	poriou	-40 -		150 125		Ç

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¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/ μ s.

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R _{th i-a}	Thermal resistance junction to mounting base Thermal resistance junction to ambient	full cycle half cycle minimum footprint, FR4 board	- - -	- - 55	1.2 1.7 -	K/W K/W K/W

STATIC CHARACTERISTICS

T_i = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{GT}	Gate trigger current ²	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}$				
		T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
l IL	Latching current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$				
		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
I _H	Holding current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$	-	31	60	mA
$V_{T}^{I_{H}}$	On-state voltage	$ I_{T} = 20 \text{ A}$	-	1.2	1.5	V
V _{GT}	Gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}$	-	0.7	1.5	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_L = 125 \text{ °C}$	0.25	0.4	-	V
I_{D}	Off-state leakage current	$V_D = V_{DRM(max)}$; $T_j = 125 ^{\circ}C$	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

 $T_i = 25$ °C unless otherwise stated

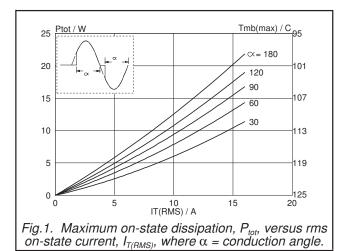
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV _D /dt	Critical rate of rise of	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125 °C;$	1000	4000	-	V/μs
	off-state voltage Critical rate of change of commutating current	exponential waveform; gate open circuit $V_{DM} = 400 \text{ V}; T_j = 125 \text{ °C}; I_{T(RMS)} = 16 \text{ A};$ without snubber; gate open circuit	-	28	-	A/ms
t _{gt}	Gate controlled turn-on time	$I_{TM} = 20 \text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1 \text{ A}$; $dI_G/dt = 5 \text{ A}/\mu\text{s}$	-	2	-	μs

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² Device does not trigger in the T2-, G+ quadrant.

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1000 ITSM / A

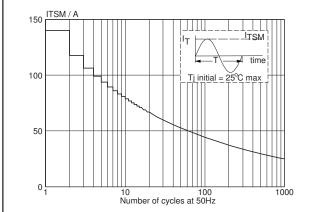
1000 I

50 IT(RMS) / A

40 30 20 10 8.01 0.1 1 10 surge duration / s

Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \le 20$ ms.

Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \le 99$ °C.



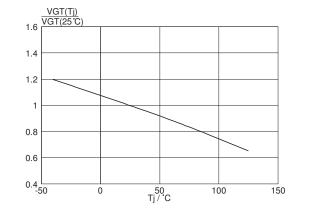
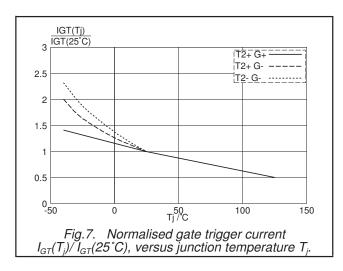


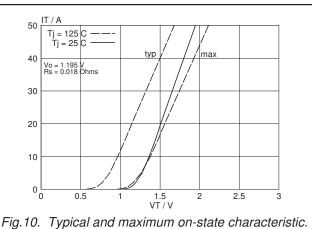
Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, f = 50 Hz.

Fig.6. Normalised gate trigger voltage $V_{GT}(T_i)/V_{GT}(25^{\circ}C)$, versus junction temperature T_i .

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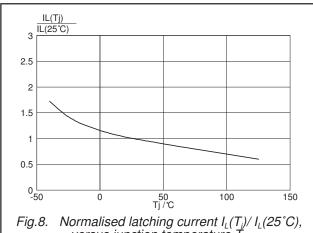


Fig.8. Normalised latching current $I_L(T_i)/I_L(25^{\circ}C)$, versus junction temperature T_i .

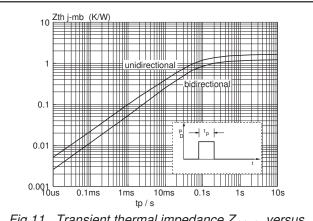


Fig.11. Transient thermal impedance $Z_{th i-mb}$, versus pulse width t_o .

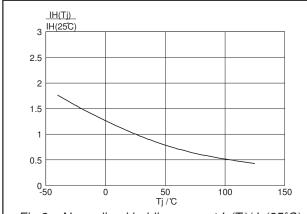


Fig.9. Normalised holding current $I_H(T_i)/I_H(25^{\circ}C)$, versus junction temperature Ti

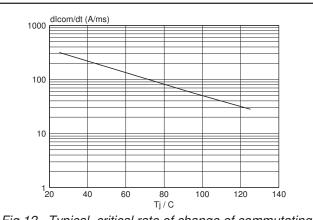
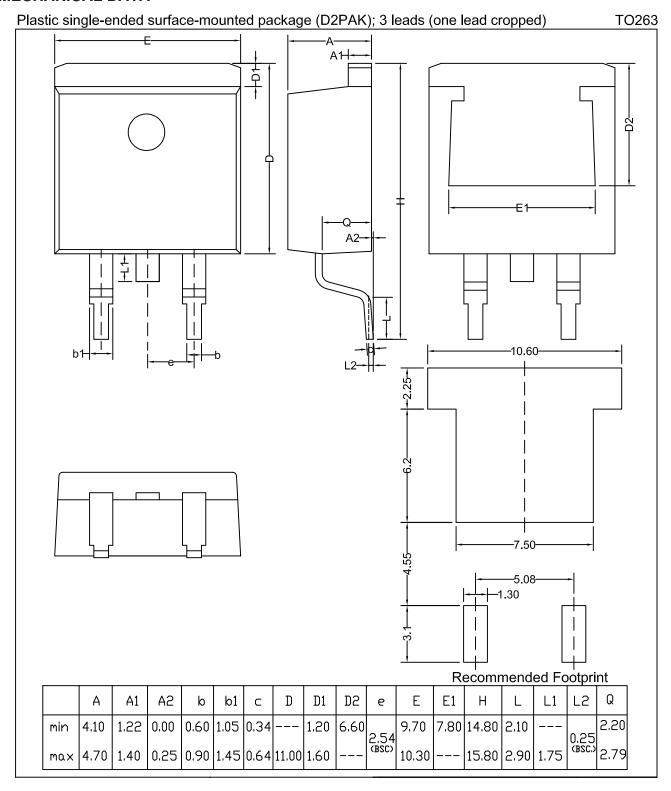


Fig.12. Typical, critical rate of change of commutating current dl_{com}/dt versus junction temperature.

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MECHANICAL DATA



Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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