# BTA225B-800BT

## 3Q Hi-Com Triac

20 June 2018 **Product data sheet**

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT404 (D2PAK) surface mountable plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series BT" triac will commutate the full rated RMS current at the maximum rated junction temperature ($T_{j(max)}$ = 150 °C) without the aid of a snubber.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- High blocking voltage capability
- High junction operating temperature capability ($T_{j(max)}$ = 150 °C)
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- Less sensitive gate for very high noise immunity
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only

## 3. Applications

- Heating controls
- High power motor control
- High power switching
- Applications subject to high temperature ($T_{j(max)}$ = 150 °C)

## 4. Quick reference data

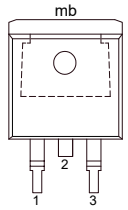
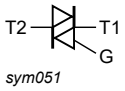
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq$ 117 °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 25 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | - | 190 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms | | - | - | 209 | A |
| $T_j$ | junction temperature | | | - | - | 150 | °C |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 2 | 18 | 50 | mA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 2 | 21 | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 2 | 34 | 50 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | 31 | 60 | mA |
| $V_T$ | on-state voltage | $I_T$ = 30 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.3 | 1.55 | V |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 150 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | - | 2300 | - | V/µs |
| | | $V_{DM}$ = 536 V; $T_j$ = 125 °C; exponential waveform; gate open circuit | | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $T_j$ = 150 °C; $I_{T(RMS)}$ = 25 A; $dV_{com}/dt$ = 20 V/µs; (without snubber condition); gate open circuit | | - | 19 | - | A/ms |
| | | $V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 25 A; $dV_{com}/dt$ = 20 V/µs; (snubber condition); gate open circuit | | - | 44 | - | A/ms |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | T1 | main terminal 1 |  D2PAK (SOT404) |  *sym051* |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| mb | T2 | mounting base; main terminal 2 | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BTA225B-800BT | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq$ 117 °C; Fig. 1; Fig. 2; Fig. 3 | | - | 25 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | 190 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms | | - | 209 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p$ = 10 ms; SIN | | - | 180 | A²s |
| $dI_T/dt$ | rate of rise of on-state current | $I_G$ = 100 mA | | - | 100 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 2 | A |
| $P_{GM}$ | peak gate power | | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.5 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | - | 150 | °C |

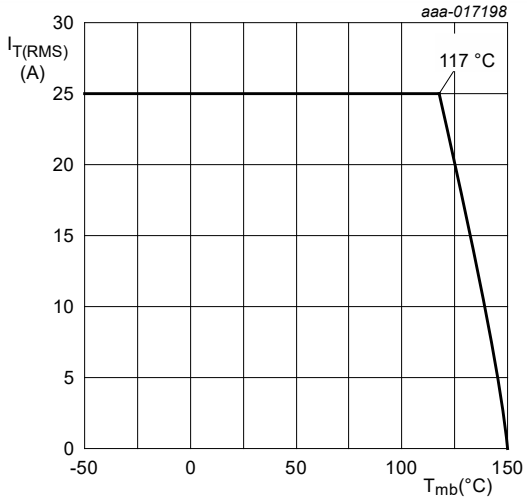
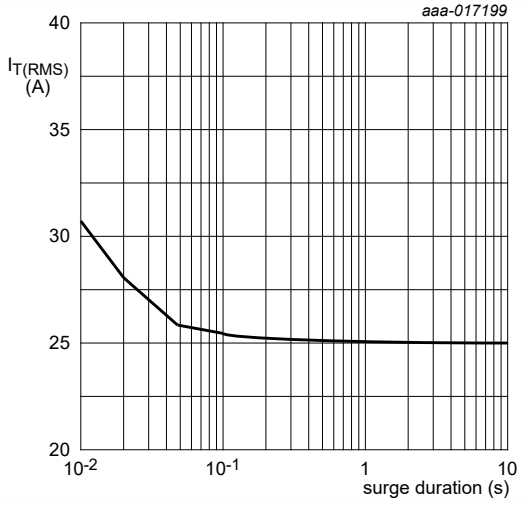
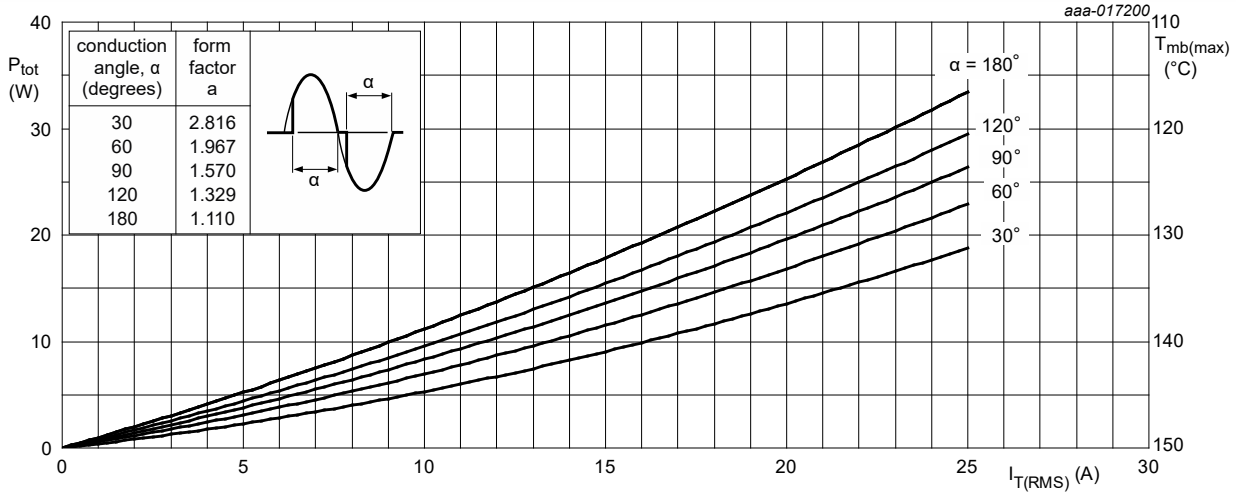



**Fig. 1. RMS on-state current as a function of mounting base temperature**



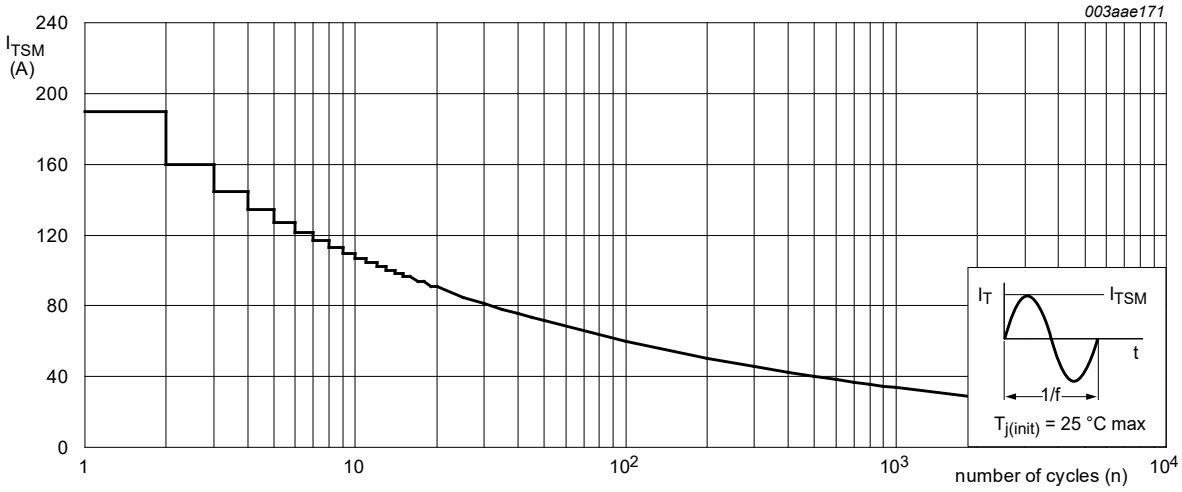

f = 50 Hz; $T_{mb}$ = 117 °C

**Fig. 2. RMS on-state current as a function of surge duration; maximum values**



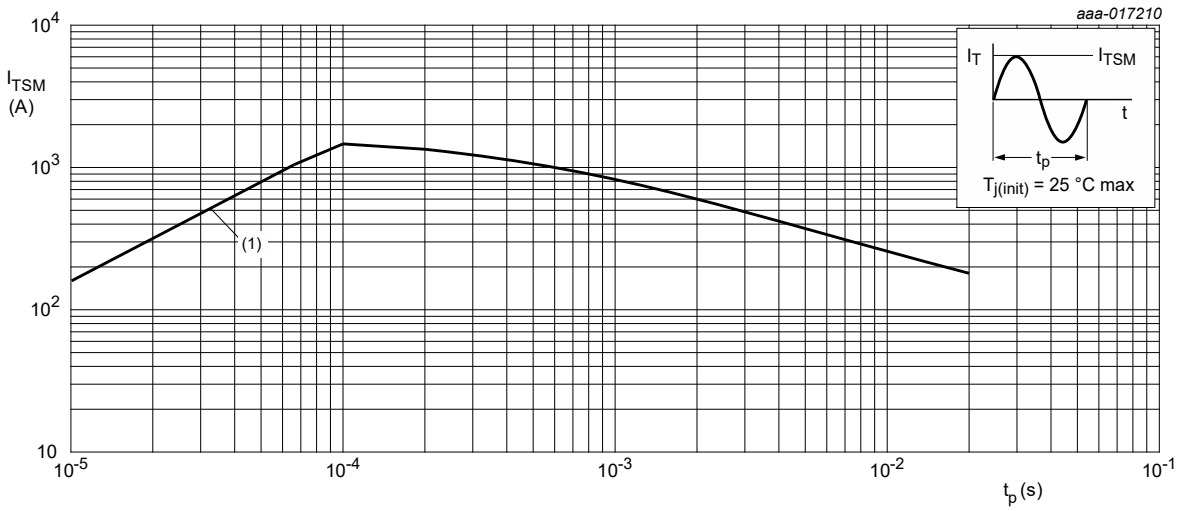

α = conduction angle;
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**



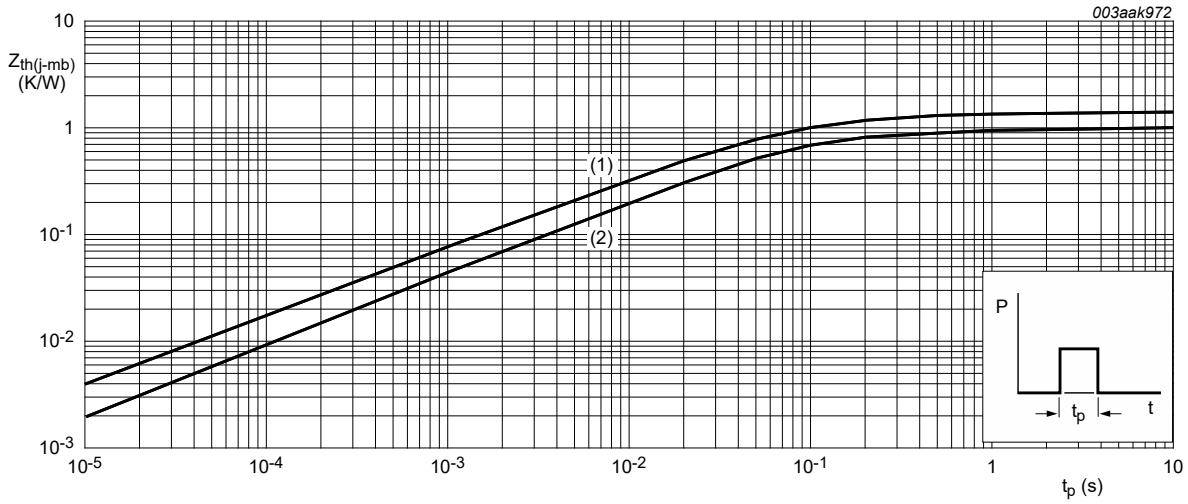

$t_p \leq 20$ ms;
(1) $dI_T/dt$ limit

**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

# 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | full cycle; Fig. 6 | | - | - | 1 | K/W |
| | | half cycle; Fig. 6 | | - | - | 1.4 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | printed circuit board (FR4) mounted | | - | 55 | - | K/W |



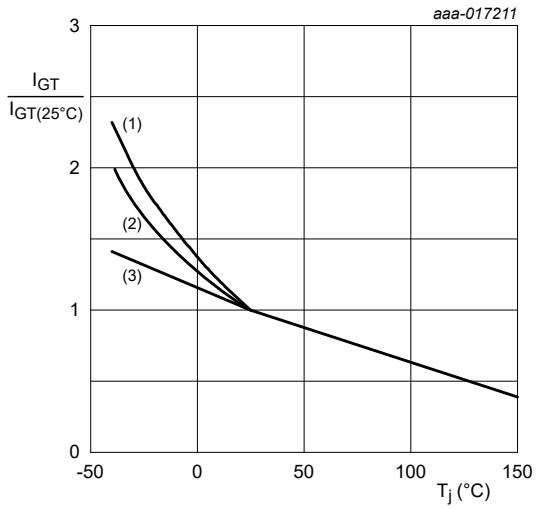

(1) Unidirectional (half cycle)
(2) Bidirectional (full cycle)

**Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 2 | 18 | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 2 | 21 | 50 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 2 | 34 | 50 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 8 | | - | 31 | 60 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 8 | | - | 34 | 90 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 8 | | - | 30 | 60 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | 31 | 60 | mA |
| $V_T$ | on-state voltage | $I_T$ = 30 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.3 | 1.55 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 150 °C | | - | 0.6 | - | V |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 0.7 | 1 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11 | | 0.25 | 0.4 | - | V |
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 150 °C | | - | 0.8 | 4 | mA |
| | | $V_D$ = 800 V; $T_j$ = 25 °C | | - | 0.1 | 10 | µA |
| | | $V_D$ = 800 V; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 150 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | - | 2300 | - | V/µs |
| | | $V_{DM}$ = 536 V; $T_j$ = 125 °C; exponential waveform; gate open circuit | | 1000 | 4000 | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $T_j$ = 150 °C; $I_{T(RMS)}$ = 25 A; $dV_{com}/dt$ = 20 V/µs; (without snubber condition); gate open circuit | | - | 19 | - | A/ms |
| | | $V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 25 A; $dV_{com}/dt$ = 20 V/µs; (snubber condition); gate open circuit | | - | 44 | - | A/ms |




(1) T2- G-
(2) T2+ G-
(3) T2+ G+

**Fig. 7. Normalized gate trigger current as a function of junction temperature**

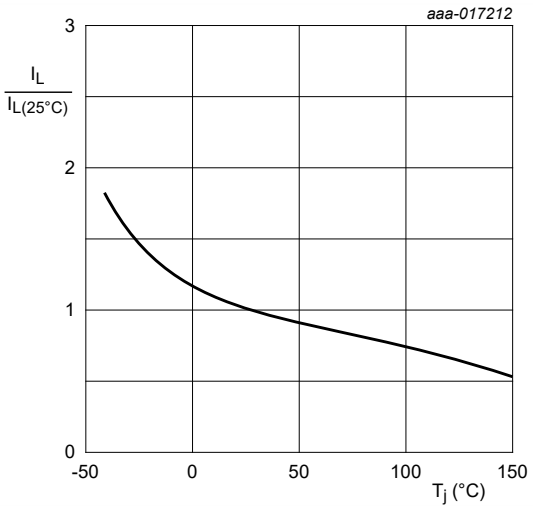



**Fig. 8. Normalized latching current as a function of junction temperature**

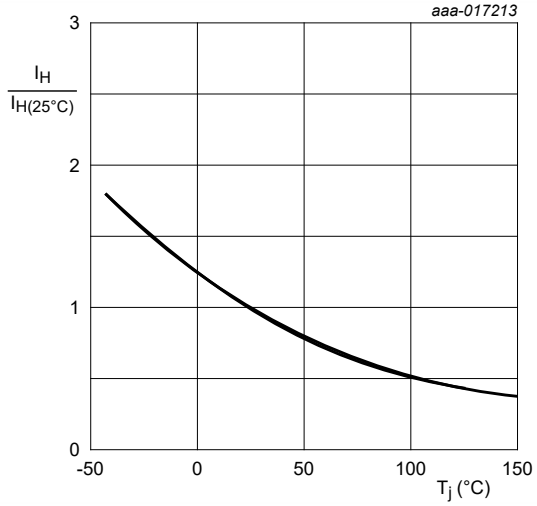
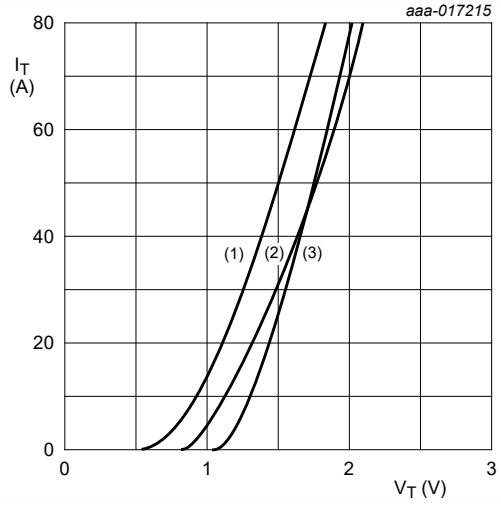



**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.061 V; $R_s$ = 0.015 Ω
(1) $T_j$ = 150 °C; typical values
(2) $T_j$ = 150 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**

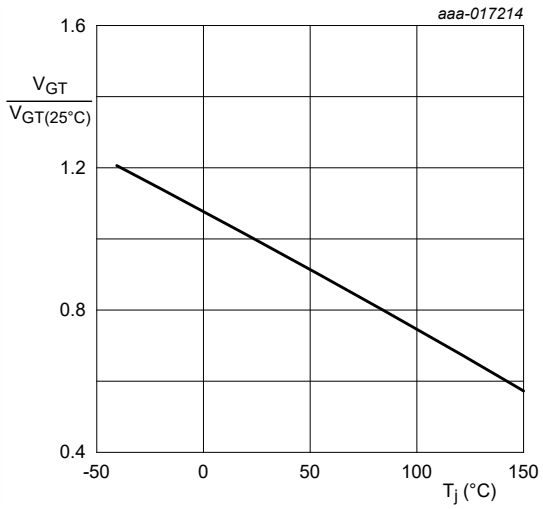
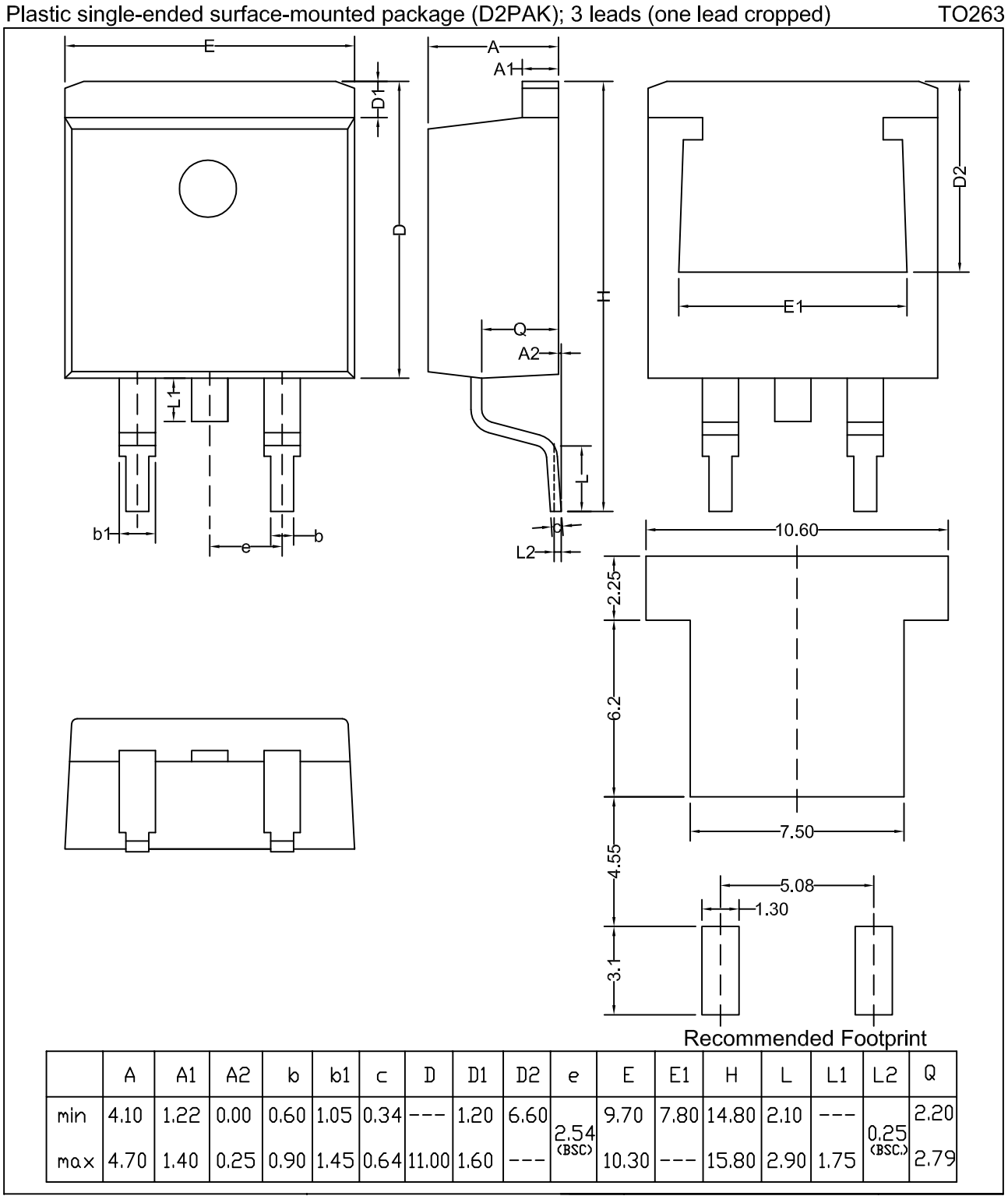



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**

## 10. Package outline




| | A | A1 | A2 | b | b1 | c | D | D1 | D2 | e | E | E1 | H | L | L1 | L2 | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| min | 4.10 | 1.22 | 0.00 | 0.60 | 1.05 | 0.34 | --- | 1.20 | 6.60 | 2.54 (BSC) | 9.70 | 7.80 | 14.80 | 2.10 | --- | 0.25 (BSC) | 2.20 |
| max | 4.70 | 1.40 | 0.25 | 0.90 | 1.45 | 0.64 | 11.00 | 1.60 | --- | | 10.30 | --- | 15.80 | 2.90 | 1.75 | | 2.79 |

**Fig. 12. Package outline D2PAK (SOT404)**

# 11. Legal information

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|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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