

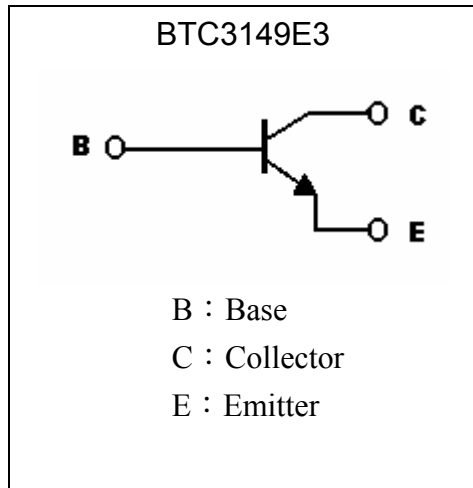
High Voltage NPN Triple Diffused Planar Transistor

BTC3149E3

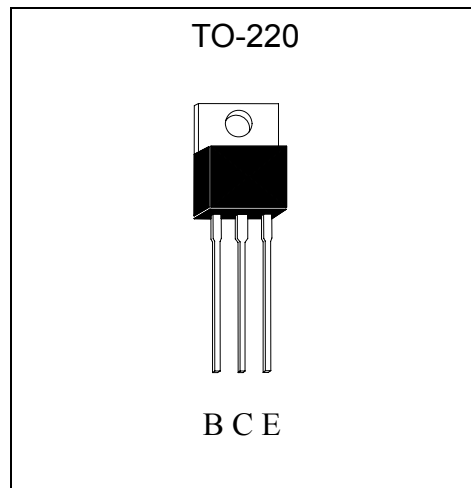
Features

- High voltage, $BV_{CBO}=1600V$ min., $BV_{CEO}=800V$ min.
- Pb-free lead plating package

Symbol



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V_{CBO}	1600	V
Collector-Emitter Voltage	V_{CEO}	800	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	$I_C(DC)$	1.2	A
	$I_C(Pulse)$	3 *1	A
Power Dissipation	$P_d(T_a=25^\circ C)$	2	W
	$P_d(T_c=25^\circ C)$	40	
Operating Junction and Storage Temperature Range	$T_j ; T_{stg}$	-55~+150	°C

Note : *1. Single Pulse $P_w \leq 300\mu s, Duty \leq 2\%$.

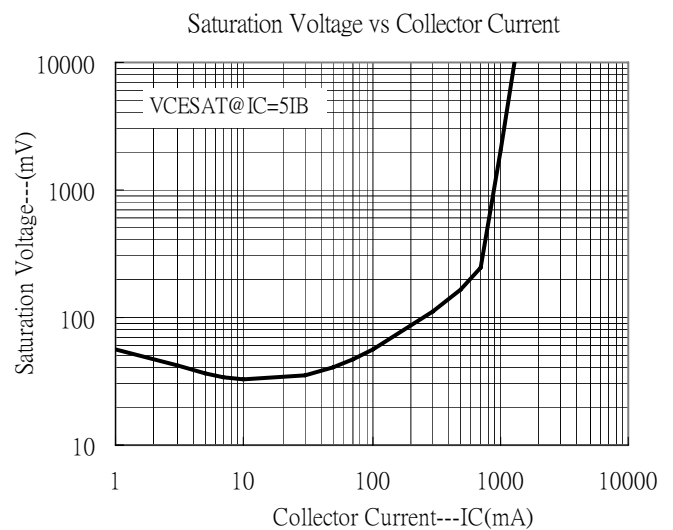
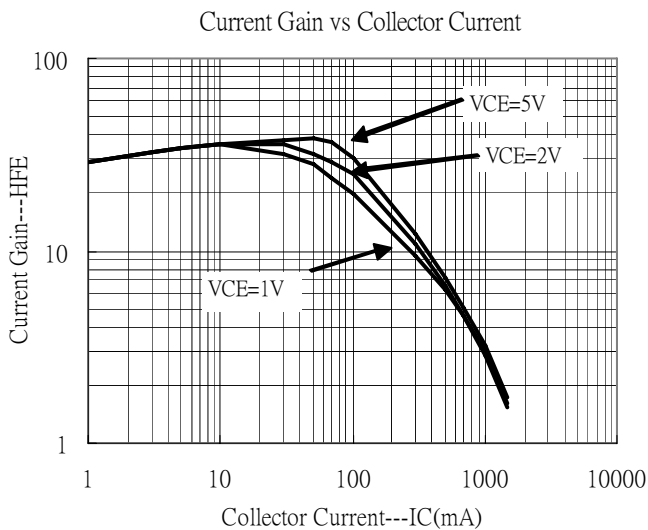
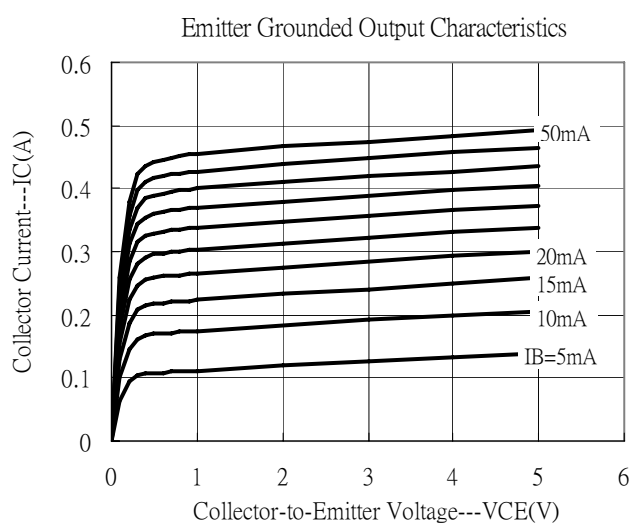
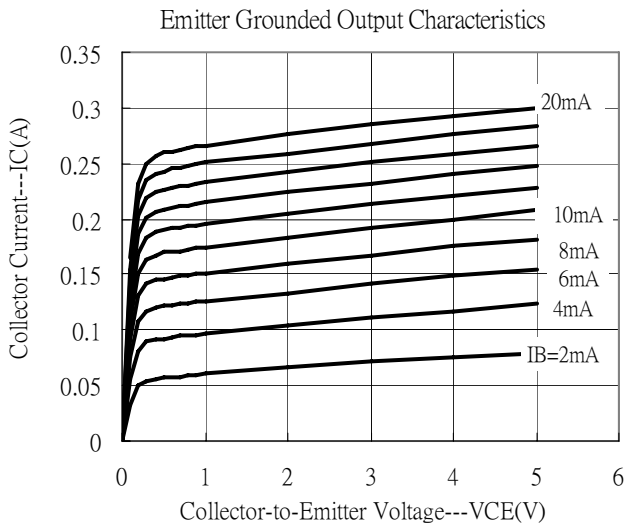
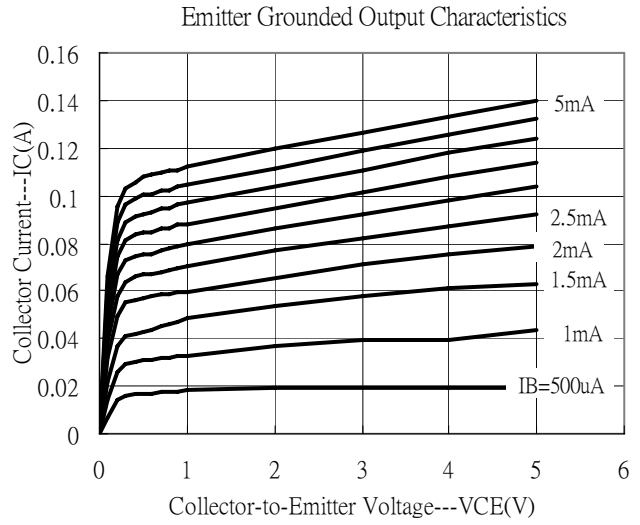
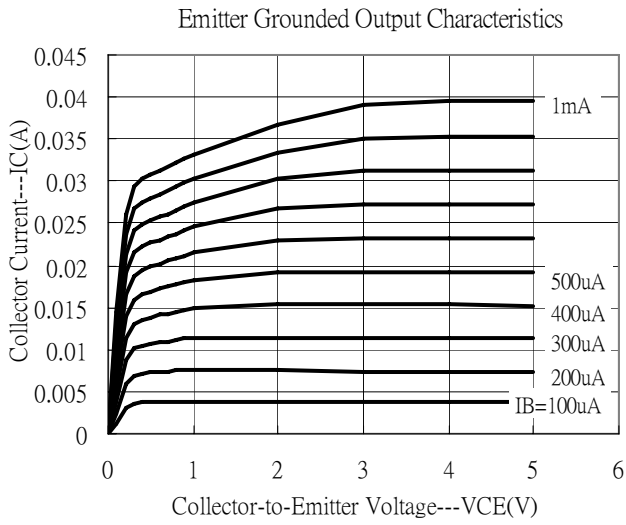
**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	1600	-	-	V	$I_C=100\mu A, I_E=0$
BV_{CEO}	800	-	-	V	$I_C=1mA, I_B=0$
BV_{EBO}	6	-	-	V	$I_E=100\mu A, I_C=0$
I_{CBO}	-	-	10	μA	$V_{CB}=1600V, I_E=0$
I_{CEO}	-	-	10	μA	$V_{CB}=800V, I_B=0$
I_{EBO}	-	-	100	nA	$V_{EB}=6V, I_C=0$
* $V_{CE(sat)}$	-	-	0.2	V	$I_C=200mA, I_B=40mA$
* $V_{CE(sat)}$	-	-	0.35	V	$I_C=500mA, I_B=100mA$
* $V_{BE(sat)}$	-	-	1.2	V	$I_C=500mA, I_B=100mA$
* h_{FE1}	20	-	-	-	$V_{CE}=5V, I_C=10mA$
* h_{FE2}	24	-	35	-	$V_{CE}=5V, I_C=100mA$
* h_{FE3}	5	-	-	-	$V_{CE}=5V, I_C=500mA$
Cob	-	10	-	pF	$V_{CB}=10V, f=1MHz$
tr	-	-	0.8	μs	$V_{CC}=400V, I_C=0.5A, I_{B1}=0.1A$ $I_{B2}=-0.2A$
tstg	-	-	3		
tf	-	-	0.4		

*Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$ **Ordering Information**

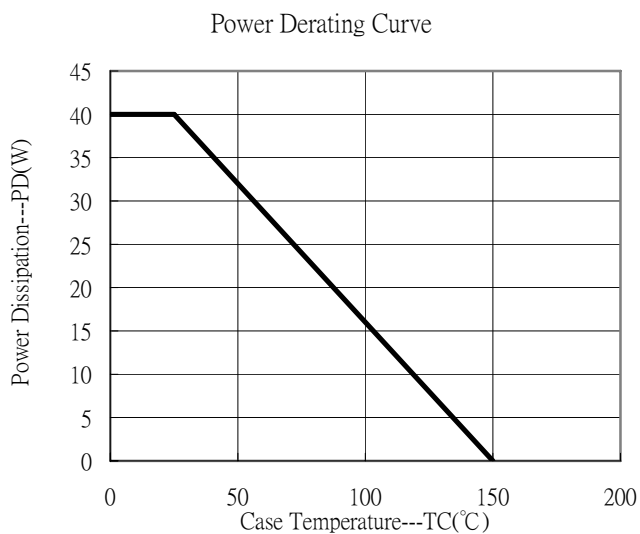
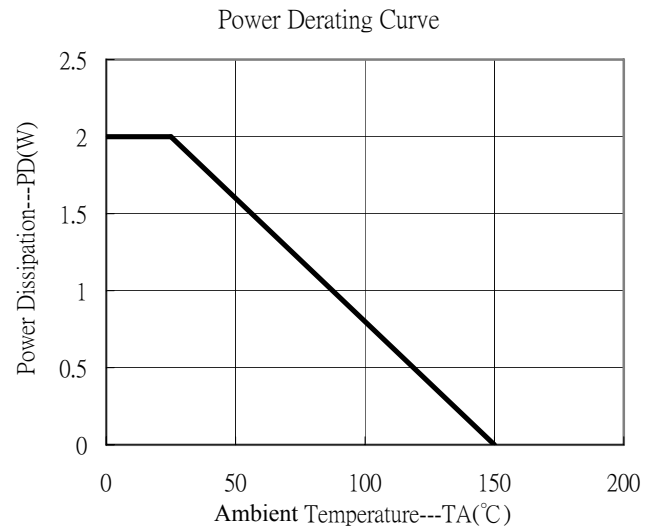
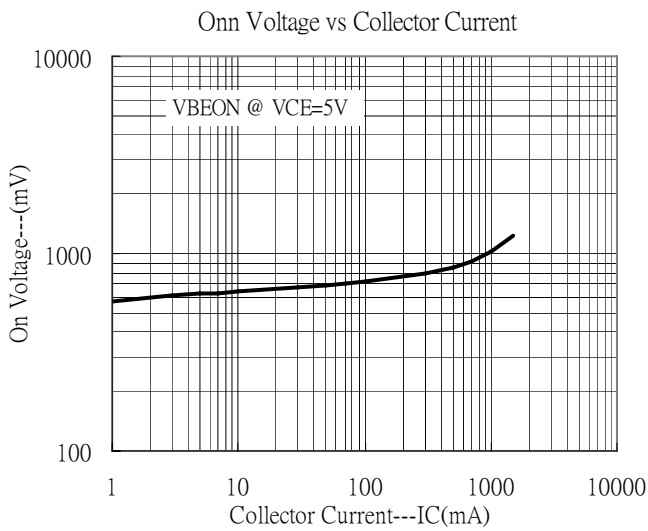
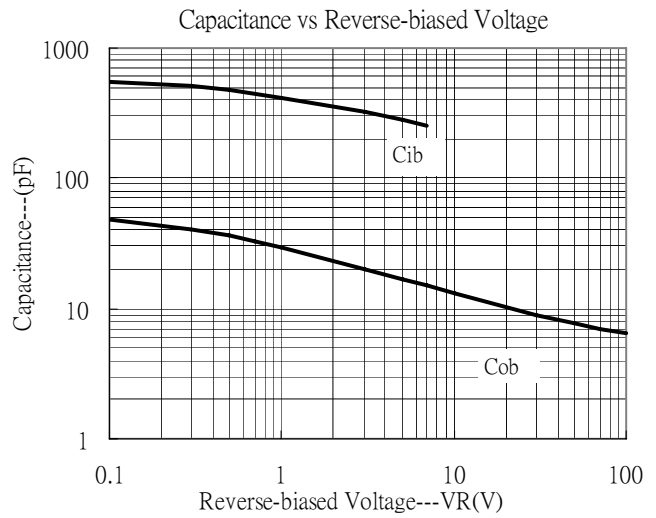
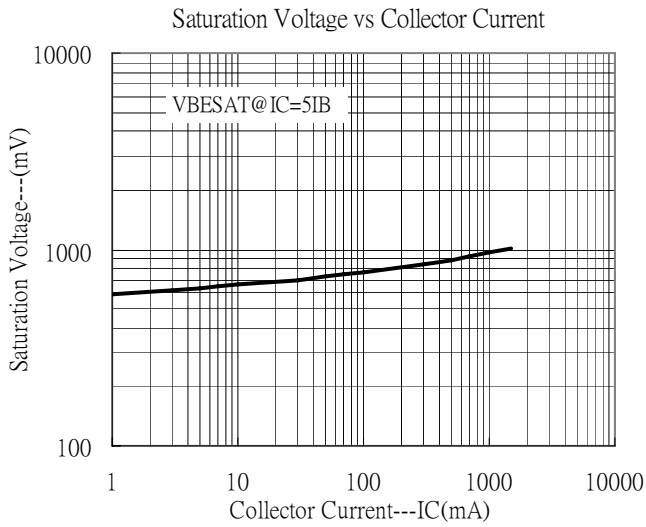
Device	Package	Shipping
BTC3149E3	TO-220 (RoHS compliant package)	50 pcs / tube , 40 tubes/box

Typical Characteristics





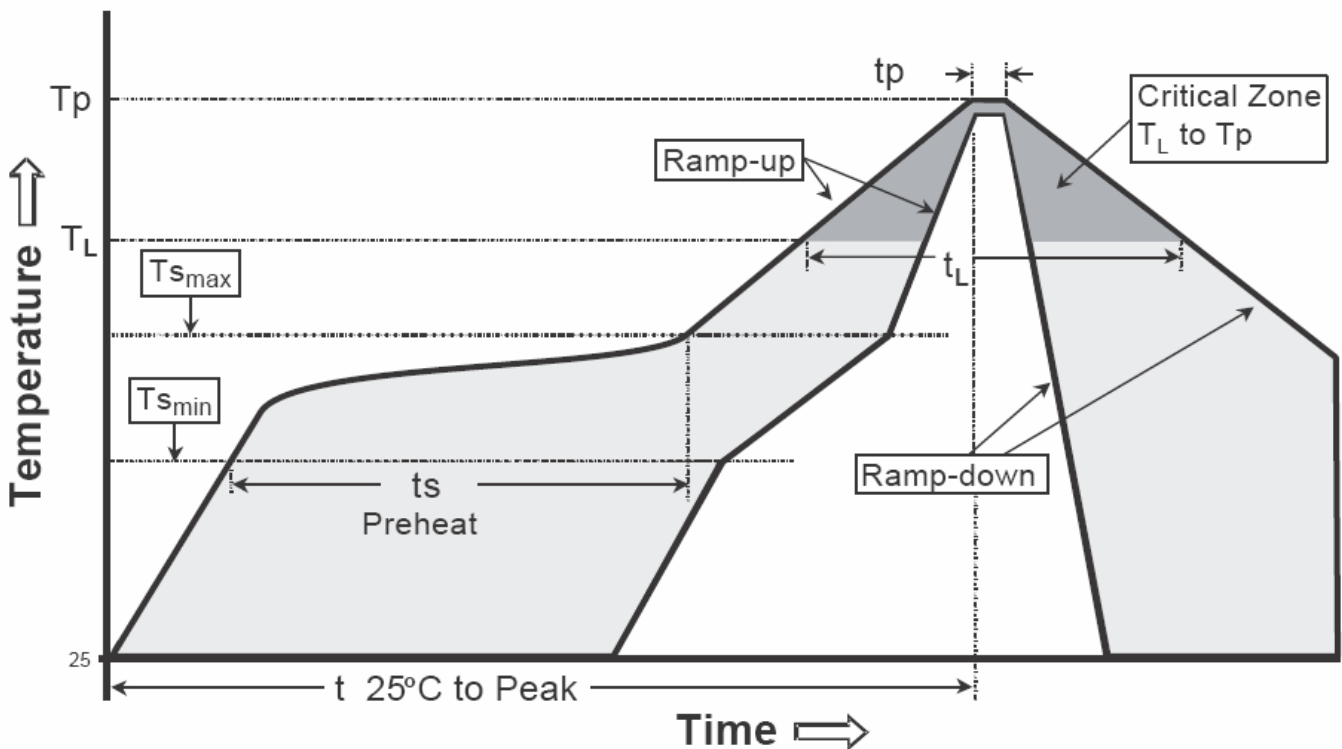
Typical Characteristics(Cont.)



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

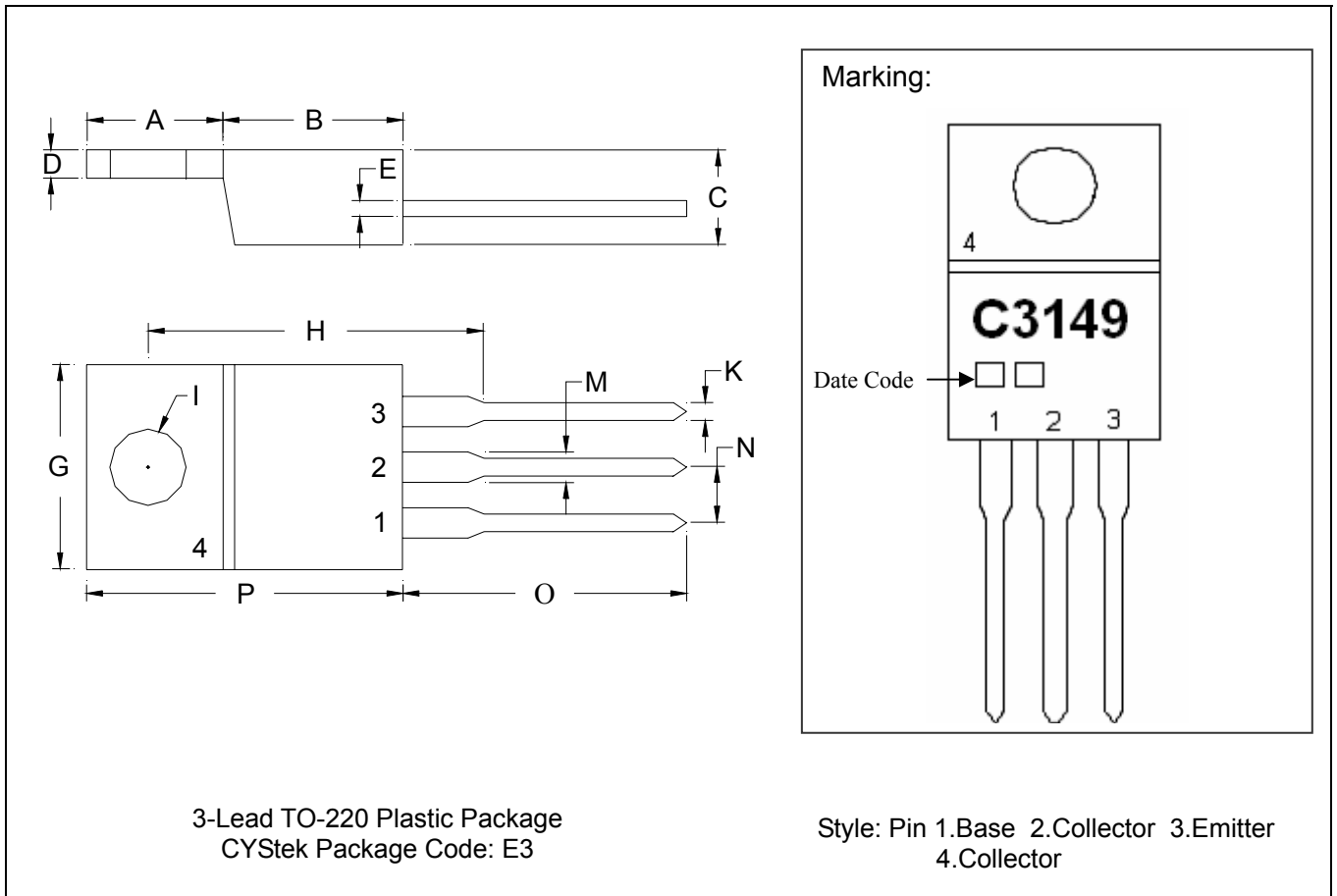
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220 Dimension



3-Lead TO-220 Plastic Package
 CYStek Package Code: E3

Marking:

Style: Pin 1.Base 2.Collector 3.Emitter
 4.Collector

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.2197	0.2949	5.58	7.49	I	-	*0.1508	-	*3.83
B	0.3299	0.3504	8.38	8.90	K	0.0295	0.0374	0.75	0.95
C	0.1732	0.185	4.40	4.70	M	0.0449	0.0551	1.14	1.40
D	0.0453	0.0547	1.15	1.39	N	-	*0.1000	-	*2.54
E	0.0138	0.0236	0.35	0.60	O	0.5000	0.5618	12.70	14.27
G	0.3803	0.4047	9.66	10.28	P	0.5701	0.6248	14.48	15.87
H	-	*0.6398	-	*16.25					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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