

Low Vcesat NPN Epitaxial Planar Transistor

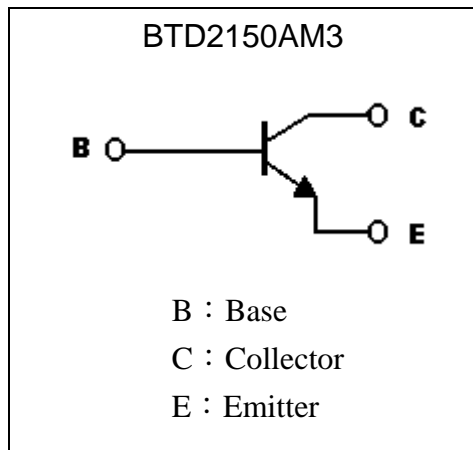
BTD2150AM3

BV_{CEO}	50V
I_C	3A
$R_{CE(SAT)}$ typ.	125m Ω

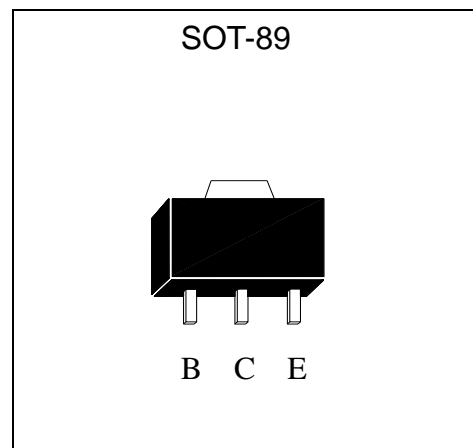
Features

- Low $V_{CE(sat)}$, $V_{CE(sat)}=0.1$ V (typical), at $I_C / I_B = 1A / 50mA$
- Excellent current gain characteristics
- Complementary to BTB1424AM3
- Pb-free lead plating package

Symbol

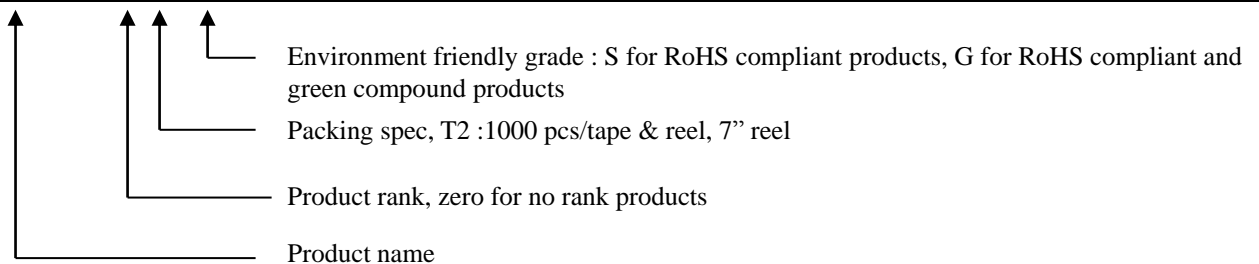


Outline



Ordering Information

Device	Package	Shipping
BTD2150AM3-X-T2-G	SOT-89 (Pb-free lead plating and halogen-free package)	1000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	80	V
Collector-Emitter Voltage	V _{CEO}	50	V
Emitter-Base Voltage	V _{EBO}	6	V
Collector Current	I _C	3	A
Power Dissipation	P _d	0.6	W
		1 *1	
		2 *2	
Operating Junction Temperature Range	T _j	-55~+150	°C
Storage Temperature Range	T _{stg}	-55~+150	°C

Note : *1 Printed circuit board, 1.7mm thick, collector copper plating 10mm*10mm.

*2 When mounted on a 40*40*0.7mm ceramic board.

Characteristics (Ta=25°C)

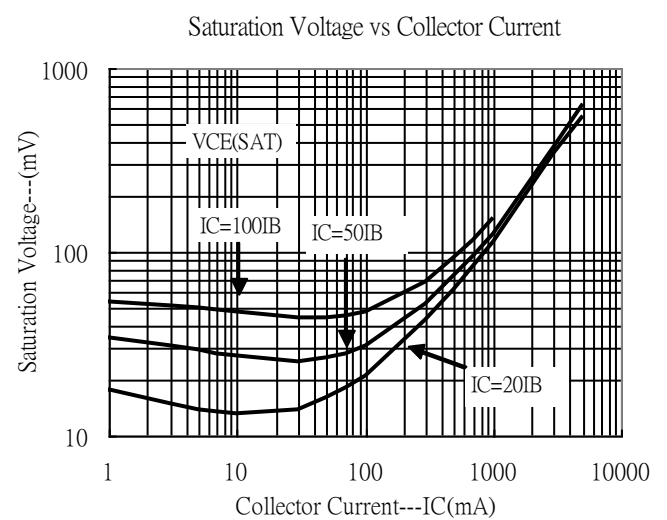
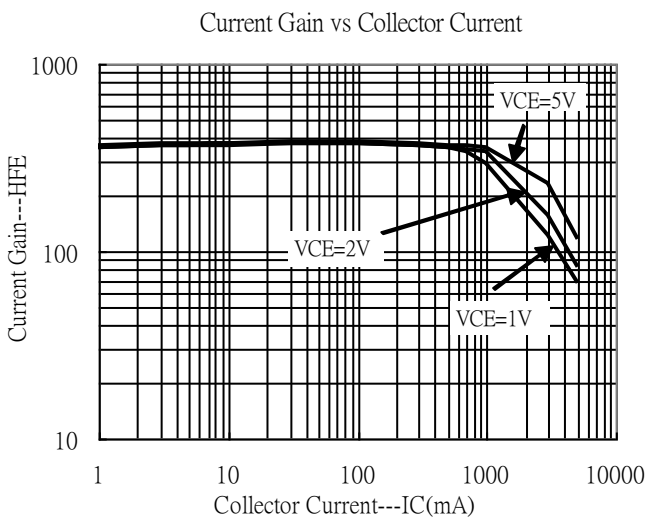
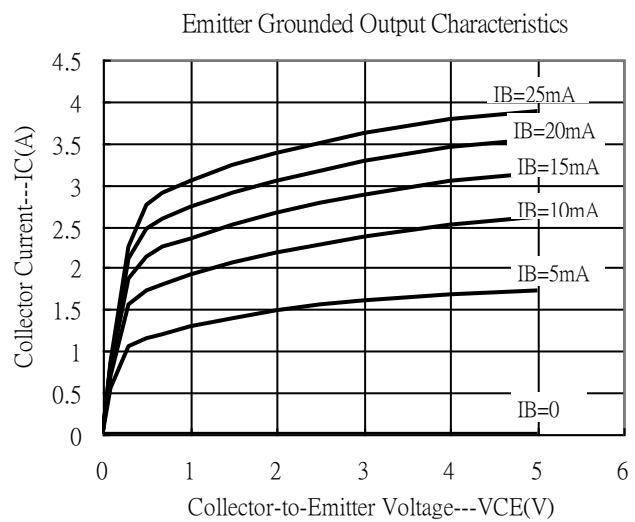
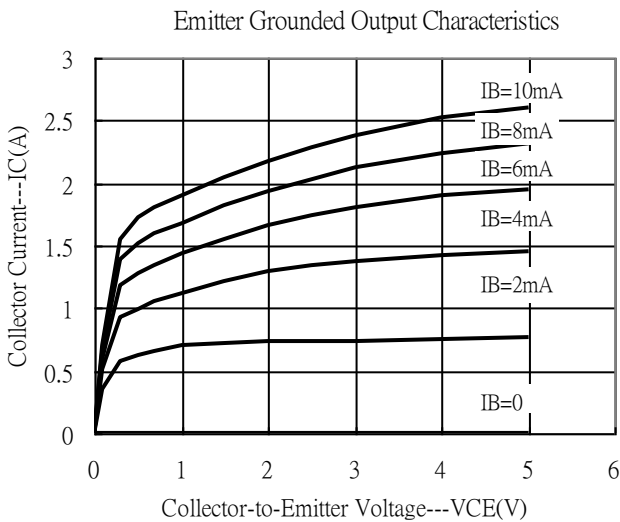
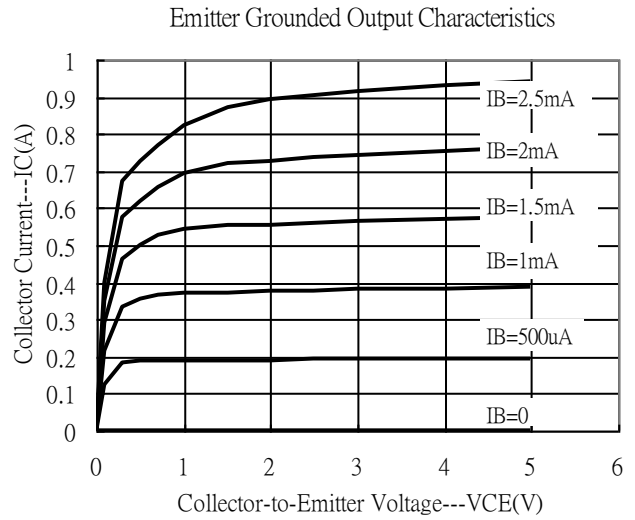
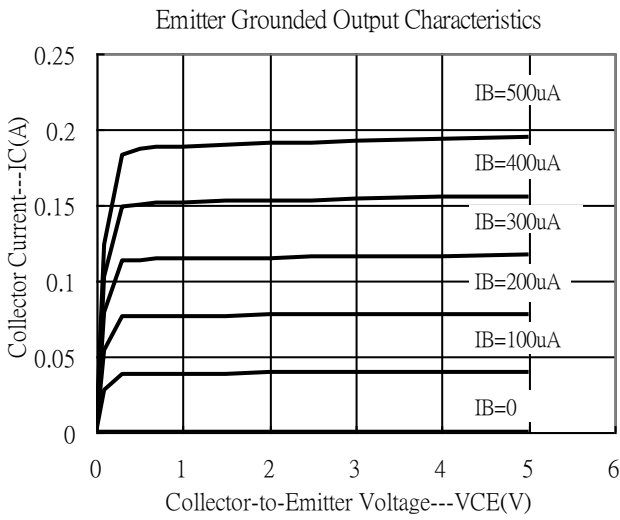
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	80	-	-	V	I _C =50μA, I _E =0
BV _{CEO}	50	-	-	V	I _C =1mA, I _B =0
BV _{EBO}	6	-	-	V	I _E =50μA, I _C =0
I _{CBO}	-	-	0.1	μA	V _{CB} =60V, I _E =0
I _{EBO}	-	-	0.1	μA	V _{EB} =5V, I _C =0
*V _{CE(sat)}	-	0.1	0.25	V	I _C =1A, I _B =50mA
*V _{CE(sat)}	-	0.25	0.5	V	I _C =2A, I _B =0.2A
*R _{CE(sat)}	-	0.125	0.25	Ω	I _C =2A, I _B =0.2A
*V _{BE(sat)}	0.8	1	1.5	V	I _C =2A, I _B =0.2A
*h _{FE1}	180	-	-	-	V _{CE} =2V, I _C =0.1A
*h _{FE2}	180	-	820	-	V _{CE} =2V, I _C =0.5A
*h _{FE3}	100	-	-	-	V _{CE} =2V, I _C =1A
f _T	-	90	-	MHz	V _{CE} =5V, I _C =0.1A, f =100MHz
C _{ob}	-	45	-	pF	V _{CB} =10V, f=1MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Classification Of hFE 2

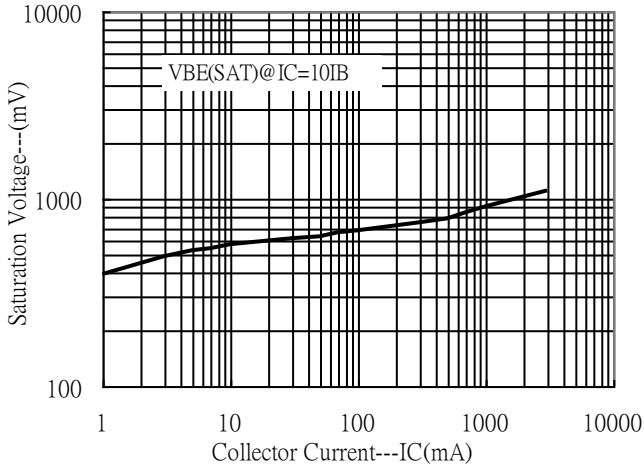
Rank	R	S	T
Range	180~390	270~560	390~820

Typical Characteristics

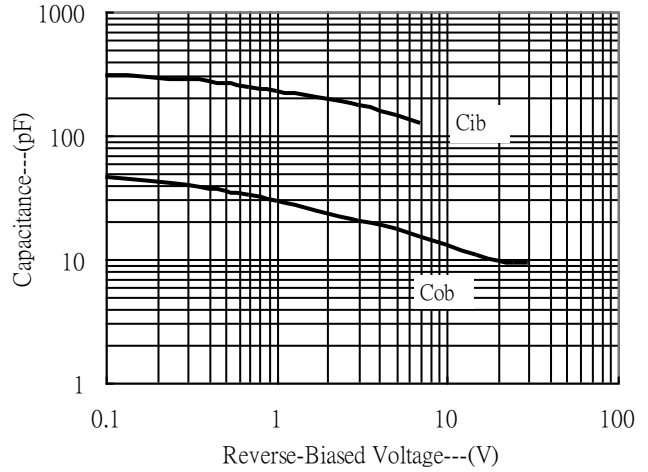


Typical Characteristics(Cont.)

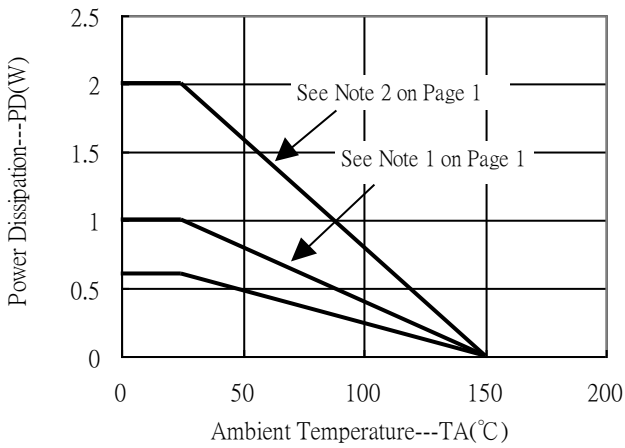
Saturation Voltage vs Collector Current



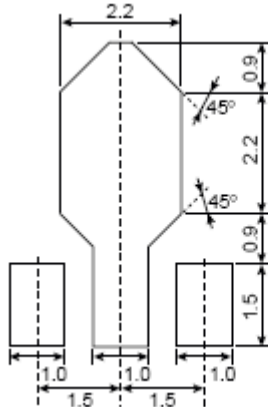
Capacitance vs Reverse-Biased Voltage



Power Derating Curves

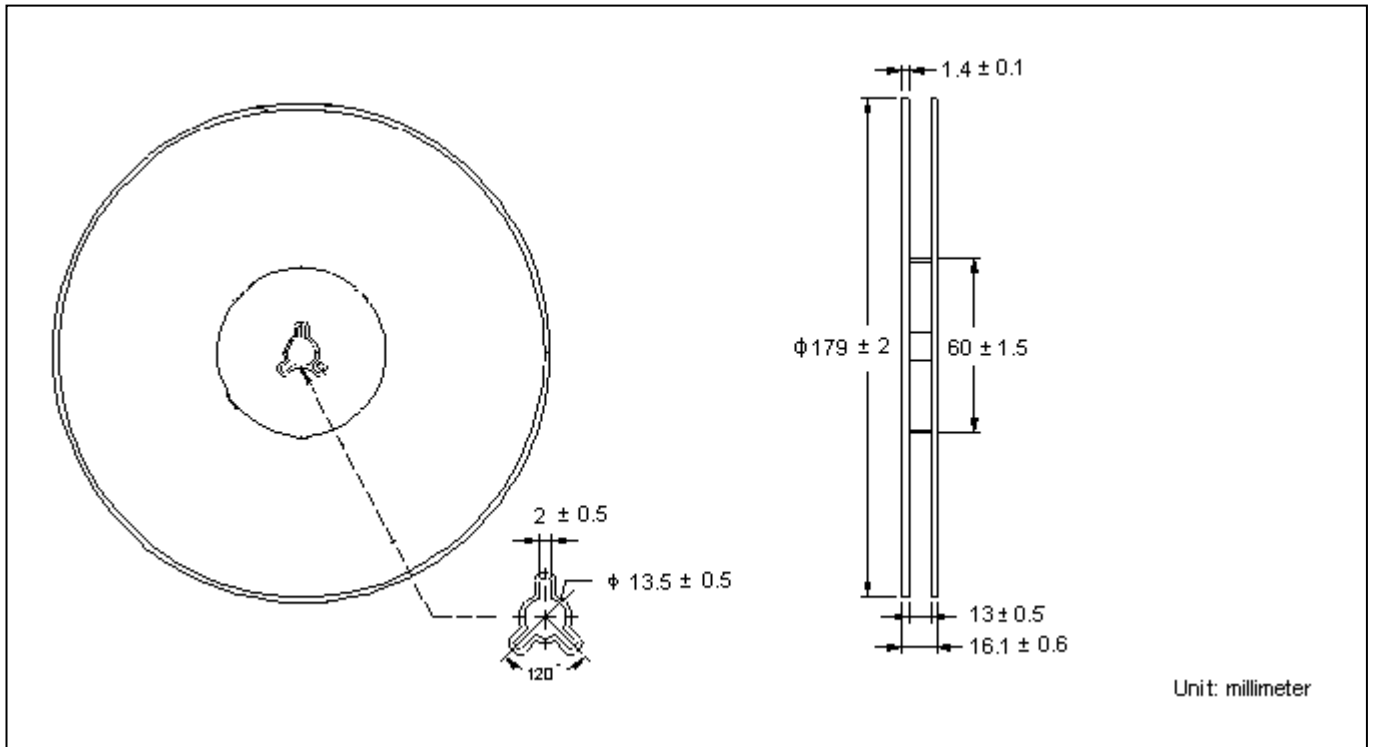


Recommended soldering footprint

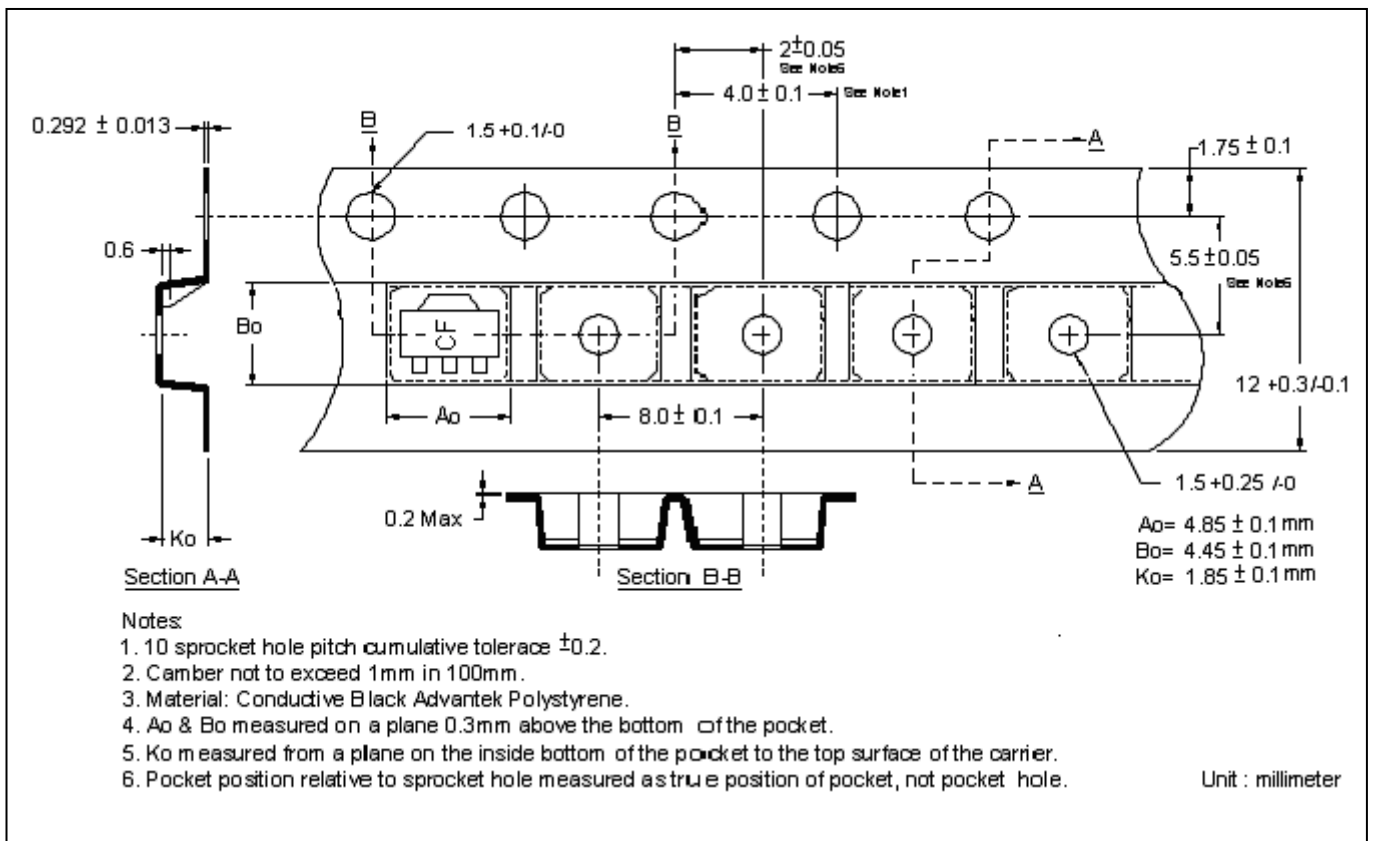


unit : mm

Reel Dimension

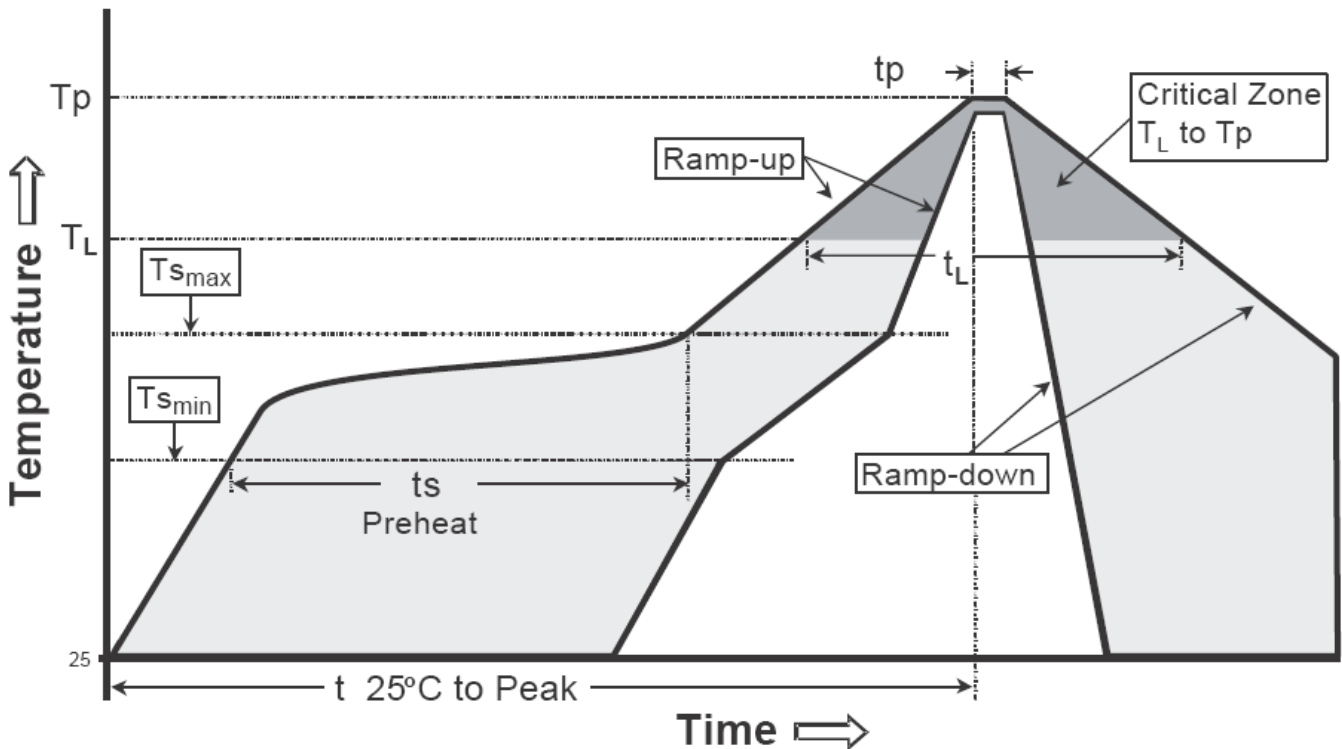


Carrier Tape Dimension



Recommended wave soldering condition

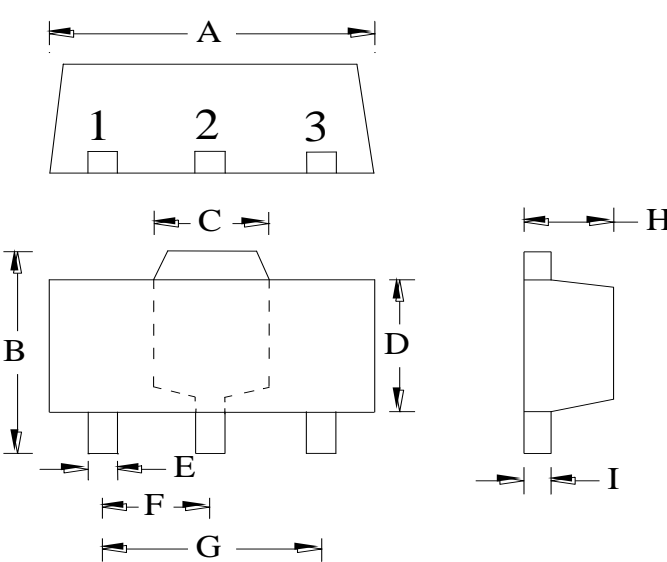
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

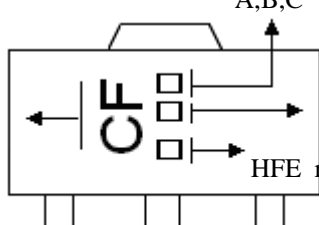
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-89 Dimension



The diagram shows three views of the SOT-89 package: a top view with dimensions A, C, E, F, and G; a front view with dimensions B, D, and I; and a side view with dimension H. The top view also labels the three leads as 1, 2, and 3.

Marking:



month code: 1~9, A,B,C
 Year code : 6→2006, 7→2007,...
 Product Code
 HFE rank

Style: Pin 1. Base 2. Collector 3. Emitter

3-Lead SOT-89 Plastic
 Surface Mounted Package
 CYStek Package Code: M3

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0591	TYP	1.50	TYP
B	0.1551	0.1673	3.94	4.25	G	0.1181	TYP	3.00	TYP
C	0.0610	REF	1.55	REF	H	0.0551	0.0630	1.40	1.60
D	0.0906	0.1024	2.30	2.60	I	0.0138	0.0173	0.35	0.44
E	0.0126	0.0205	0.32	0.52					

- Notes:**
- Controlling dimension: millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.