

# Low Vcesat NPN Epitaxial Planar Transistor

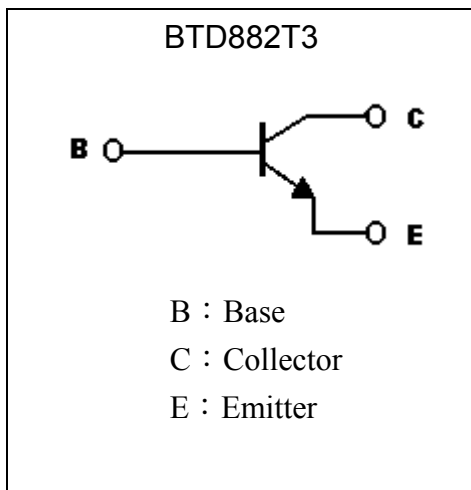
## BTD882T3

$BV_{CEO}$	50V
$I_C$	3A

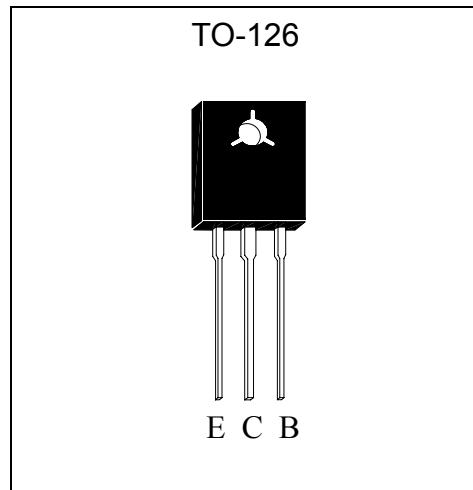
### Features

- Low  $V_{CE(sat)}$ , typically 0.25V at  $I_C / I_B = 2A / 0.2A$
- Excellent current gain characteristics
- Complementary to BTB772T3
- Pb-free lead plating package

### Symbol

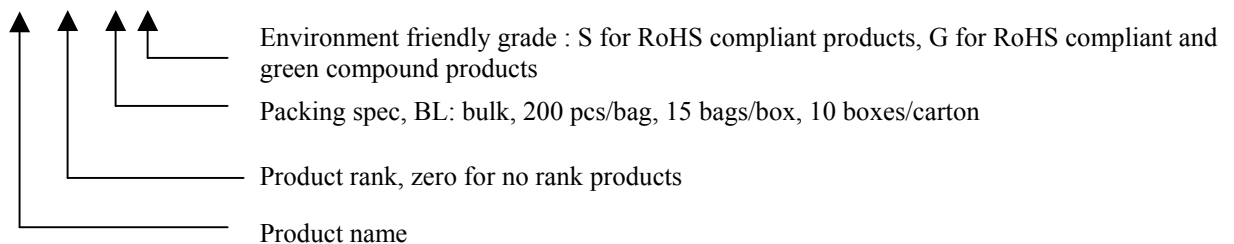


### Outline



### Ordering Information

Device	Package	Shipping
BTD882T3-X-BL-X	TO-126 (Pb-free lead plating package)	200 pcs / bag, 3,000 pcs/box , 30,000 pcs/carton





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V <sub>CB0</sub>	50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	50	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C</sub> (DC)	3	A
	I <sub>C</sub> (Pulse)	7 *1	A
Power Dissipation	Pd(Ta=25°C)	1	W
	Pd(Tc=25°C)	10	
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

Note : \*1. Single Pulse Pw ≤ 350μs, Duty ≤ 2%.

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>th,j-c</sub>	12.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R <sub>th,j-a</sub>	125	°C/W

**Characteristics** (Ta=25°C)

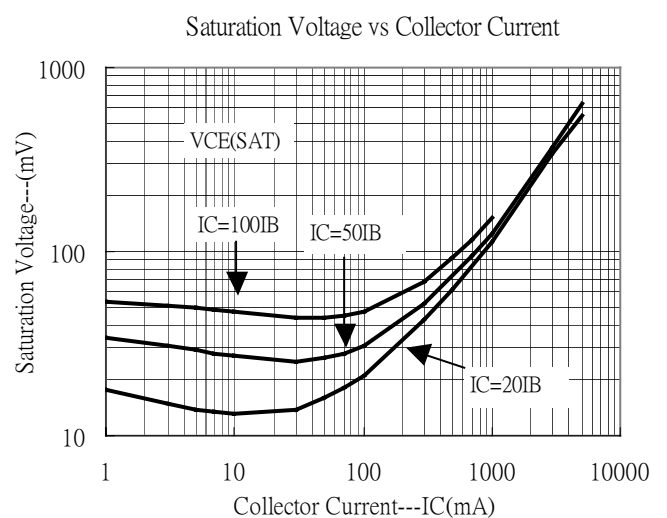
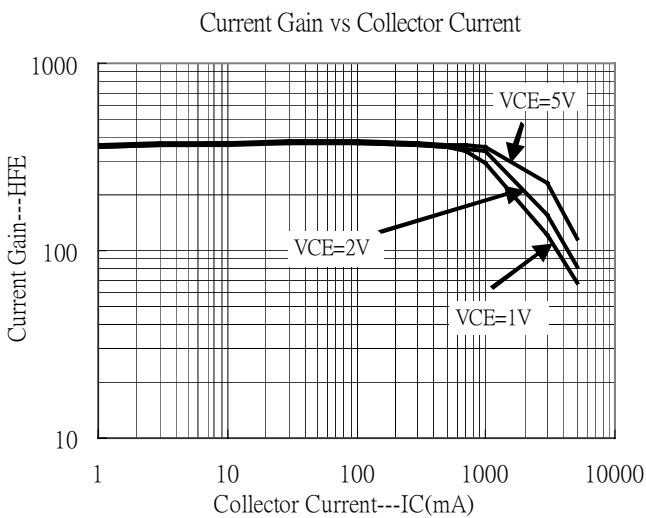
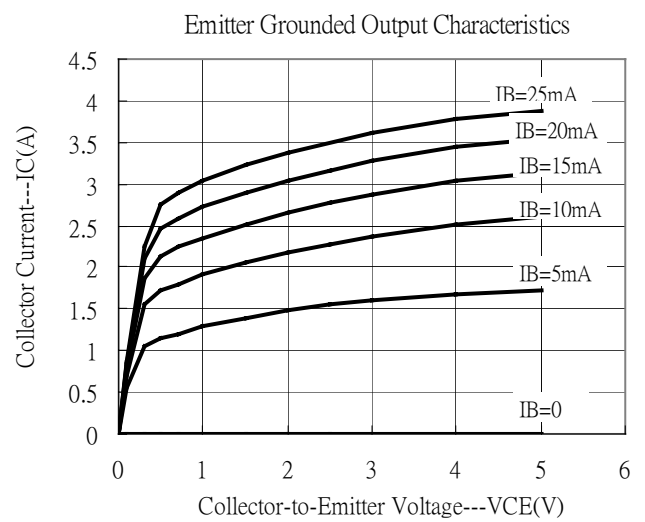
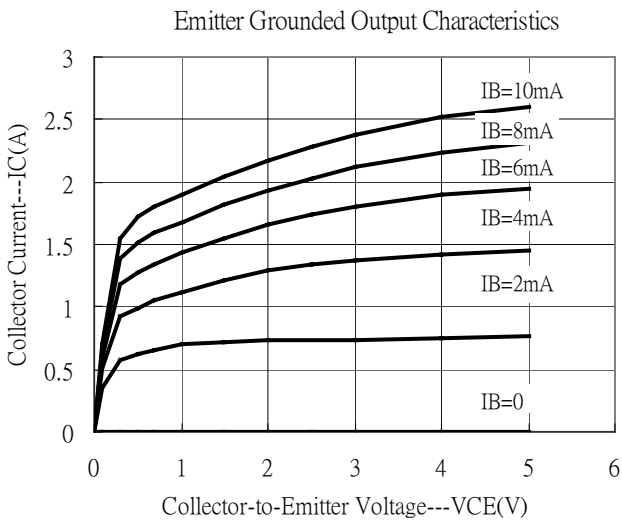
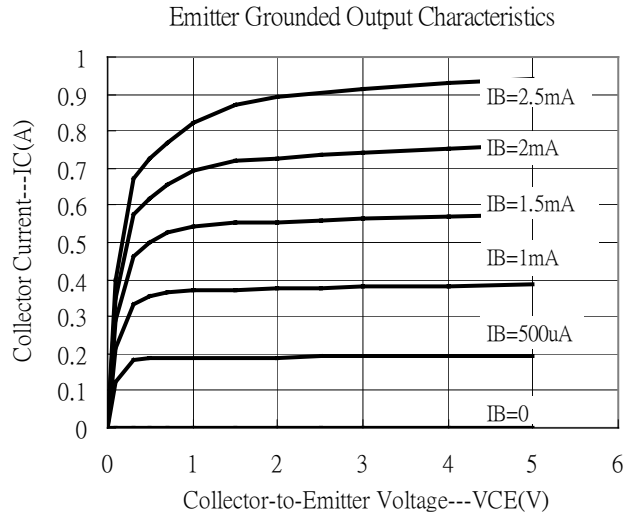
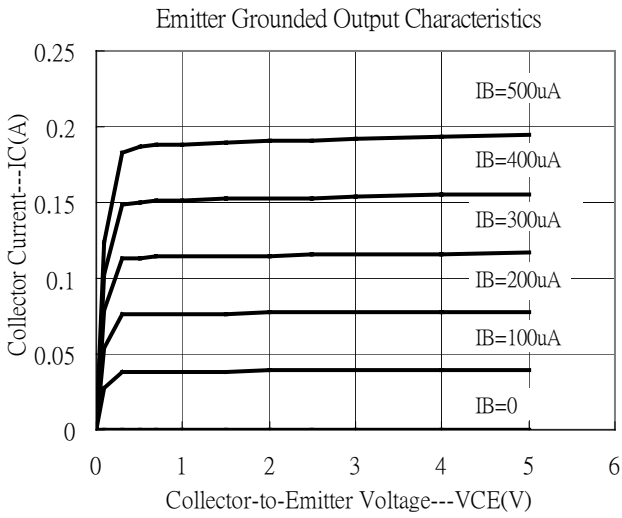
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CB0</sub>	50	-	-	V	I <sub>C</sub> =50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	50	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	5	-	-	V	I <sub>E</sub> =50μA, I <sub>C</sub> =0
I <sub>CB0</sub>	-	-	1	μA	V <sub>CB</sub> =40V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	1	μA	V <sub>EB</sub> =5V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	0.25	0.5	V	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*V <sub>BE(sat)</sub>	-	-	2	V	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*h <sub>FE1</sub>	150	-	-	-	V <sub>CE</sub> =2V, I <sub>C</sub> =20mA
*h <sub>FE2</sub>	180	-	560	-	V <sub>CE</sub> =2V, I <sub>C</sub> =1A
f <sub>T</sub>	-	90	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =0.1A, f=100MHz
Cob	-	45	-	pF	V <sub>CB</sub> =10V, f=1MHz

\*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

**Classification Of hFE 2**

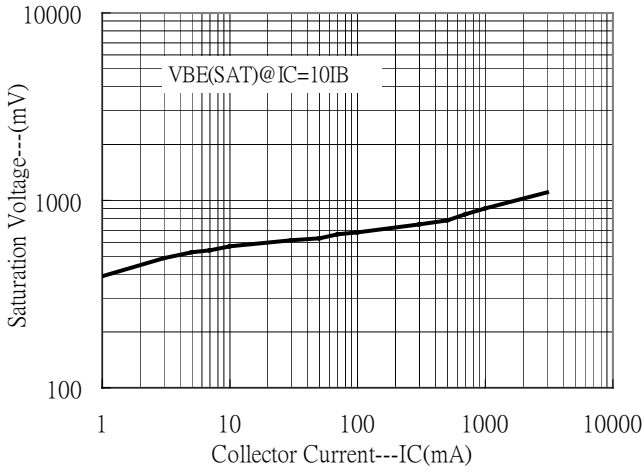
Rank	P	E
Range	180~390	270~560

**Characteristic Curves**

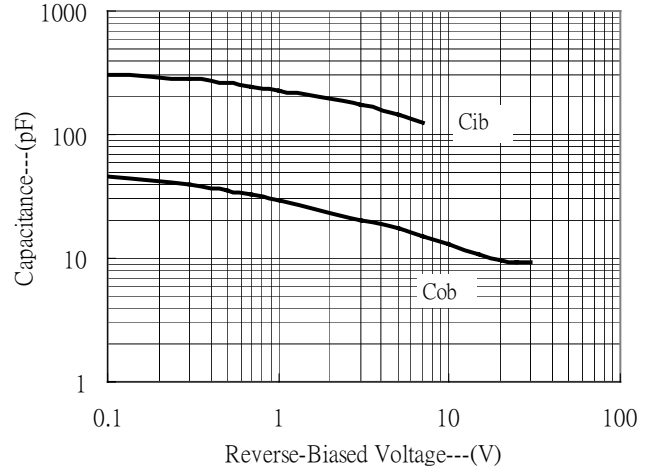


**Characteristic Curves(Cont.)**

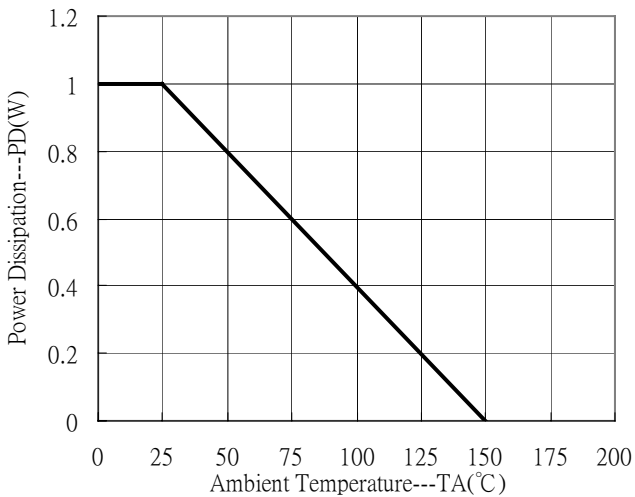
Saturation Voltage vs Collector Current



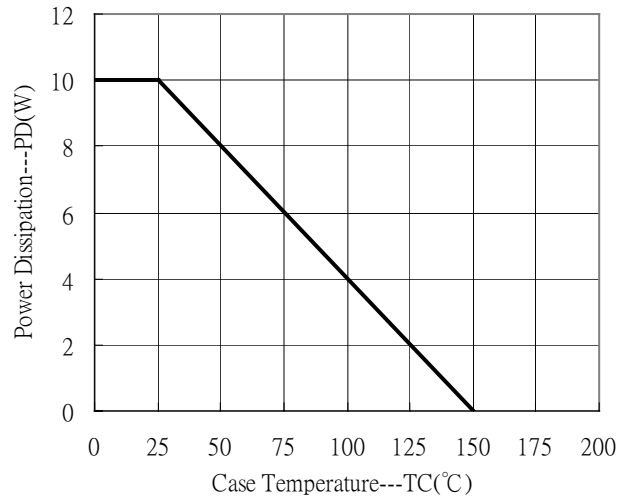
Capacitance vs Reverse-Biased Voltage



Power Derating Curve

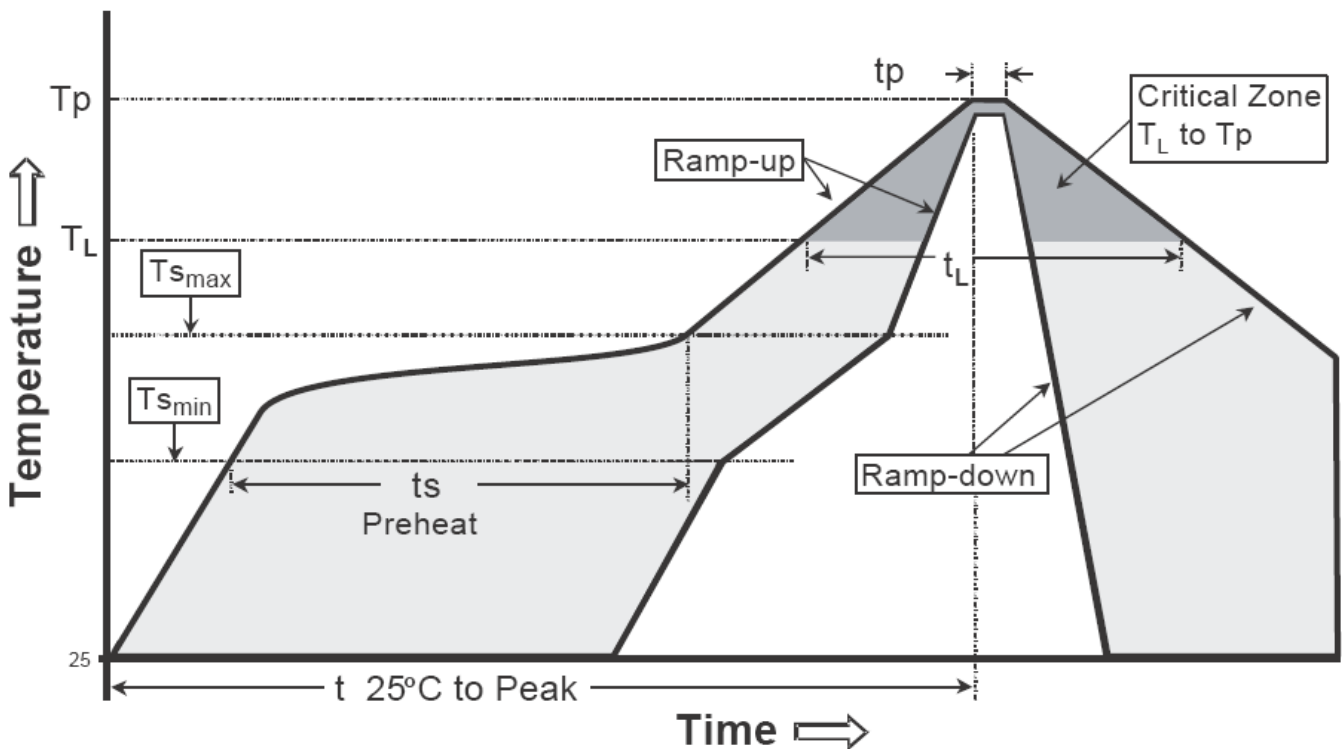


Power Derating Curve



**Recommended wave soldering condition**

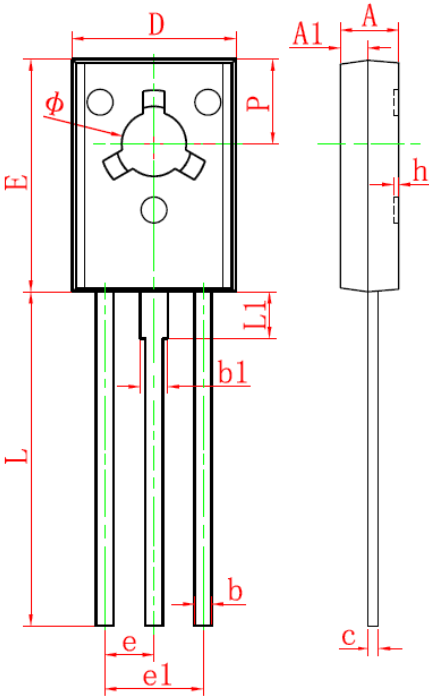
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(ts <sub>min</sub> to ts <sub>max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>p</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

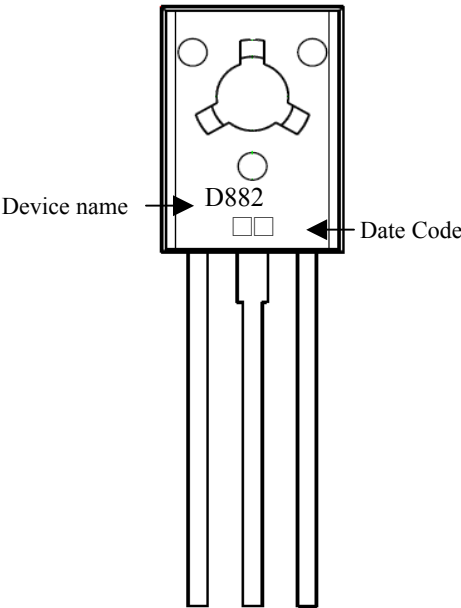
Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-126 Dimension**



The diagram shows two views of a TO-126 package. The left view is a top-down perspective showing dimensions: D (width), E (height), P (pitch),  $\phi$  (lead diameter), L (lead length), L1 (lead length to base), b (lead width), b1 (lead width at base), e (lead spacing), and e1 (lead spacing at base). The right view is a side profile showing dimensions: A (height), A1 (height to base), h (lead thickness), and c (lead thickness at base).

**Marking:**



Device name → D882 ← Date Code

Date Code : Year Code + Month Code  
 Year Code : 2011→1, 2012→2, ..., 2020→0,  
 2021→1, 2022→2, ..., etc  
 Month Code : Jan →1, Feb → 2, ..., Sep→9,  
 Oct→A, Nov→B, Dec→C

Style: Pin 1. Emitter 2. Collector 3. Base

3-Lead TO-126 Plastic Package  
 CYStek Package Code: T3

\*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	$\Phi$	3.000	3.200	0.118	0.126

**Notes:** 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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