Rayson *Bluetooth® Module*

CSR8670 Class2 Stereo Flash Module BTM-860

Features

- The module is a Max.4dBm(Class2) module.
- Fully Qualified Bluetooth v4.0.
- Integrated Switched-Mode Regulator.
- Integrated Battery Charger (200mA)
- 16Mb internal flash memory (64-bit wide,45ns)
- Serial Quad I/O Flash_4Mb(Option)
- Embedded Kalimba DSP Co-Processor.
- Integrated 16-bit Stereo Audio CODEC.
- Support for CSR's latest CVC technology for narrowband and wideband voice connections including wind noise reduction.
- Support Host Interface: USB2.0 or UART.
- Audio interfaces: I²S, PCM and SPDIF
- SBC, MP3, AAC, Faststream ,APTX codec support.
- APTX low-latency including support for SCMS-T
- HSP / HFP / A2DP / AVRCP/ PBAP / SPP
- Bluetooth Low Energy compatible
- Support for up to 6 capacitive touch sensor inputs
- Integrated chip antenna
- RoHS compliant.
- Small outline. 16.0 x 23.9 x 2.3 mm

Outline

Applications

- Stereo Wireless Headsets.
- Wired or wireless speakers and headphones.
- Smart remote controllers.
- TVs
- Audio adaptors

V05 2013.11.04

General Electrical Specification

Absolute Maximum Ratings:		
Ratings	**Min.**	**Max.**
Storage Temperature	-40 ℃	+85 ℃
Supply Voltage (VCHG)	-0.4V	5.75V
Supply Voltage (VBAT)	-0.4V	4.4V
Supply Voltage (VBAT_SENSE)	-0.4V	5.75V
Supply Voltage (VREG_ENABLE)	-0.4V	4.4V

Supply Voltage (LED[2:0])	-0.4V	4.4V
Supply Voltage (PIO_POWER)	-0.4V	3.6V
Recommended Operating Condition:		
Operating Condition		
Operating Temperature range	-20 ℃	+75 ℃
Supply Voltage (VCHG)	4.75V / 3.10 V	5.75V
Supply Voltage (VBAT)	2.5V	4.25V
Supply Voltage (VBAT_SENSE)	0V	4.25V
Supply Voltage (VREG_ENABLE)	0V	4.25V
Supply Voltage (LED[2:0])	1.10V	4.25V
Supply Voltage (PIO_POWER)*	1.7V	3.6V

1.8V Switch-mode Regulator

1.8V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage (VBAT)	2.80	3.70	4.25	V
Output voltage (1V8_SMPS)	1.70	1.80	1.90	V
Normal Operation				
Transient settling time	-	30	-	μs
Load current	-	-	185	mA
Current available for external use, stereo audio with 16Ω load[a]	-	-	25	mA
Peak conversion efficiency	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	μs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

(a) More current available for audio loads above 16Ω.

Regulator Enable

VREG_ENABLE, Switching Threshold	Min	Typ	Max	Unit
Rising threshold	1.0	-	-	V

Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage, VCHG[a]	4.75 / 3.10	5.00	5.75	V

(a) Reduced specification from 3.1 to 4.75. Full specification > 4.75V.

Trickle Charge Mode		**Min**	**Typ**	**Max**	**Unit**
Charge current $I_{trickle}$, as percentage of fast charge current		8	10	12	%
V_{fast} rising threshold		-	2.9	-	V
V_{fast} rising threshold trim step size		-	0.1	-	V
V_{fast} falling threshold		-	2.8	-	V
Fast Charge Mode		**Min**	**Typ**	**Max**	**Unit**
Charge current during constant Current mode, I_{fast}	Max, headroom > 0.55V	194	200	206	mA
	Min, headroom > 0.55V		10		mA
Reduced headroom charge current, As a percentage of I_{fast}	Mid, headroom=0.15V	50	-	100	%
I-CTRL charge current step size		-	10	-	mA
V_{float} threshold, calibrated		4.16	4.20	4.24	V
Standby Mode		**Min**	**Typ**	**Max**	**Unit**
Voltage hysteresis on VBAT, V_{hyst}		100	-	150	mV
Error Charge Mode		**Min**	**Typ**	**Max**	**Unit**
Headroom[(a)] error rising threshold		30	-	50	mV
Headroom[(a)] error threshold hysteresis		20	-	30	mV

(a) Headroom=VCHG-VBAT

External Charge Mode	**Min**	**Typ**	**Max**	**Unit**
Fast charge current, I_{fast}	200	-	500	mA
Control current into CHG_EXT	0	-	20	mA
Voltage on CHG_EXT	0		5.75	V
External pass device h_{fe}	-	50	-	-
Sense voltage, between VBAT_SENSE and VBAT at maximum current	195	200	205	mV

(a) In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

Stereo Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Input Sample Rate, Fsample	-		8	-	48	kHz
SNR	fin = 1kHz	F_{sample}				
	B/W = 20Hz→Fsample/2	8kHz	-	93	-	dB

	(20kHz max)	16kHz	-	92	-	dB
	A-Weighted	32kHz	-	92	-	dB
	THD+N < 1%	44.1kHz	-	92	-	dB
	1.6Vpk-pk input	48kHz	-	92	-	dB
THD+N	fin = 1kHz B/W = 20Hz→Fsample/2 (20kHz max) 1.6Vpk-pk input	F_{sample}				
		8kHz	-	0.004	-	%
		48kHz	-	0.008	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or30dB Analogue setting = -3dB to 12dB in 3dB steps		-3	-	42	dB
Stereo separation (crosstalk)			-	-89	-	dB

Stereo Codec: Digital to Analogue Converter

Digital to Analogue Converter							
Parameter	**Conditions**			**Min**	**Typ**	**Max**	**Unit**
Resolution	-			-	-	16	Bits
Output Sample Rate, Fsample	-			8	-	96	kHz
SNR	fin = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.1% 0dBFS input	Fsample	Load				
		48kHz	100kΩ	-	96	-	dB
		48kHz	32Ω	-	96	-	dB
		48kHz	16Ω	-	96	-	dB
THD+N	fin = 1kHz B/W = 20Hz→20kHz 0dBFS input	Fsample	Load				
		8kHz	100kΩ	-	0.002	-	%
		8kHz	32Ω	-	0.002	-	%
		8kHz	16Ω	-	0.003	-	%
		48kHz	100kΩ	-	0.003	-	%
		48kHz	32Ω	-	0.003	-	%
		48kHz	16Ω	-	0.004	-	%
Digital Gain	Digital Gain Resolution = 1/32			-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB			-21	-	0	dB
Stereo separation (crosstalk)				-	-88	-	dB

Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7xPIO_POWER	-	PIO_POWER+0.4	V
Tr/Tf	-	-	25	ns
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{IH} output logic level high, I_{OH} = -0.4mA	0.75xPIO_POWER	-	-	V
Tr/Tf	-	-	5	ns
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	uA
Strong pull-down	10	40	150	uA
Weak pull-up	-5	-1.0	-0.33	uA
Weak pull-down	0.33	1.0	5.0	uA
C_I input Capacitance	1.0		5.0	pF

LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Current, I_{PAD}	High impedance state	-	-	5	μA
	Current sink state	-	-	10	mA
LED pad voltage, V_{PAD}	I_{PAD} = 10mA	-	-	0.55	V
LED pad resistance	V_{PAD} < 0.5V	-	-	40	Ω
V_{OL} output logic level low[(a)]		-	0	-	V
V_{OH} output logic level high[(a)]		-	0.8	-	V
V_{IL} input logic level low		-	0	-	V
V_{IH} input logic level high		-	0.8	-	V

(a) LED output port is open-drain and requires a pull-up

Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range(a)		0	-	1.35	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		1.38	1.69	2.75	µs
Sample rate(b)		-	-	700	Samples/s

(a) LSB size = VDD_AUX/1023

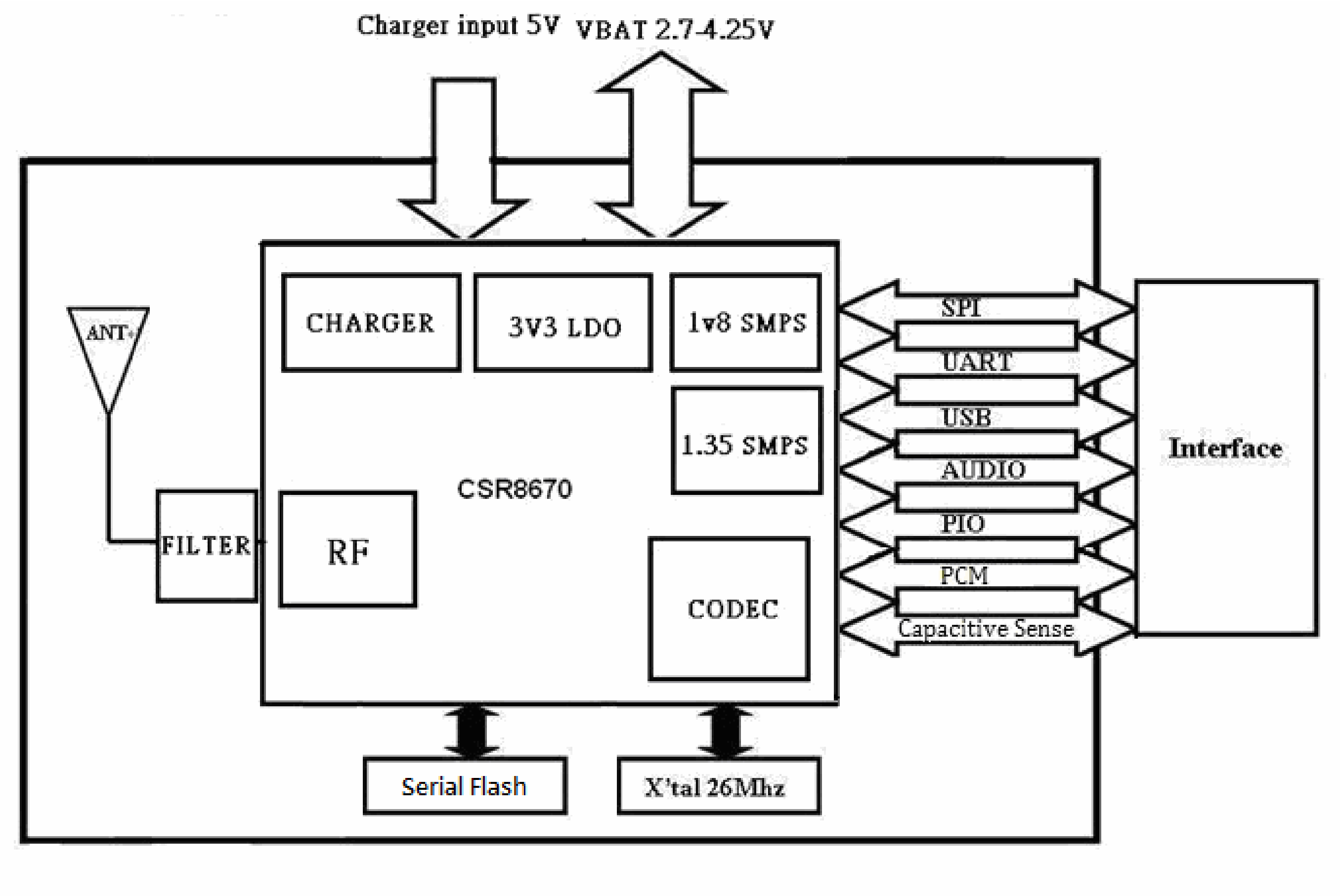
(b) The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Supply voltage, VDD_DAC	1.30	1.35	1.40	V
Output voltage range	0	-	1.35	V
Full-scale output voltage	1.30	1.35	1.40	V
LSB size	0	1.32	2.64	mV
Offset	-1.32	0	1.32	mV
Integral non-linearity	-1	0	1	LSB
Settling time(a)	-	-	250	ns

(a) The settling time does not include any capacitive load

Block Diagram



RF Specification: Temperature=+20℃

Transmitter

	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power	-6	2	-	-6 to +4	dBm
RF power variation over temperature range with compensation enabled	-	±0.5	-	-	dB
RF power variation over temperature range with compensation disabled	-	±1.5	-	-	dB
20dB bandwidth for modulated carrier	-	925	1000	≤1000	kHz
Adjacent channel transmit power F = F0 ± 2MHz	-	-23	-20	≤-20	dBm
Adjacent channel transmit power F = F0 ± 3MHz	-	-32	-28	≤-40	dBm
Adjacent channel transmit power F = F0 ± > 3MHz	-	-65	-40	≤-40	dBm
Δf1avg Maximum Modulation	140	165	175	140<f1avg<175	kHz
Δf2max Minimum Modulation	115	137	-	≥115	kHz
Δf2avg/Δf1avg	0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-75	15	75	±75	kHz
Drift Rate	-	5	20	≤20	kHz/50µ
Drift (single slot packet)	-	15	25	≤25	kHz
Drift (five slot packet)	-	15	40	≤40	kHz
2nd Harmonic Content	-	-40	-	≤-30	dBm
3rd Harmonic Content	-	-55	-	≤-30	dBm

Receiver

	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-87	-83	≤-70	dBm
	2.441	-	-90	-86		
	2.480	-	-90	-86		
Maximum received signal at 0.1% BER		-20	>-10	-	≥-20	dBm
C/I co-channel		-	5	11	≤11	dB
Adjacent channel selectivity C/I F = F0 + 1MHz		-	-5	0	≤0	dB
Adjacent channel selectivity C/I F = F0 - 1MHz		-	-3	0	≤0	dB
Adjacent channel selectivity C/I		-	-35	-30	≤-30	dB

F = F0 + 2MHz					
Adjacent channel selectivity C/I F = F0 - 2MHz	-	-25	-20	≤-20	dB
Adjacent channel selectivity C/I F = F0 + 3MHz	-	-45	-40	≤-40	dB
Adjacent channel selectivity C/I F = F0 - 5MHz	-	-45	-40	≤-40	dB
Adjacent channel selectivity C/I F = FImage	-	-20	-9	≤-9	dB
Maximum level of intermodulation interferers	-39	-23	-	≥-39	dBm
Spurious output level	-	-155	-		dBm/Hz

BTM-860 Pin Functions

No.	Pin Name	Pin Type	Supply Domain	Pin Description
1.	GND	GND		Common Ground
2.	AIO1	Bi-directional	VDD_AUX(1.35V)	Analogue programmable input/output line
3.	AIO0	Bi-directional	VDD_AUX(1.35V)	Analogue programmable input/output line
4.	CAP_SENSE_0	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Capacitive touch sensor input
5.	CAP_SENSE_1	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Capacitive touch sensor input
6.	CAP_SENSE_2	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Capacitive touch sensor input
7.	CAP_SENSE_3	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Capacitive touch sensor input
8.	CAP_SENSE_4	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Capacitive touch sensor input
9.	CAP_SENSE_5	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Capacitive touch sensor input
10.	SD_IN & SPDIF_IN	Bidirectional with weak pull-down	PIO_POWER	I2S Interface & SPDIF Interface Synchronous data output. Alternative function PIO_17.
11.	SD_OUT & SPDIF_OUT	Bidirectional with weak pull-down	PIO_POWER	I2S Interface & SPDIF Interface Synchronous data output. Alternative function PIO_18.
12.	WS	Bidirectional with weak	PIO_POWER	I2S Interface Synchronous data output.

		pull-down		Alternative function PIO_19.
13.	SCK	Bidirectional with weak pull-down	PIO_POWER	I2S Interface Synchronous data output. Alternative function PIO_20.
14.	SPI_CLK	Input with strong pull-down	PIO_POWER	SPI clock
15.	SPI_MOSI	Input with weak pull-down	PIO_POWER	SPI data input
16.	SPI_MISO	Output with strong pull-up	PIO_POWER	SPI data output
17.	SPI_CS#	Input with weak pull-down	PIO_POWER	Chip select for SPI, active low
18.	RESET	Input with strong pull-up	PIO_POWER	Reset if low. Pull low for minimum 5ms to cause a reset
19.	UART_RX	Bi-directional strong pull-up	PIO_POWER	UART data input
20.	GND	GND		Common Ground
21.	UART_TX	Bi-directional weak pull-up	PIO_POWER	UART data output
22.	LED0	Open drain output	PIO_POWER	LED Driver
23.	LED1	Open drain output	PIO_POWER	LED Driver
24.	LED2	Open drain output	PIO_POWER	LED Driver
25.	PIO0	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
26.	PIO1	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
27.	PIO2	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
28.	PIO3	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
29.	PIO4	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
30.	PIO5	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
31.	PIO6	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
32.	PIO7	Bi-directional with weak pull-down	PIO_POWER	Programmable input / output line
33.	USB_DP	Bi-directional	3V3_USB	USB data plus
34.	USB_DN	Bi-directional	3V3_USB	USB data minus
35	PIO_POWER	VDD		Positive supply for PIO

36.	GND	GND		Common Ground
37.	1V8_SMPS	VDD		1V8 Output
38.	VBAT	Battery terminal +ve		Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator
39.	VBAT_SENSE			Battery charger sense input
40.	VCHG	Charger input		Lithium ion/polymer battery charger input
41.	CHG_EXT			External charger control. Otherwise leave unconnected.
42.	VREG_ENABLE	Analogue		Regulator enable input
43.	UART_CTS	Bi-directional weak pull-down	PIO_POWER	UART clear to send, active low.
44.	UART_RTS	Bi-directional weak pull-up	PIO_POWER	UART request to send, active low. Alternative function PIO[16].
45.	MIC_LN	Analogue	VDD_AUDIO(1.35V)	Microphone input negative, left
46.	MIC_LP	Analogue	VDD_AUDIO(1.35V)	Microphone input positive, left
47.	MIC_BIAS_A	Analogue	VBAT/3V3_USB	Microphone bias A
48.	MIC_RN	Analogue	VDD_AUDIO(1.35V)	Microphone input negative,right
49.	MIC_RP	Analogue	VDD_AUDIO(1.35V)	Microphone input positive, right
50.	MIC_BIAS_B	Analogue	VBAT/3V3_USB	Microphone bias B
51.	SPKR_RN	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output negative, right
52.	SPKR_RP	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output positive, right
53.	SPKR_LN	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output negative, left
54.	SPKR_LP	Analogue	VDD_AUDIO_DRV (1V8_SMPS)	Speaker output positive, left
55.	GND	GND		Common Ground

1. Serial Interface

1.1 USB Interface

BTM-860 has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices.

The USB interface on BTM-860 acts as a USB peripheral, responding to requests from a master host controller.

BTM-860 contains internal USB termination resistors and requires no external resistor matching.

BTM-860 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification), supports USB standard charger detection and fully supports the USB Battery Charging Specification , available from http://www.usb.org. For more information on how to integrate the USB interface on BTM-860 see the Bluetooth and USB Design Considerations Application Note.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

1.2 Programming and Debug Interface

BTM-860 provides a debug SPI interface for programming, configuring (PS Keys) and debugging the BTM-860. Access to this interface is required in production. Ensure the 4 SPI signals and the SPI line are brought out to either test points or a header. To use the SPI interface, the SPI line requires the option of being pulled high externally.

2. interfaces

2.1 Analogue I/O Ports, AIO

BTM-860 has 2 general-purpose analogue interface pin, AIO[0] & AIO[1]. Typically, this connects to a thermistor for battery pack temperature measurements during charge control.

2.2 LED Drivers

BTM-860 includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

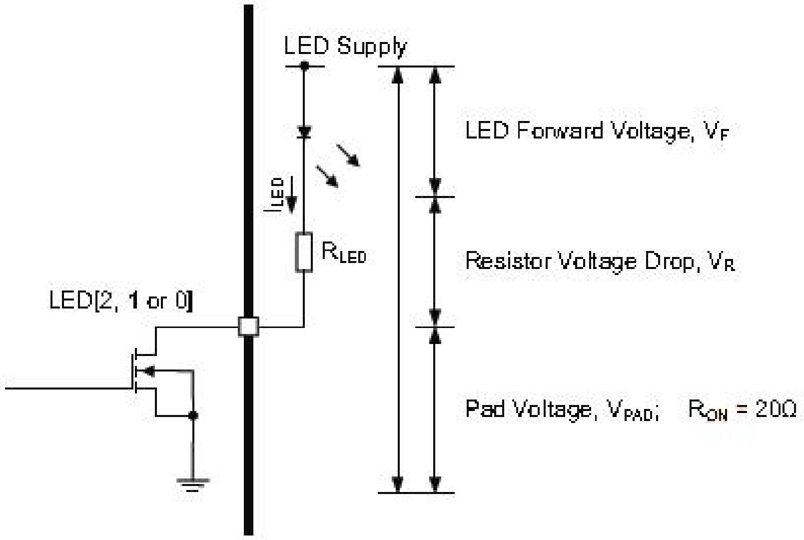


Figure 2.1: LED Equivalent Circuit

From Figure 2.1 it is possible to derive Equation 2.1 to calculate ILED. If a known value of current is required through the LED to give a specific luminous intensity, then the value of RLED is calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 2.1: LED Current

For the LED pads to act as resistance, the external series resistor, RLED, needs to be such that the voltage drop across it, VR, keeps VPAD below 0.5V. Equation 2.2 also applies.

$$VDD = VF + VR + VPAD$$

Equation 2.2: LED PAD Voltage

Note:

The LED current adds to the overall current. Conservative LED selection extends battery life.

3. Power Control and Regulation

3.1 Voltage Regulator Enable

When using the integrated regulators the voltage regulator enable pin, VREG_ENABLE, enables the BTM-860 and the following regulators:

- ■ 1.8V switch-mode regulator
- ■ 1.35V switch-mode regulator
- ■ Low-voltage VDD_DIG linear regulator
- ■ Low-voltage VDD_AUX linear regulator

The VREG_ENABLE pin is active high.

BTM-860 boots-up when the voltage regulator enable pin is pulled high, enabling the regulators. The firmware then latches the regulators on, it is then permitted to release the voltage regulator enable pin.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

3.2 Reset, RST#

BTM-860 is reset from several sources:

- ■ RST# pin
- ■ Power-on reset
- ■ USB charger attach reset
- ■ Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. Rayson recommends applying RST# for a period >5ms.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

4. Battery Charger

4.1 Battery Charger hardware Operating Modes

The battery charger hardware is controlled by the VM. The battery charger has 5 modes:

- ■ Disabled
- ■ Trickle charge
- ■ Fast charge
- ■ Standby: fully charged or float charge
- ■ Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current.

The internal charger circuit can provide up to 200mA of charge current, for currents higher than this the BTM-860 can control an external pass transistor

4.2 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, Rsense, connected in series with the external pass device, see Figure 4.2.1. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across Rsense is typically 200mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

In Figure 4.2.1, R1 (220mΩ) and C1 (4.7μF) form a RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be <1.0Ω

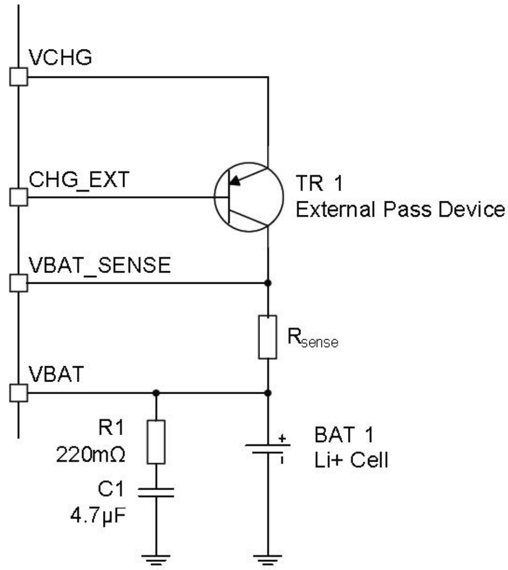


Figure 4.2.1: Battery Charger External Mode Typical Configuration

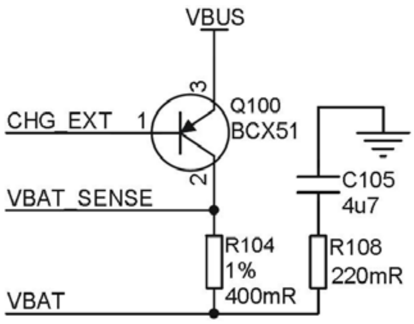


Figure 4.2.2: Optional Ancilliary Circuits

In Figure 4.2.2, Optional fast charge,400mΩ = 500m. Connect VBAT_SENSE to VBAT if not using this circuit.

5. Flash Memory

5.1 eFlash Memory

The internal flash memory provides 16Mb of internal code and data storage. For improved performance, the internal flash memory has 45ns access time and is organised as 64-bit wide.

5.2 Serial Quad I/O Flash (option)

BTM-860 supports serial flash. This enables additional data storage areas for device specific data. BTM-860 use the Serial Quad I/O Flash 4Mb Flash.

6. Capacitive Touch Sensor

BTM-860 capacitive touch sensor interface features:

■ Support for up to 6 capacitive touch sensing electrodes:

■ Printed on the PCB

■ Made from flex PCB

■ Configuration for individual buttons

■ Configuration for a wipe-type arrangement where 2 or more pads sense taps at each end or a wipe from one side to the other

■ Operates in deep sleep and is a programmable source for wake-up

Figure 6.1 shows the system block diagram for the capacitive touch sensor interface. The interface depends on the capacitive touch sensor type. Therefore the overall control of the capacitive touch sensor interface resides in the VM, so it is easily modified in each end-user application.

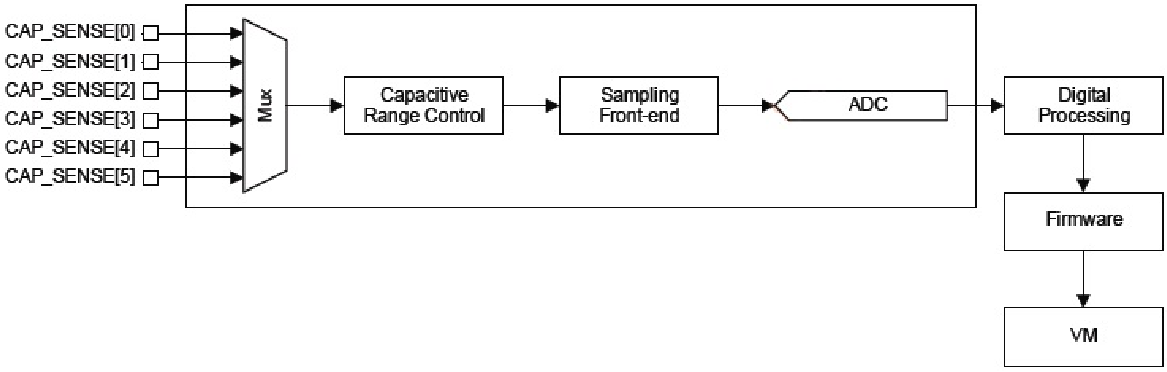


Figure 6.1: Capacitive Touch Sensor Block Diagram

The overall system-level specification for the capacitive touch sensor interface on the BTM-860 Module is:

■ 6 inputs multiplexed in to 1 touch sensor on the front-end

■ Capacitances of 0pF to 50pF measured with a resolution of 4fF, where a touch is assumed to be between ±50fF and ±1pF

■ Each reading takes 172µs:

■ 6 pads read every 1.03ms

■ System auto-calibrates to remove parasitic and environmental effects including:

■ PCB construction

■ Temperature

■ Humidity

■ Works in normal and deep sleep modes

■ System current is approximately 50µA from the battery

■ The touch sensor also functions like a PIO

The system block diagram in Figure 6.1 highlights the top-level architecture for the capacitive touch sensor interface, it consists of:

■ Capacitive range control:

■ Sets the rough capacitance of the touch sensor pad, which is product dependent

■ Splits into 4 integrated capacitors

■ The VM selects which capacitors are enabled, i.e. the range capacitance

■ Sampling front end:

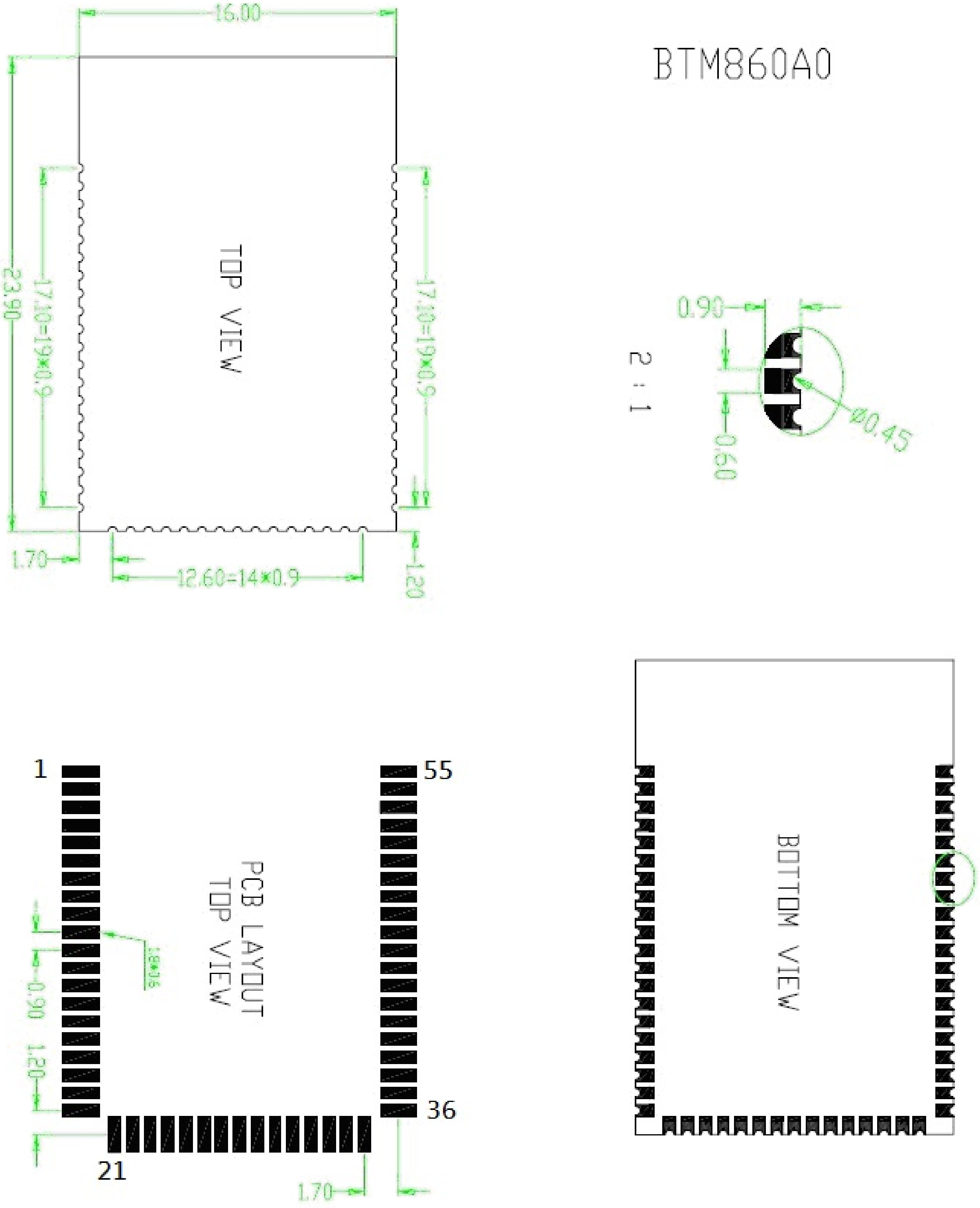
■ An internal capacitance is trimmed by the digital state machine ensuring:

■ Touch Capacitance = Range Capacitance + Internal Capacitance

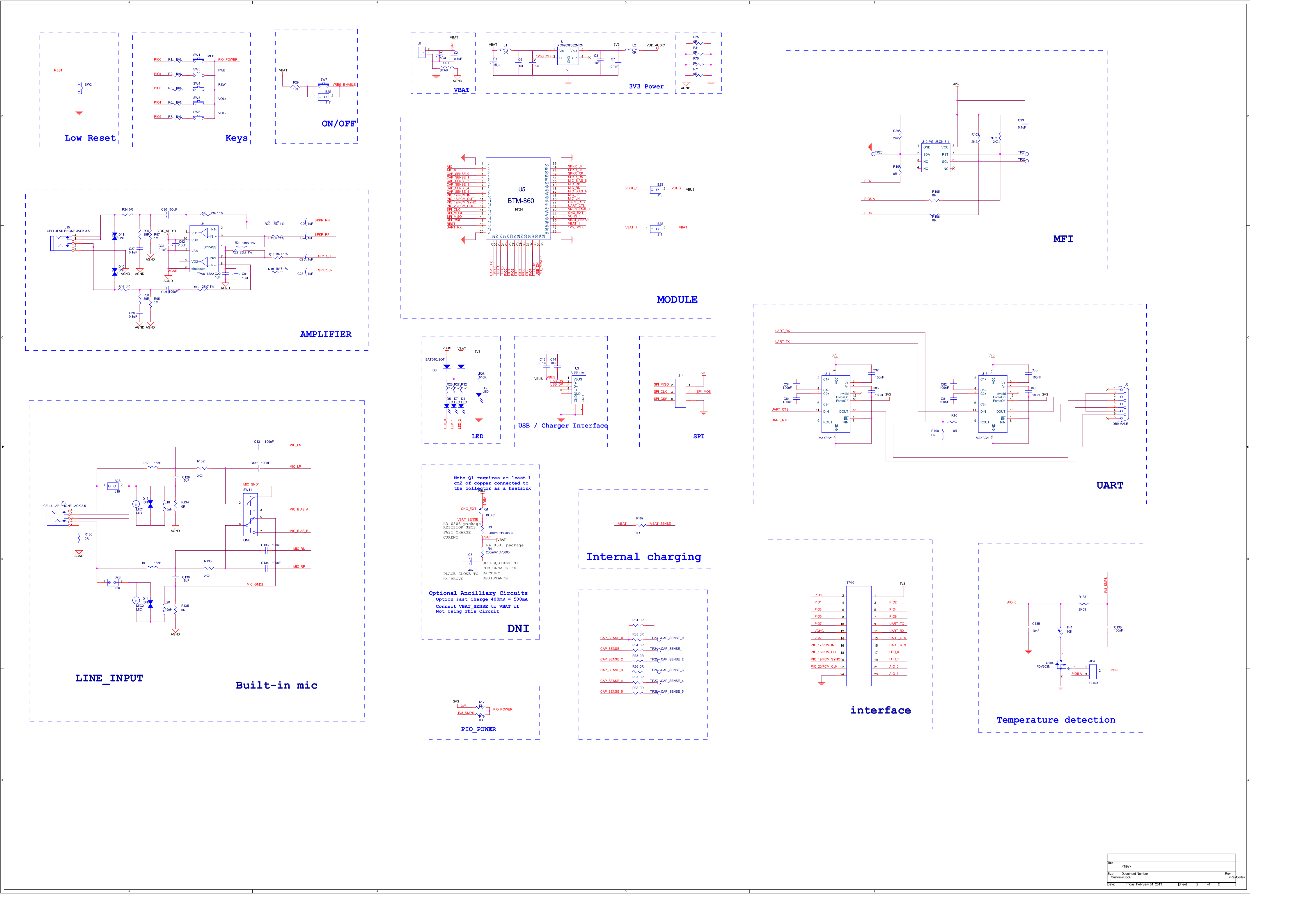
■ When the internal capacitance is correctly trimmed:

■ The sense voltage is 0V
■ A touch changes the touch capacitance, which then changes the sense voltage
■ ADC:
■ Uses a successive approximation, charge redistribution ADC
■ Clocked at 64kHz
■ 9-bit resolution, where LSB is ±2fF and full range is ±1pF
■ The internal capacitance is a 7-bit variable capacitor with 114fF steps and 14.5pF range
■ The internal capacitance is trimmed, putting it in the mid range of the ADC. This enables measurements from 0pF to 50pF, where a capacitive touch is between ±50fF and ±1pF.
■ Digital signal conditioning:
■ Only the enabled inputs are scanned
■ Enabling fewer inputs increases readings per second
■ Averaging of ADC readings reduces noise, this is software programmable from 1 to 64 readings in intervals to the power of 2
■ The internal capacitance updates using a rolling average of the ADC readings, software programmable from 1 to 215 readings in intervals to the power of 2. For example, 32768 readings take approximately:
■ 5.6s if polling one pad (no averaging)
■ 33.8s if polling 6 pads (no averaging)
■ Pulse skipping mode is possible, reducing the current consumption. Here the system waits a programmable number of 64kHz clock cycles (maximum 29) before the next read, i.e. an 8ms maximum pause.
■ ADC trigger level is software programmable. If the threshold is crossed the firmware gets an interrupt.
■ 6 hardware event registers store the pad number and trigger time, which enables the system to sense swipes.
■ Programmable hysteresis, with one value for all pads
■ Software signal conditioning (firmware):
■ The firmware reads ADC and Cint values after an interrupt as the hardware only stores the pad number and trigger time
■ Digital state machine scans pads and calibrates the internal capacitance
■ If a swipe happens in deep sleep the firmware reads the trigger order and event time when it wakes up. It then reads the last ADC reading for each input, not the reading that triggered the interrupt.
■ VM:
■ Configures the hardware and gets an interrupt when a programmable threshold is crossed
■ Selects the range capacitance
■ Decides whether an event is a valid touch

7. Dimension



16.00
BTM860A0
23.90
17.10=19*0.9
TOP VIEW
0.90
0.60
2 : 1
Ø0.45
1.70
12.60=14*0.9
1.20
1
55
PCB LAYOUT
TOP VIEW
BOTTOM VIEW
0.90
1.20
36
21
1.70


Low Reset
Keys
ON/OFF
VBAT
3V3 Power
MFI
MODULE
U5
BTM-860
AMPLIFIER
LED
USB / Charger Interface
SPI
UART
Note Q1 requires at least 1 cm2 of copper connected to the collector as a heatsink
R3 0805 package RESISTOR SETS FAST CHARGE CURENT
R4 0603 package
RC REQUIRED TO COMPENSATE FOR BATTERY RESISTANCE
PLACE CLOSE TO R4 ABOVE
Optional Ancilliary Circuits
Option Fast Charge 400mA = 500mA
Connect VBAT_SENSE to VBAT if Not Using This Circuit
DNI
Internal charging
LINE_INPUT
Built-in mic
PIO_POWER
interface
Temperature detection
Title <Title>
Size Custom
Document Number <Doc>
Rev <RevCode>
Date: Friday, February 01, 2013
Sheet 2 of 2