BTM52

Bluetooth Module Data Sheet

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Revision History

Date	Version	Description	Author
2012-03-14	V1.0	■ First Release	
2012-04-20	V1.01	■ Add to support A2DP Codes	

CONTENT

1. INTRODUCTION

The BTM52 Bluetooth® module is a perfect solution for enhanced audio applications, such as stereo headphones and high performance automobile handsfree. It can be connected with any Bluetooth® devices in an operating range. It is slim and light so the designers can have better flexibilities for the product shapes.

The BTM52 Bluetooth® module complies with Bluetooth® specification version 2.1. It supports HSP, HFP, A2DP, AVRCP, PBAP, SPP, profiles. It integrates RF Baseband controller, antenna, etc. and provides UART interface, programmable I/O, stereo speaker output, microphone input, etc.

The detail information of BTM52 Bluetooth® module is presented in this document below.

1.1 Block Diagram

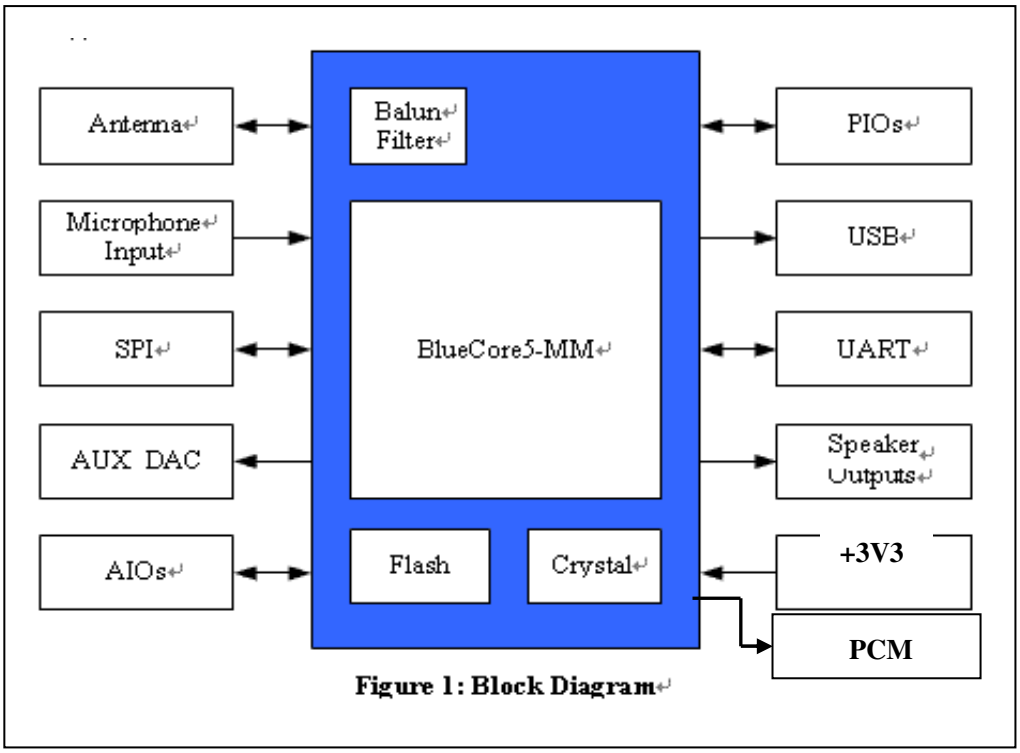


Figure 1: Block Diagram

1.2 Features

- ✓ Small overall dimension(15mm x 20mm x 2mm)
- ✓ Bluetooth Specification V2.1
- ✓ Class 2 and Class 3 support
- ✓ Physical connection as SMD type
- ✓ DSP Co-Processor 16-bit Internal Stereo CODEC with -95dB SNR for DAC.
- ✓ High quality stereo audio (sample rate up to 44.1KHz)
- ✓ Supports A2DP Codecs: SBC(**mandatory**); MPEG-1,2 Audio / MPEG-2,4 AAC / ATRAC family / APTX (**optional**)
- ✓ Built-in RF combo filter, Integrated 26M Crystal.
- ✓ Supports up to 8 Mbits/16 Mbits on module flash memory.
- ✓ Support phonebook download from mobile phones to serial flash.
- ✓ Support phonebook sorting and searching.
- ✓ Support DFU for firmware upgrade.
- ✓ Support DUN for internet access.
- ✓ Support active inquires BT device and pairing.
- ✓ Support HSP, HFP, A2DP, AVRCP, OPP, SPP, PBAP, SYNC, PB-Sync for Nokia, PB-Sync For Samsung profile.
- ✓ Support active inquires BT device and pairing.
- ✓ Support customizable PIN code and device name.
- ✓ Support pairing up to 8 Bluetooth® device.
- ✓ Compatible with CSR cVc software echo cancellation solution.
- ✓ No radio signal interference, support for 802.11 co-existence

※ ***Some features are optional for customization on demand.***

1.3 Application

- ✓ Automobile hands-free applications
- ✓ Hands-Free Car Kits for embedded Car audio systems
- ✓ Bluetooth Audio source gateway and data gateways for PND systems
- ✓ High Quality Stereo Bluetooth Headsets
- ✓ High Quality Mono Bluetooth Headsets
- ✓ Bluetooth Speakers
- ✓ Industrial sensors and controls
- ✓ Measurement and monitoring systems

2. GENERAL SPECIFICATION

Bluetooth Specification	
Chip Set	CSR BC05-MultiMedia External
Module ID	BTM52
BT Standard	Bluetooth® V2.1 + EDR specification
RF TX Output Power	4dBm (Class II)
Sensitivity	-86dBm@0.1%BER
Frequency Band	2.402GHz~2.480GHz ISM Band
Baseband Crystal OSC	26MHz
Hopping	1600hops/sec, 1MHz channel space
RF Input Impedance	50 ohms
Major Interface	• Microphone : Input (Differential) • Speaker : Output (Differential) • PCM : Output • UART : Tx/Rx • USB : DP/DN • PIOs • Antenna
Profile	HSP, HFP, A2DP, AVRCP, PBAP, …….. detailed profiles depends on the firmware
Voice Processor	64MIPS Kalimba with cVc support
Power	
Supply Voltage	3.0V ~ 3.6V DC
Working Current	35mA typical, Depends on profiles
Standby Current	<1mA
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Environmental	RoHS Compliant

3. PHYSICAL CHARACTERISTIC

Dimension:

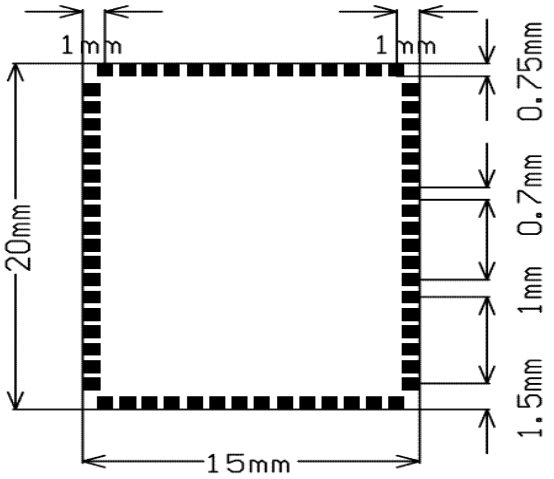


Figure 2

Top View:

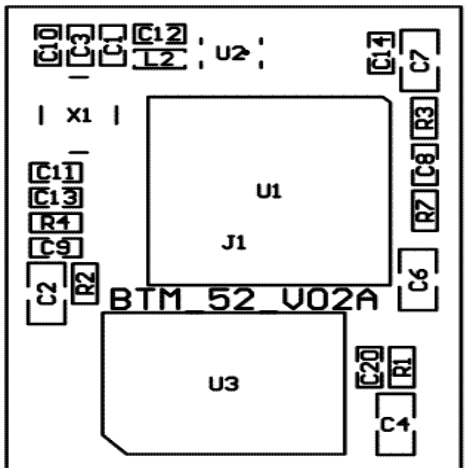


Figure 3

Pin Definition:

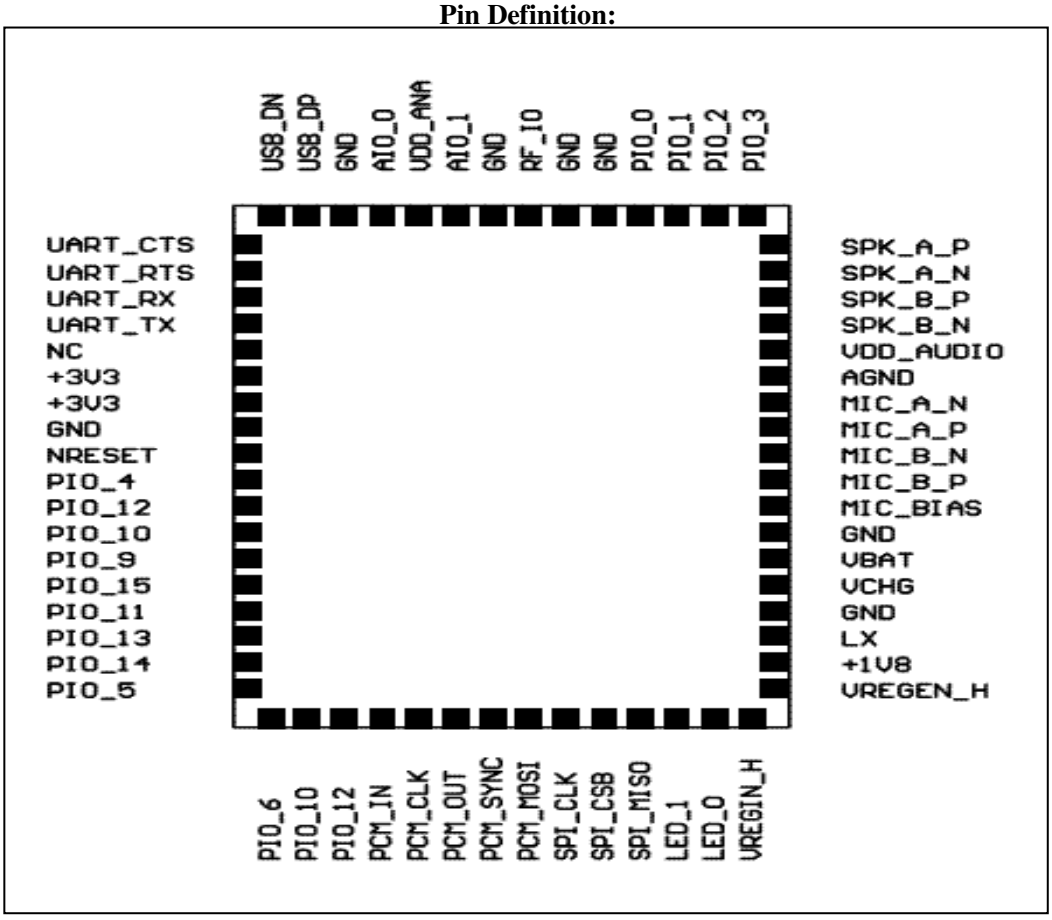


Figure 4

3.1 Pin Description

Pin#	Pin Name	Pad Type	Description
1	UART_CTS	CMOS input with weak internal pull-down	UART clear to send active low
2	UART_RTS	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART request to send active low
3	UART_RX	CMOS input with weak internal pull-down	UART data input
4	UART_TX	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART data output
5	NC	NC	NC
6	+3V3	VDD	Positive supply for BT Module (3.2V~3.6V)
7	+3V3	VDD	Positive supply for BT Module(3.2V~3.6V)
8	GND	Ground	Digital Ground
9	NRESET	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
10	PIO[4]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
11	PIO[12]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
12	PIO[10]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
13	PIO[9]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
14	PIO[15]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
15	PIO[11]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
16	PIO[13]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line

17	PIO[14]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
18	PIO[5]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
19	PIO[6]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
20	PIO[10]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
21	PIO[12]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
22	PCM_IN	CMOS input, with weak internal pull-down	Synchronous data input
23	PCM_CLK	Bi-directional with weak internal pull-down	Synchronous data clock
24	PCM_OUT	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
25	PCM_SYNC	Bi-directional with weak internal pull-down	Synchronous data sync
26	SPI_MOSI	CMOS input, with weak internal pull-down	SPI data input
27	SPI_CLK	Input with weak internal pull-down	SPI clock
28	SPI_CSB	Input with weak internal pull-up	Chip select for Serial Peripheral Interface (SPI),active low
29	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	SPI data output
30	LED[1]	Open drain output	LED driver

31	LED[0]	Open drain output	LED driver
32	VREGIN_H	Regulator input	Input to internal high-voltage linear regulator (2.5V~4.9V)
33	VREGEN_H	Analogue	Take high to enable high-voltage linear regulator and switch-mode regulator
34	+1V8	Supply	High-voltage linear regulator output (1.8V out)
35	LX	Switch-mode power regulator output	Switch-mode power regulator output (1.8V out)

36	GND	Ground	Digital Ground
37	VCHG	Charger input	Lithium ion/polymer battery charger input (4.5V~6.5V)
38	VBAT	Battery terminal +ve	Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator (4.2V out)
39	GND	Ground	Digital Ground
40	MIC_BIAS	Analogue	Microphone bias
41	MIC_B_P	Analogue	Microphone input positive, right
42	MIC_B_N	Analogue	Microphone input negative, right
43	MIC_A_P	Analogue	Microphone input positive, left
44	MIC_A_N	Analogue	Microphone input negative, left
45	AGND	Ground	Analogue Ground
46	VDD_AUDIO	Bi-directional VDD/Low-voltage regulator output	Analogue programmable input/ output line circuitry and 1.5V regulated output (from internal low-voltage regulator)
47	SPK_B_N	Analogue	Speaker output negative, right

48	SPK_B_P	Analogue	Speaker output positive, right
49	SPK_A_N	Analogue	Speaker output negative, left
50	SPK_A_P	Analogue	Speaker output positive, left
51	PIO[3]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
52	PIO[2]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line (external TXEN)
53	PIO[1]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line

54	PIO[0]	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line (external RXEN)
55	GND	Ground	Digital Ground
56	GND	Ground	Digital Ground
57	RF_IO	RF	RF out
58	GND	Ground	Digital Ground
59	AIO[1]	Bi-directional	Analogue programmable input/ output line
60	AIO[1] VDD_ANA	Bi-directional VDD/Low-voltage regulator output	Analogue programmable input/ output line circuitry and 1.5V regulated output (from internal low-voltage regulator)
61	AIO[0]	Bi-directional	Analogue programmable input/ output line
62	GND	Ground	Digital Ground
63	USB_DP	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
64	USB_DN	Bi-directional	USB data minus

4. REFERENCE SCHEMATIC

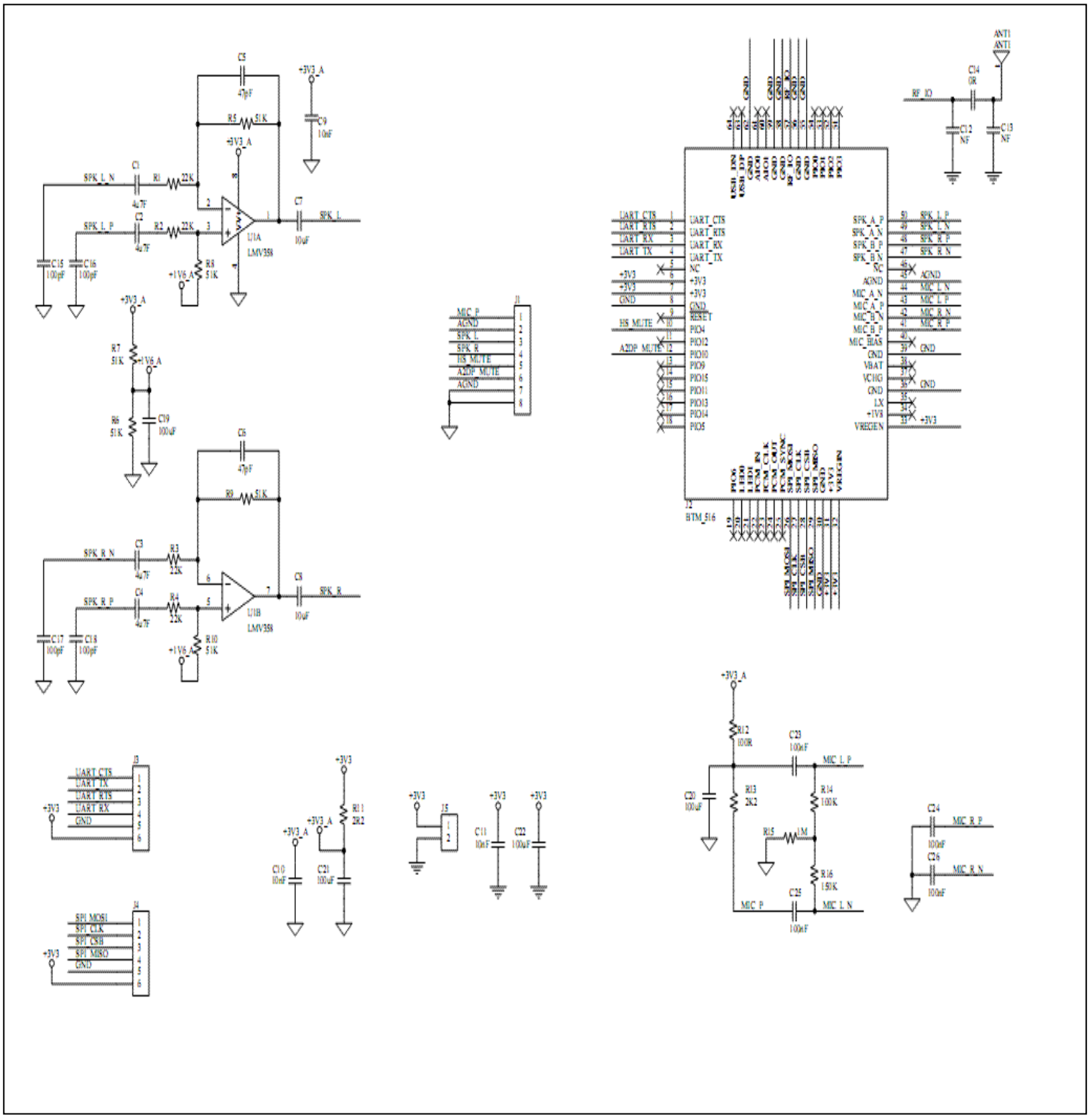


Figure 5

5. PHYSICAL INTERFACE

5.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less.

5.2 Reset

The module may be reset from several sources: NRESET pin, power-on reset, a UART break character or via a software configured watchdog timer.

The NRESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active.
It is recommended that RESETB be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

5.3 Audio Interfaces

Audio interface as following features:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

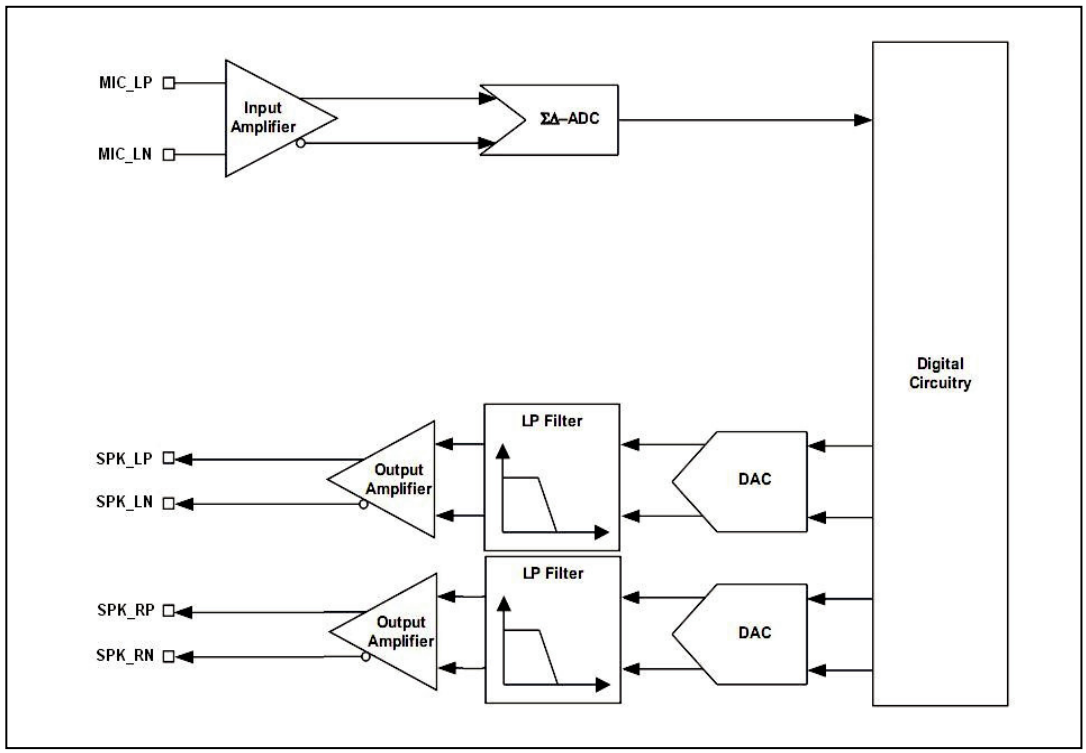


Figure 6

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It uses a minimum of external components.The module features a differential stereo audio output interfaces.

5.3.1 ADC

The ADC consists of a second order Digma Delta converter as show in **Figure 6.**

5.3.2 ADC Sample Rate Selection and Warping

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz,44.1kHz.

One of the main concerns for stereo wireless music applications is the ability to keep sampl rates forthe CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of $1/2^{17}$, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

5.3.3 ADC Gain

The ADC contains two gain stages for each channel, an analogue and a digital gain stage.

5.3.4 DAC

The DAC contains two second order Sigma Delta converters allowing two separate channels that are identical in functionality as show in **Figure 6**.

5.3.5 DAC Sample Rate Selection and Warping

Each DAC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz,44.1kHz, 48kHz.

One of the main concerns for the DAC used in stereo wireless music applications is the ability to keep sampl rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of $1/2^{17}$, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

5.3.6 DAC Gain

The DAC contains two gain stages for each channel, a digital and an analogue gain stage.

5.3.7 Mono Operation

Mono operation is single channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is auxiliary mono channel that may be used in dual mono channel operation.

5.3.8 Audio Input Stage

The audio input stage of the module consists of a low noise input amplifier, which receives its analogue input signal from pins MIC_A_P and MIC_A_N to a second–order ∑-Δ ADC that outputs a 4Mbit/sec single-bit stream into the digital circuitry. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

5.3.9 Microphone Input

Check the reference design in **Figure 5** for the microphone input design.

5.3.10 Audio Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/sec multi-bit stream, which is fed into the analogue output circuitry.
The output circuit comprises a digital to analogue converter with gain setting and output amplifier.Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk- differential into a load of 16Ω. The output is available as a differential signal between SPK_A_P and SPK_A_N for the left channel; and between SPK_B_P and SPK_B_N for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω if only one channel is connected or an external regulator is used.

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The multi-bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

5.3.11 PCM

The audio pulse code modulation (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels.Through its PCM interface, BTM52 provide hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications.BTM52offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BTM52 allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any time.

5.4 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

5.5 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

5.6 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

5.7 Serial Interfaces

5.7.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device,UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

5.7.2 USB

There is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The module features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with section7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD =3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and DP on the USB cable.

5.7.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

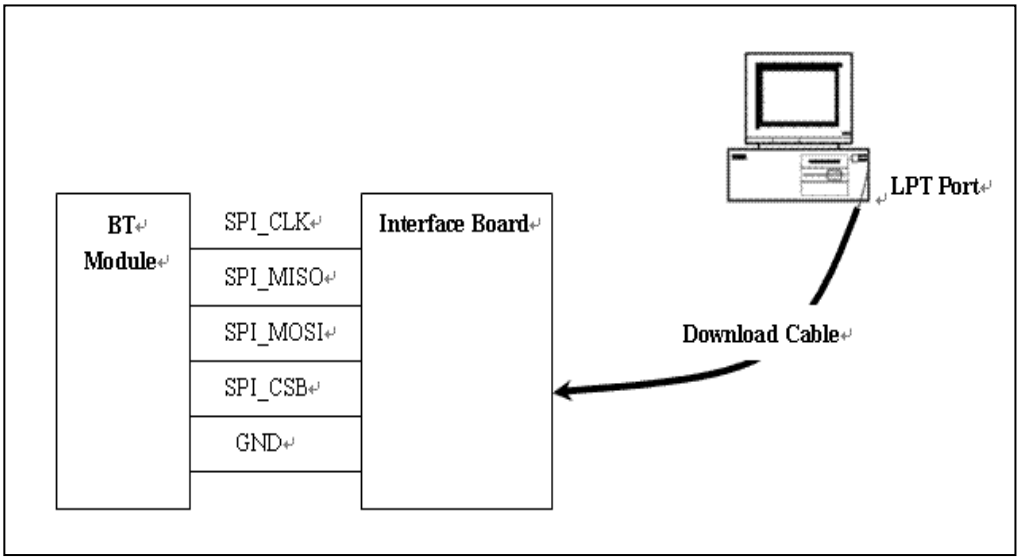


Figure 7

6. ELECTRICAL CHARACTERISTIC

6.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+125	℃
Operating Temperature	-40	+85	℃
PIO/AIO Voltage	-0.4	+3.6	V
+3V3 Voltage	-0.4	+3.6	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	3V3+0.4	V

Table 1

6.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Operating Temperature Range	-40	--	+85	℃
+3V3 Voltage	+3.0	+3.3	+3.6	V

Table 2

6.3 Input/output Terminal Characteristics

6.3.1 Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.3	-	+0.25x3V3	V
VIH input logic level high	0.625*3V3	-	3V3+0.3	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75x3V3	-	0.625x3V3	V
Input and Tri-state Current				
Ii input leakage current at Vin=+3V3 or 0V	-100	0	100	nA
Ioz tri-state output leakage current at Vo=+3V3 or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	µA
With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	0. 2	+1. 0	5.0	µA
I/O pad leakage current	-1	0	+1	µA

CI Input Capacitance	1.	-	5.0	pF
Resistive Strength				
Rpuw weak pull-up strength at +3V3-0.2V	500k	-	2M	Ω
Rpdw weak pull-up strength at 0.2V	500k	-	2M	Ω
Rpus strong pull-up strength at +3V3-0.2V	10k	-	50k	Ω
Rpds strong pull-up strength at 0.2V	10k	-	50k	Ω

Table 3

6.3.2 USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3*3V3	V
V_{IH} input logic level high	0.7*3V3	-	-	V
Input Leakage Current				
GND < VIN < +3V3[(a)]	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{IL} output logic level low	0.0	-	0.2	V
V_{IH} output logic level high	2.8	-	+3V3	V

Table 4

6.3.3 Internal CODEC - Analogue to Digital Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Input Sample Rate	8	-	44.1	kHz
Signal / Noise, f_{in}=1kHz, BW=20Hz->20kHz A-Weighted THD+N<1% 150mV Vpk-pk				
F_{sample} = 8kHz	-	82	-	dB
F_{sample} = 11.025kHz	-	81	-	dB
F_{sample} = 16kHz	-	80	-	dB
F_{sample} = 22.05kHz	-	79	-	dB
F_{sample} = 32kHz	-	79	-	dB
F_{sample} = 44.1kHz	-	78	-	dB
Digital Gain	-24	-	21.5	dB

Table 5

6.3.4 Internal CODEC - Digital to Analogue Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Output Sample Rate, Fsample	8	-	48	kHz
Signal / Noise, f_{in}=1kHz, BW=20Hz->20kHz A-Weighted THD+N<0.01% 0dBFS signal Load 100kΩ				
F_{sample} = 8kHz	-	95	-	dB
F_{sample} = 11.025kHz	-	95	-	dB
F_{sample} = 16kHz	-	95	-	dB
F_{sample} = 22.05kHz	-	95	-	dB
F_{sample} = 32kHz	-	95	-	dB
F_{sample} = 44kHz	-	95	-	dB
F_{sample} = 48kHz	-	95	-	dB
Digital Gain	-24	-	21.5	dB
Gain Resolution		1/32		dB

Table 6

6.3.5 Microphone Input

Microphone Input	Min	Typical	Max	Unit
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gian(differential)		800	-	mV rms
Gain	-3	-	42	dB
Gain resolution	-	3	-	dB
Distortion at 1kHz	-	-	-74	dB
3dB Bandwidth	-	20		kHz
Input impedance	-	6		kΩ
THD+N(microphone input)@30mV rms input	-	0.04	-	%

Table 7

6.3.6 Speaker Output

Speaker Driver	Min	Typical	Max	Unit
Output voltage full scale swing (differential)	-	750	-	mV rms
THD+N 100kΩ load	-	-	0.01%	%
THD+N 16Ω load	-	-	0.1%	%
SNR(Load=16Ω, 0dBFS input relative to	-	95	-	dB

Table 8

6.4 Power consumptions

Operating Condition	Min	Typical	Max	Unit
Connected Idle (Sniff 1.28 secs)		0.19		mA
Connected with audio streaming	30	35	40	mA
Deep Sleep Idle mode		60		uA

Table 9

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

2F Friday March 09, 2012 10:21:21

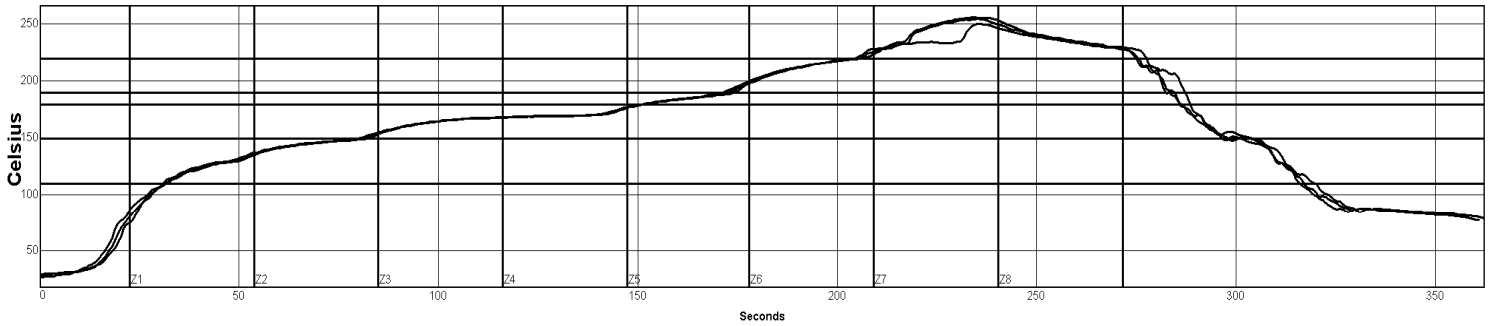
Site:

Oven Name: WQ Process Window Name: 无铅

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8
Top	140	150	170	170	190	225	265	230
Bottom	140	150	170	170	190	225	265	230

Conveyor Speed (cm/min): 75.0



PWI= 304%	Max Rising Slope		Preheat 110-190C		Soak Time 150-180C		Reflow Time /220C		Peak Temp	
2	3.9	189%	141.4	157%	70.4	-296%	71.1	111%	254.8	97%
3	4.0	197%	139.7	149%	70.6	-294%	70.3	103%	250.6	11%
4	3.9	192%	142.1	160%	69.6	-304%	71.2	112%	256.5	130%

Process Window:

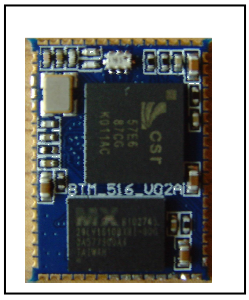
Solder Paste: SYSTEM DEFAULT

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.0)	0.0	3.0	Degrees/Second
Preheat Time 110-190C	90	130	Seconds
Soak Time 150-180C	90	110	Seconds
Time Above Reflow - 220C	50	70	Seconds
Peak Temperature	245	255	Degrees Celsius

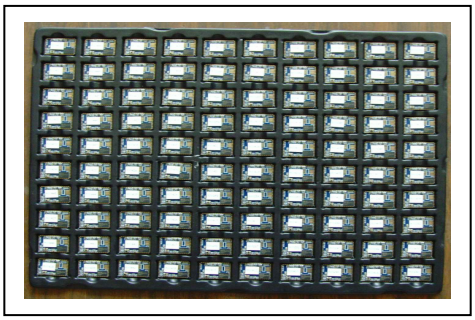
Description:

8. PACKAGING INFORMATION

1. BLUETOOTH® Module: BTM52



2. Assembly



3. Dimension