BTM521

Bluetooth Module Data Sheet

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Document Version:	V1.11
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Revision History

Date	Version	Description	Author
2012-03-14	V1.0	■ First Release	
2012-05-28	V1.1	■ Update Reference Schematic & Pin Definition	
2012-06-26	V1.11	■ Add UART Port Application Notes	

CONTENT

1. INTRODUCTION

The BTM521 Bluetooth® module is a perfect solution for enhanced audio applications, such as stereo headphones. It can be connected with any Bluetooth® devices in an operating range. It is slim and light so the designers can have better flexibilities for the product shapes.

The BTM521 Bluetooth® module complies with Bluetooth® specification version 2.1. It supports HSP, HFP, A2DP, AVRCP profiles. It integrates RF Baseband controller, antenna, etc. and provide UART interface, programmable I/O, stereo speaker output, microphone input,… etc.

The detail information of BTM521 Bluetooth® module is presented in this document below.

1.1 Block Diagram

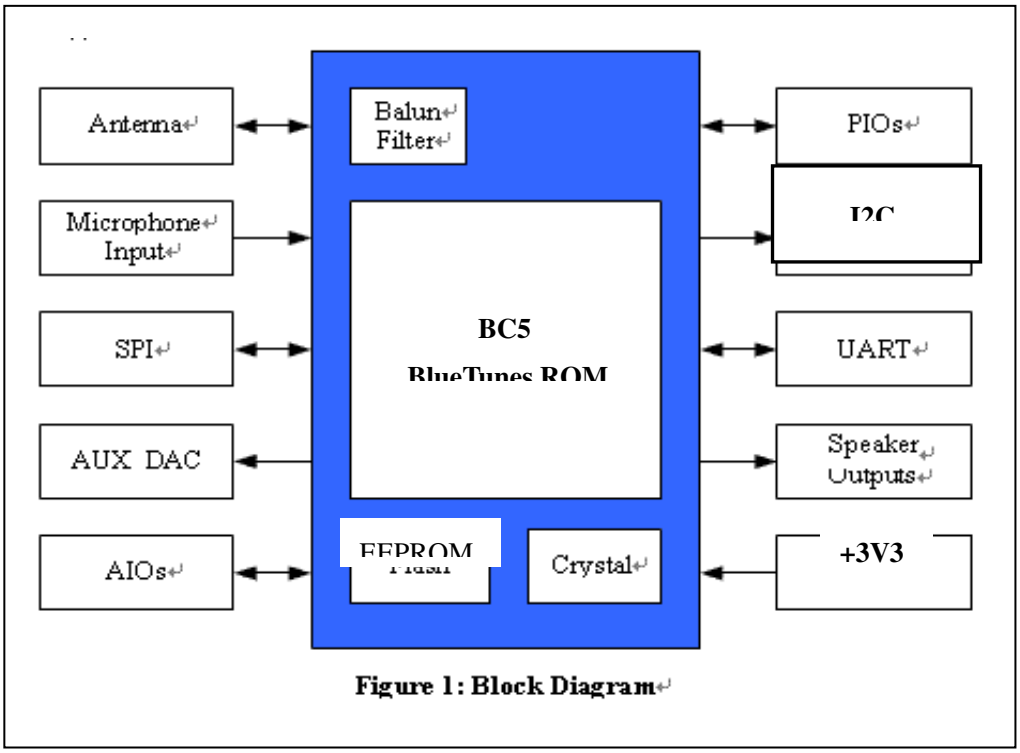


Figure 1: Block Diagram

1.2 Features

- ✓ Small overall dimension(17.6mm x 24mm x 2mm)
- ✓ Bluetooth Specification V2.1 + EDR
- ✓ Class 1, Class 2and Class 3 support
- ✓ Physical connection as SMD type
- ✓ DSP Co-Processor 16-bit Internal Stereo CODEC for DAC.
- ✓ High quality stereo audio
- ✓ Music Enhancements: SBC,MP3,FastStream(low-latency codec) and 5-band EQ
- ✓ Built-in RF combo filter, Integrated 26M Crystal.
- ✓ Support HSP, HFP, A2DP, AVRCP profile.
- ✓ Compatible with CSR cVc software echo cancellation solution.
- ✓ No radio signal interference, support for 802.11 co-existence

※ ***Some features are optional for customization on demand.***

1.3 Application

- ✓ High Quality Stereo Bluetooth Headsets
- ✓ High Quality Wired Stereo Headset and Headphones
- ✓ Bluetooth Speakers

2. GENERAL SPECIFICATION

Bluetooth Specification	
Chip Set	BC5(BlueTunes ROM)
Module ID	BTM521
BT Standard	Bluetooth® V2.1 + EDR specification
RF TX Output Power	4dBm (Class II)
Sensitivity	-82dBm@0.1%BER
Frequency Band	2.402GHz~2.480GHz ISM Band
Baseband Crystal OSC	26MHz
Hopping	1600hops/sec, 1MHz channel space
RF Input Impedance	50 ohms
Major Interface	• Microphone : Input (Differential) • Speaker : Output (Differential) • UART : Tx/Rx • PIOs • Antenna
Profile	HSP, HFP, A2DP, AVRCP
Voice Processor	64MIPS Kalimba with cVc support
Power	
Supply Voltage	3.3V ~ 4.2V DC
Working Current	35mA typical, Depends on profiles
Standby Current	<1mA
Operating Environment	
Temperature	-20ºC to +70ºC
Humidity	10%~90% Non-Condensing
Environmental	RoHS Compliant

3. PHYSICAL CHARACTERISTIC

Dimension:

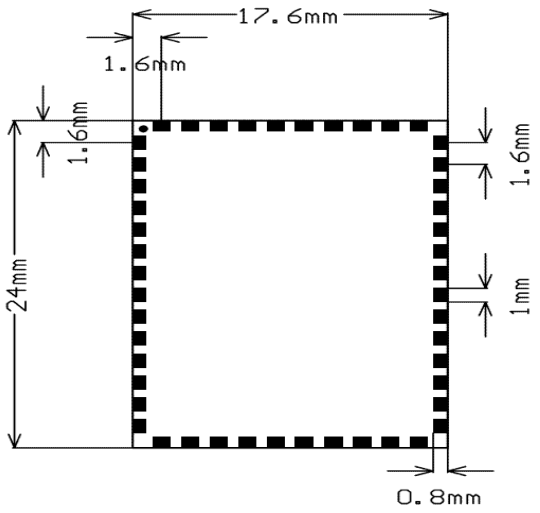


Figure 2

Top View:

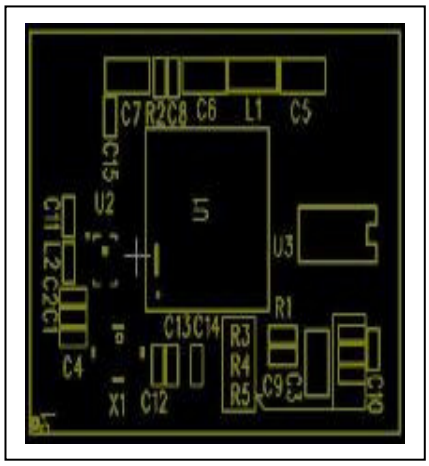


Figure 3

Pin Definition:

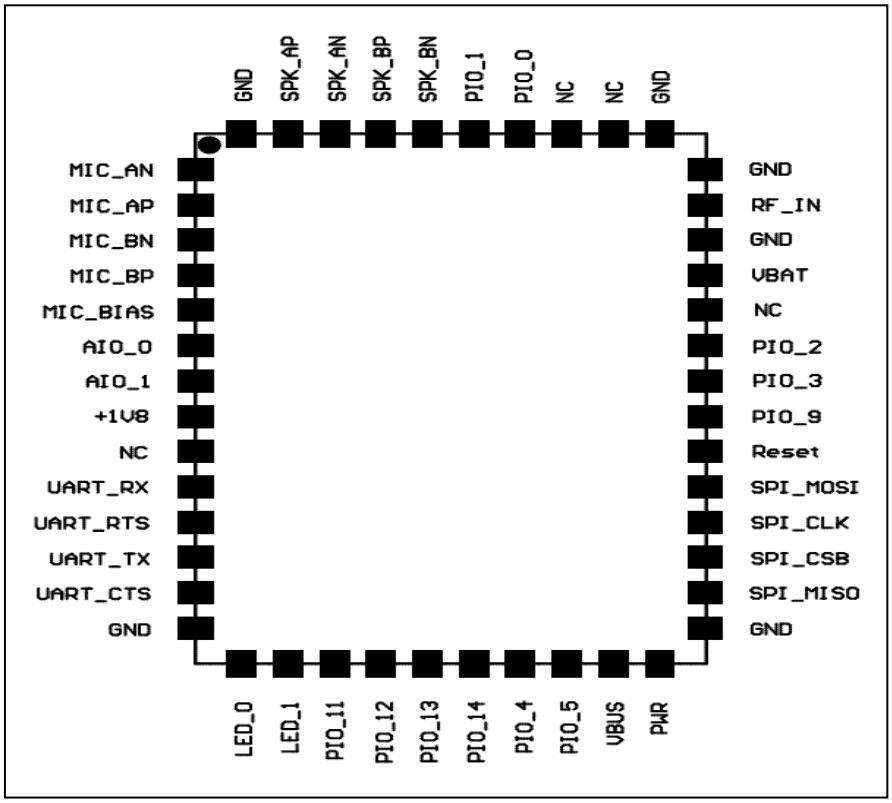


Figure 4

3.1 Pin Description

Pin#	Pin Name	Pad Type	Description
1	MIC_AN	Analogue	Microphone input negative, left
2	MIC_AP	Analogue	Microphone input positive, left
3	MIC_BN	Analogue	Microphone input negative, right
4	MIC_BP	Analogue	Microphone input positive, right
5	MIC_BIAS	Analogue	Microphone bias
6	AIO_0	Bi-directional VDD/Low-voltage regulator output	Analogue programmable input/ output line circuitry and 1.5V regulated output (from internal low-voltage regulator)
7	AIO_1	Bi-directional VDD/Low-voltage regulator output	Analogue programmable input/ output line circuitry and 1.5V regulated output (from internal low-voltage regulator)
8	+1V8	Power	High-voltage linear regulator output (1.8V out)
9	NC	NC	NC
10	UART_RX	CMOS input with weak internal pull-down	UART data input
11	UART_RTS	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART request to send active low
12	UART_TX	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART data output
13	UART_CTS	CMOS input with weak internal pull-down	UART clear to send active low
14	GND	Ground	Digital Ground
15	LED_0	Open drain output	LED driver
16	LED_1	Open drain output	LED driver
17	PIO_11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
18	PIO_12	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
19	PIO_13	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
20	PIO_14	Bi-directional with programmable	Programmable input/output line

		strength internal pull-up/down	
21	PIO_4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
22	PIO_5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
23	VBUS	Charger input	Lithium ion/polymer battery charger input (4.5V~6.5V)
24	PWR	Analogue	Take high to enable high-voltage linear regulator and switch-mode regulator
25	GND	Ground	Digital Ground
26	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	SPI data output
27	SPI_CSB	Input with weak internal pull-up	Chip select for Serial Peripheral Interface (SPI),active low
28	SPI_CLK	Input with weak internal pull-down	SPI clock
29	SPI_MOSI	CMOS input, with weak internal pull-down	SPI data input
30	Reset	Input with weak internal pull-up	Input debounced so must be low for >5ms to cause a reset.
31	PIO_9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
32	PIO_3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
33	PIO_2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
34	NC	NC	NC
35	VBAT	VDD	Positive supply for BT Module(3.3V~4.2V)
36	GND	Ground	Digital Ground
37	RF_IO	RF	RF out
38	GND	Ground	Digital Ground
39	GND	Ground	Digital Ground
40	NC	NC	NC
41	NC	NC	NC

42	PIO_0	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
43	PIO_1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
44	SPK_BN	Analogue	Speaker output negative, right
45	SPK_BP	Analogue	Speaker output positive, right
46	SPK_AN	Analogue	Speaker output negative, left
47	SPK_AP	Analogue	Speaker output positive, left
48	AGND	Analogue	Analogue ground

4. REFERENCE SCHEMATIC

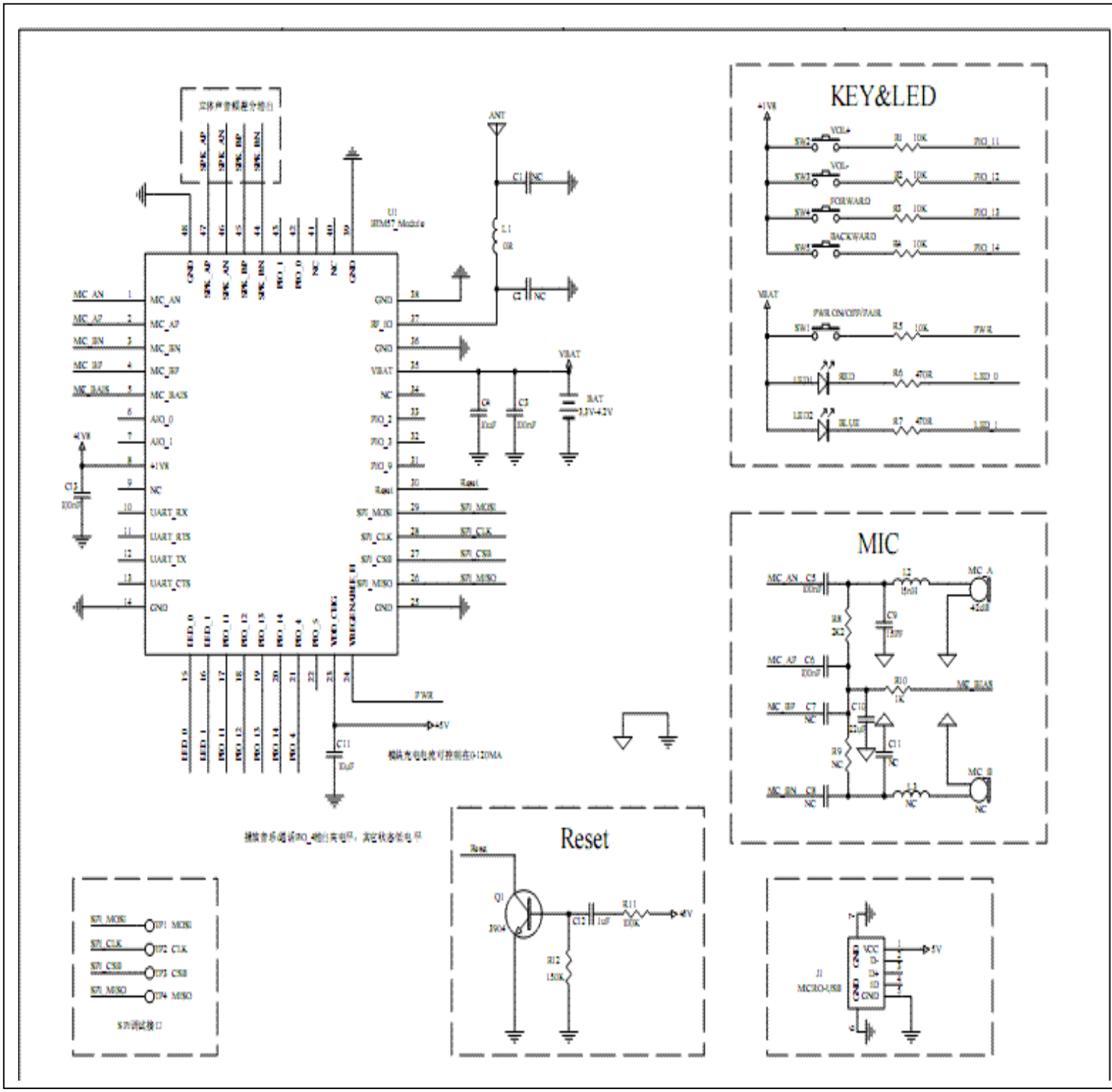


Figure 5

5. PHYSICAL INTERFACE

5.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less.

5.2 Audio Interfaces

Audio interface as following features:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

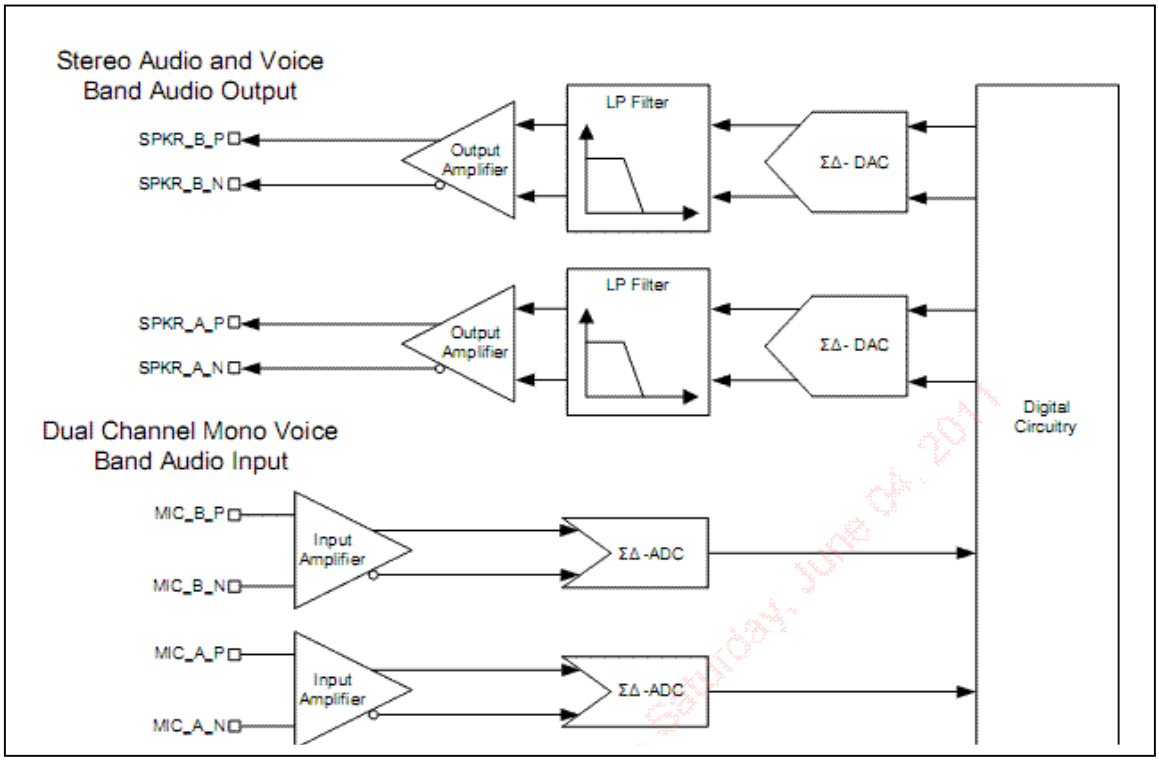


Figure 6

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It uses a minimum of external components. The module features a differential stereo audio output interfaces.

5.2.1 ADC

The ADC consists of a second order Digma Delta converter as show in **Figure 6.**

5.2.2 ADC Sample Rate Selection and Warping

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz,44.1kHz,48kHz.

One of the main concerns for stereo wireless music applications is the ability to keep sample rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of $1/2^{17}$, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

5.2.3 ADC Gain

The ADC contains two gain stages for each channel, an analogue and a digital gain stage.

5.2.4 DAC

The DAC contains two second order Sigma Delta converters allowing two separate channels that are identical in functionality as show in **Figure 6**.

5.2.5 DAC Sample Rate Selection and Warping

Each DAC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz,44.1kHz, 48kHz,96kHz.

One of the main concerns for the DAC used in stereo wireless music applications is the ability to keep sample rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of $1/2^{17}$, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

5.2.6 DAC Gain

The DAC contains two gain stages for each channel, a digital and an analogue gain stage.

5.2.7 Mono Operation

Mono operation is single channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is auxiliary mono channel that may be used in dual mono channel operation.

5.2.8 Audio Input Stage

The audio input stage of the module consists of a low noise input amplifier, which receives its analogue input signal from pins MIC_AP and MIC_AN to a second–order ∑-Δ ADC that outputs a 4Mbit/sec single-bit stream into the digital circuitry. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

5.2.9 Microphone Input

Check the reference design in **Figure 6** for the microphone input design.

5.2.10 Audio Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/sec multi-bit stream, which is fed into the analogue output circuitry.
The output circuit comprises a digital to analogue converter with gain setting and output amplifier. Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk- differential into a load of 16Ω. The output is available as a differential signal between SPK_AP and SPK_AN for the left channel; and between SPK_BP and SPK_BN for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω if only one channel is connected or an external regulator is used.

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The multi-bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

5.3 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

5.4 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

5.5 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

5.6 Serial Interfaces

5.6.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

Note: The serial port interface(UART)can be used for system debugging. Don't support to use command set for profile function application by UART, such as HFP/A2DP/AVRCP and so on. These profiles function application can be controlled only by PIO, such as pairing/connect/answer/play/pause/next/previous function application and so on.

5.6.2 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

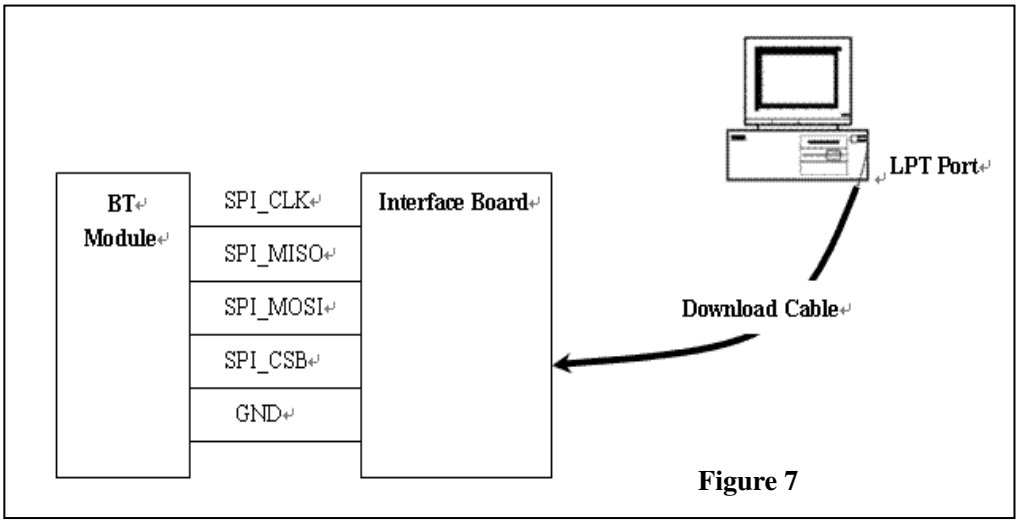


Figure 7

6. ELECTRICAL CHARACTERISTIC

6.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+105	°C
Operating Temperature	-20	+70	°C
PIO/AIO Voltage	-0.4	+1.8	V
VBAT Voltage	-0.4	+3.6	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	VBAT+0.4	V

Table 1

6.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Operating Temperature Range	-20	--	+70	°C
VBAT Voltage	+3.0	+3.3	+4.2	V

Table 2

6.3 Input/output Terminal Characteristics

6.3.1 Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.3	-	+0.25xVBAT	V
VIH input logic level high	0.625*VBAT	-	VBAT+0.3	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75xVBAT	-	0.625xVBAT	V
Input and Tri-state Current				
Ii input leakage current at Vin=+3V3 or 0V	-100	0	100	nA
Ioz tri-state output leakage current at Vo=+3V3 or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	µA
With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	0.2	+1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA

CI Input Capacitance	1.	-	5.0	pF
Resistive Strength				
Rpuw weak pull-up strength at +3V3-0.2V	500k	-	2M	Ω
Rpdw weak pull-up strength at 0.2V	500k	-	2M	Ω
Rpus strong pull-up strength at +3V3-0.2V	10k	-	50k	Ω
Rpds strong pull-up strength at 0.2V	10k	-	50k	Ω

Table 3

6.3.2 Internal CODEC - Analogue to Digital Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Input Sample Rate	8	-	44.1	kHz
Signal / Noise, f_{in}=1kHz, BW=20Hz->20kHz A-Weighted THD+N<1% 150mV Vpk-pk				
F_{sample} = 8kHz	-	82	-	dB
F_{sample} = 11.025kHz	-	81	-	dB
F_{sample} = 16kHz	-	80	-	dB
F_{sample} = 22.05kHz	-	79	-	dB
F_{sample} = 32kHz	-	79	-	dB
F_{sample} = 44.1kHz	-	78	-	dB
Digital Gain	-24	-	21.5	dB

Table 4

6.3.3 Internal CODEC - Digital to Analogue Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Output Sample Rate, Fsample	8	-	48	kHz
Signal / Noise, f_{in}=1kHz, BW=20Hz->20kHz A-Weighted THD+N<0.01% 0dBFS signal Load 100kΩ				
F_{sample} = 8kHz	-	95	-	dB
F_{sample} = 11.025kHz	-	95	-	dB
F_{sample} = 16kHz	-	95	-	dB
F_{sample} = 22.05kHz	-	95	-	dB
F_{sample} = 32kHz	-	95	-	dB
F_{sample} = 44kHz	-	95	-	dB
F_{sample} = 48kHz	-	95	-	dB
F_{sample} = 96kHz		95		dB
Digital Gain	-24	-	21.5	dB
Gain Resolution		1/32		dB

Table 5

6.3.4 Microphone Input

Microphone Input	Min	Typical	Max	Unit
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gian(differential)		800	-	mV rms
Gain	-3	-	42	dB
Gain resolution	-	3	-	dB
Distortion at 1kHz	-	-	-74	dB
3dB Bandwidth	-	20		kHz
Input impedance	-	6		kΩ
THD+N(microphone input)@30mV rms input	-	0.04	-	%

Table 6

6.3.5 Speaker Output

Speaker Driver	Min	Typical	Max	Unit
Output voltage full scale swing (differential)	-	750	-	mV rms
THD+N 100kΩ load	-	-	0.01%	%
THD+N 16Ω load	-	-	0.1%	%
SNR(Load=16Ω, 0dBFS input relative to	-	95	-	dB

Table 7

6.4 Power consumptions

Operating Condition	Min	Typical	Max	Unit
Connected Idle (Sniff 1.28 secs)		0.19		mA
Connected with audio streaming	30	35	40	mA
Deep Sleep Idle mode		60		uA

Table 8

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

2F Friday March 09, 2012 10:21:21

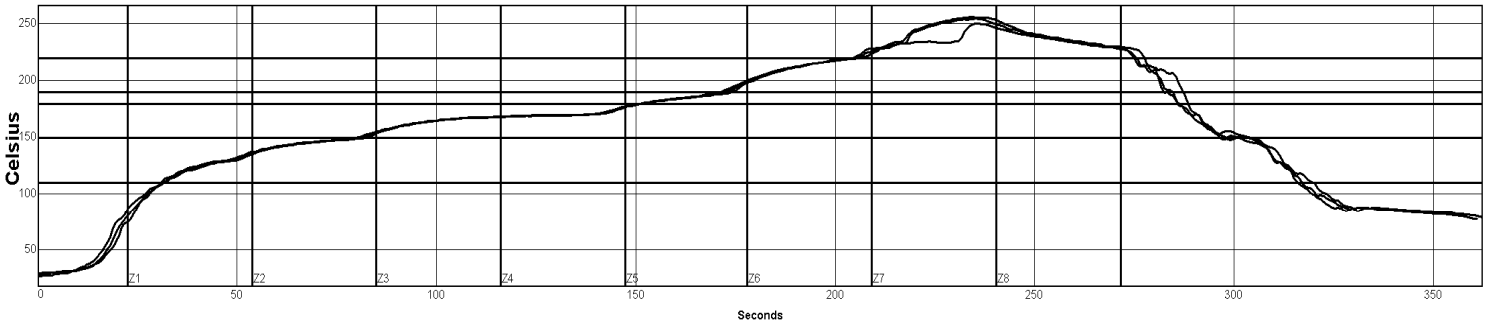
Site:

Oven Name: WQ Process Window Name: 无铅

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8
Top	140	150	170	170	190	225	265	230
Bottom	140	150	170	170	190	225	265	230

Conveyor Speed (cm/min): 75.0



PWI= 304%	Max Rising Slope		Preheat 110-190C		Soak Time 150-180C		Reflow Time /220C		Peak Temp	
2	3.9	189%	141.4	157%	70.4	-296%	71.1	111%	254.8	97%
3	4.0	197%	139.7	149%	70.6	-294%	70.3	103%	250.6	11%
4	3.9	192%	142.1	160%	69.6	-304%	71.2	112%	256.5	130%

Process Window:

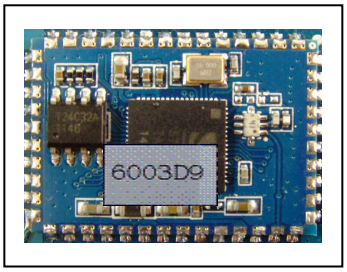
Solder Paste: SYSTEM DEFAULT

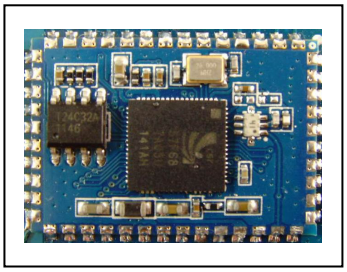
Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.0)	0.0	3.0	Degrees/Second
Preheat Time 110-190C	90	130	Seconds
Soak Time 150-180C	90	110	Seconds
Time Above Reflow - 220C	50	70	Seconds
Peak Temperature	245	255	Degrees Celsius

Description:

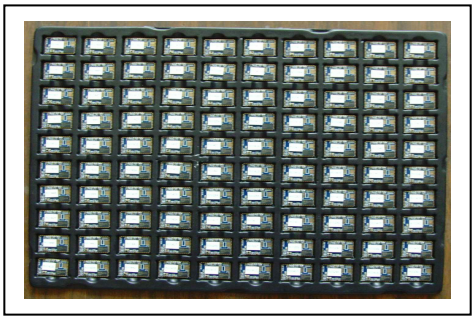
8. PACKAGING INFORMATION

1. BLUETOOTH® Module: BTM521





2. Assembly



3. Dimension