Data Sheet, Rev. 2.0, May 2010

BTM7755G

High Current H-Bridge
Trilith IC 3G

Automotive Power

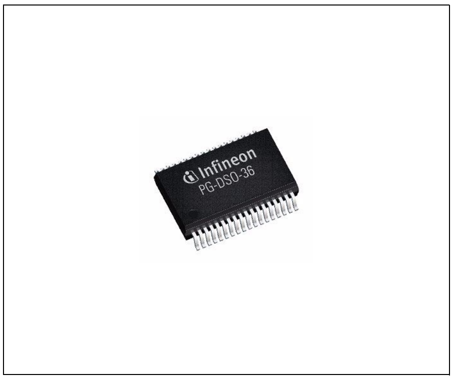
Never stop thinking

Table of Contents

High Current H-Bridge
Trilith IC 3G

BTM7755G

1 Overview


PG-DSO-36-29

Features

- Integrated high current H-Bridge
- Path resistance of max. 295 mΩ @ 150 °C (typ. 150 mΩ @ 25 °C)
- Low quiescent current of typ. 5µA @ 25 °C
- Current limitation level of 12 A typ. (8 A min.)
- Driver circuit with logic inputs
- Status flag diagnosis
- Overtemperature shut down with latch behaviour
- Overvoltage lock out
- Undervoltage shut down
- Switch-mode current limitation for reduced power dissipation in overcurrent situation
- Integrated dead time generation
- Operation up to 28V
- Green Product (RoHS compliant)
- AEC Qualified

Description

The BTM7755G is a fully integrated high current H-bridge for motor drive applications. It contains two p-channel highside MOSFETs and two n-channel lowside MOSFETs with an integrated driver IC in one package. Due to the p-channel highside switches the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis, dead time generation and protection against overtemperature, overvoltage, undervoltage, overcurrent and short circuit.

The BTM7755G provides an optimized solution for protected high current motor drives with very low board space consumption.

Type	Package	Marking
BTM7755G	PG-DSO-36-29	BTM7755G

2 Block Diagram

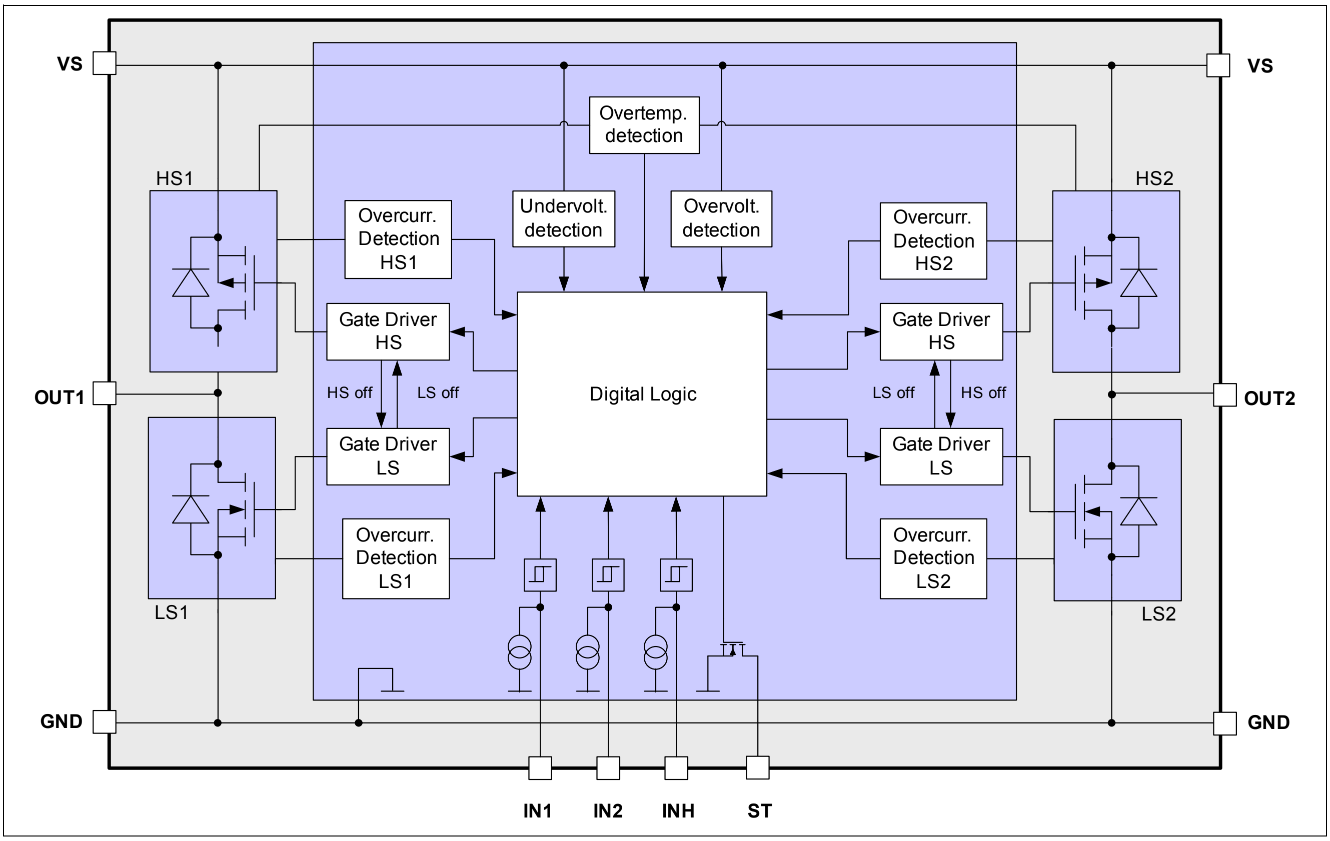


Figure 1 Block Diagram

3 Terms

following figure shows the terms used in this data sheet.

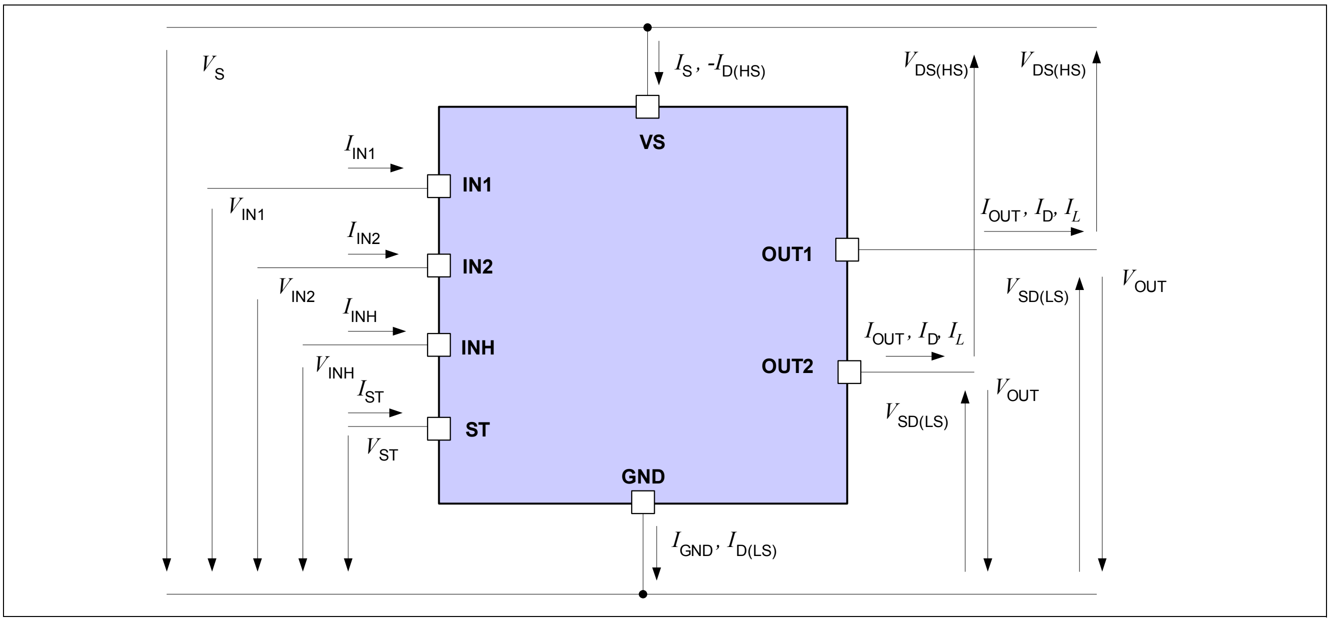


Figure 2 Terms

4 Pin Configuration

4.1 Pin Assignment

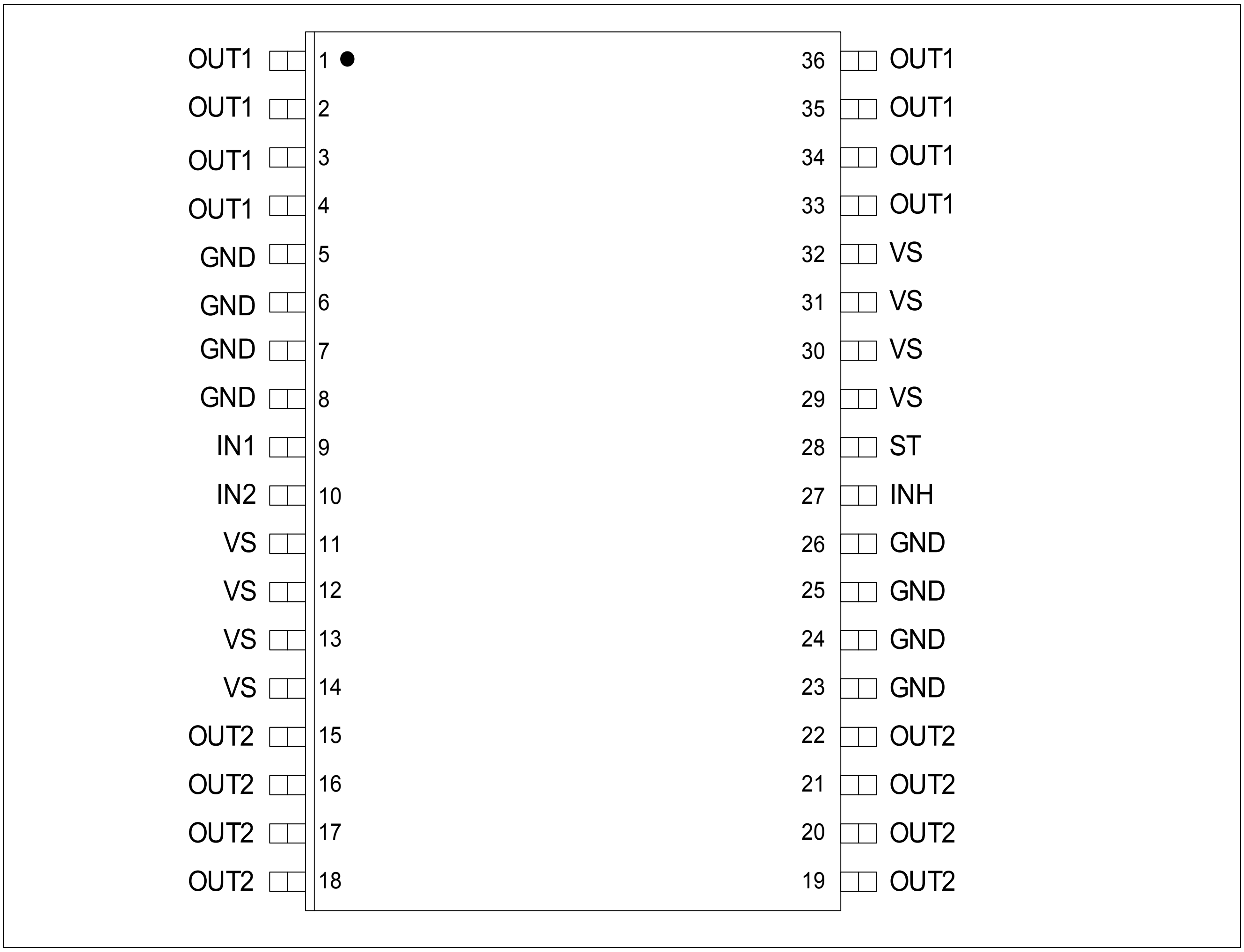


Figure 3 Pin Configuration BTM7755G

4.2 Pin Definitions and Functions

Pins written in bold type need power wiring.

Pin	Symbol	Function
1..4, 33..36	**OUT1**	**Output of first half bridge**
5..8, 23..26	**GND**	**Ground**
9	IN1	Input of first half bridge
10	IN2	Input of second half bridge
11..14, 29..32	**VS**	**Supply, all pins to be connected and shorted externally**
15..22	**OUT2**	**Output of second half bridge**
27	INH	Inhibit pin, to set device in sleep/stand-by mode
28	ST	Status signal, open drain output

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
5.1.1	Supply voltage	V_S	-0.3	45	V	–
5.1.2	Logic Input Voltage	V_{IN1}, V_{IN2}, V_{INH}	-0.3	5.5	V	–
5.1.3	HS/LS continuous drain current	$I_{D(HS)}$ $I_{D(LS)}$	-4	4	A	$T_C < 85°C$ switch active
5.1.4	Voltage at ST pin	V_{ST}	-0.3	45	V	–
5.1.5	ST pin continuous current	I_{ST}	0	2	mA	–
5.1.6	ST pin peak current	I_{ST}	0	4	mA	$t_{peak} < 10\mu s$
Thermal Maximum Ratings						
5.1.7	Junction temperature	T_j	-40	150	°C	–
5.1.8	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
5.1.9	ESD susceptibility	V_{ESD}			kV	HBM[2]
	IN1, IN2, ST, INH		-2	2		
	OUT1, OUT2, GND, VS		-4	4		

1) Not subject to production test, specified by design.

2) HBM according to EIA/JESD 22-A 114B (1.5 kΩ, 100pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Maximum Single Pulse Current

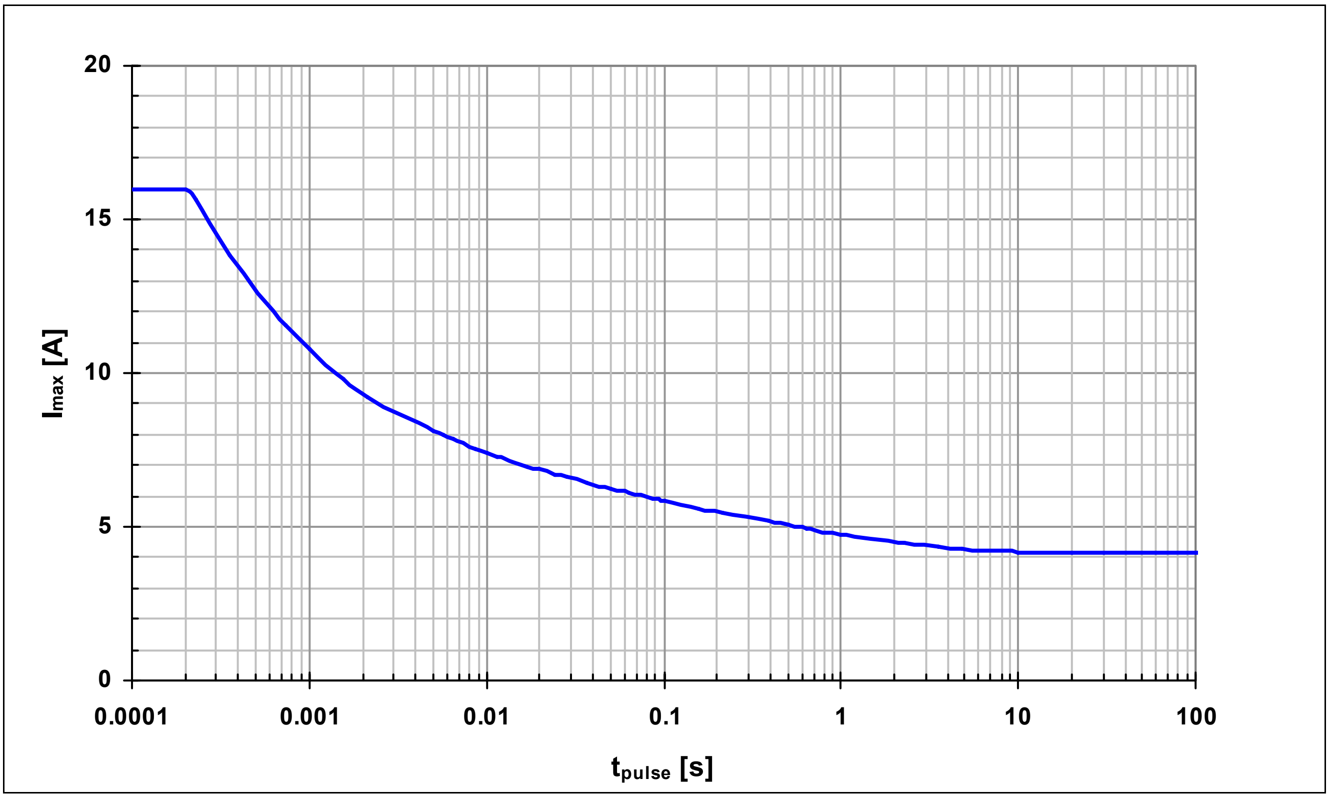


Figure 4 BTM7755G Maximum Single Pulse Current ($T_C = T_{j(0)} < 85°C$)

This diagram shows the maximum single pulse current that can be driven for a given pulse time t_{pulse}. The maximum reachable current may be smaller depending on the current limitation level. Pulse time may be limited due to thermal protection of the device.

5.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
5.2.1	Supply Voltage Range for Normal Operation	$V_{S(nor)}$	8	18	V	VS pins shorted
5.2.2	Extended Supply Voltage Range for Operation	$V_{S(ext)}$	5.5	28	V	VS pins shorted; Parameter deviations possible; [1]
5.2.3	Junction Temperature	T_j	-40	150	°C	–

1) Overtemperature protection available up to supply voltage V_S = 18V.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Thermal Resistance Junction to Soldering Point, Low Side Switch $R_{thjSP(LS)} = \Delta T_{j(LS)} / P_{v(LS)}$	$R_{thjSP(LS)}$	–	–	29	K/W	[1]
5.3.2	Thermal Resistance Junction to Soldering Point, High Side Switch $R_{thjSP(HS)} = \Delta T_{j(HS)} / P_{v(HS)}$	$R_{thjSP(HS)}$	–	–	29	K/W	[1]
5.3.3	Thermal Resistance Junction to Soldering Point, both switches $R_{thjSP} = \max[\Delta T_{j(HS)}, \Delta T_{j(LS)}] / (P_{v(HS)} + P_{v(LS)})$	R_{thjSP}	–	–	29	K/W	[1]
5.3.4	Thermal Resistance Junction-Ambient	R_{thja}	–	46	–	K/W	[1]; [2]

1) Not subject to production test, specified by design.

2) Specified R_{thja} value is according to Jedec JESD51-2, -7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

Transient thermal impedance Z_{thja}

Figure 5 is showing the typical transient thermal impedance of high side or low side switch of BTM7755G mounted according to JEDEC JESD51-7 at natural convection on FR4 2s2p board. The device (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). For the simulation each chip was separately powered with 1W at an ambient temperature T_a of 85°C.

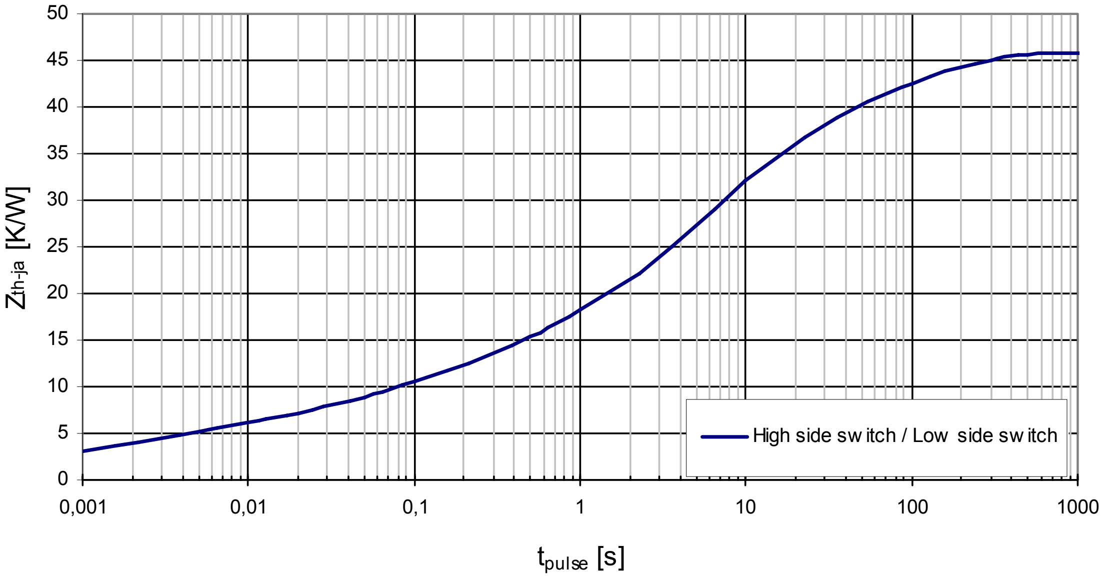


Figure 5 Typical transient thermal impedance of BTM7755G on JESD51-7 2s2p board (1W each chip (separately heated), T_a = 85°C, single pulse)

6 Block Description and Characteristics

6.1 Supply Characteristics

V_S = 8 V to 18 V, **T_j = -40 °C to +150 °C**, **I_L** = 0A, VS pins shorted, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	**Typ.**	**Max.**		
General							
6.1.1	Supply Current	$I_{S(on)}$	–	5	9.5	mA	V_{INH} or V_{IN1} or V_{IN2} = 5 V DC-mode normal operation (no fault condition)
6.1.2	Quiescent Current	$I_{S(off)}$	–	5	15	µA	$V_{INH} = V_{IN1} = V_{IN2}$ = 0 V T_j < 85 °C; [1]
			–	–	30	µA	$V_{INH} = V_{IN1} = V_{IN2}$ = 0 V

[1] Not subject to production test, specified by design.

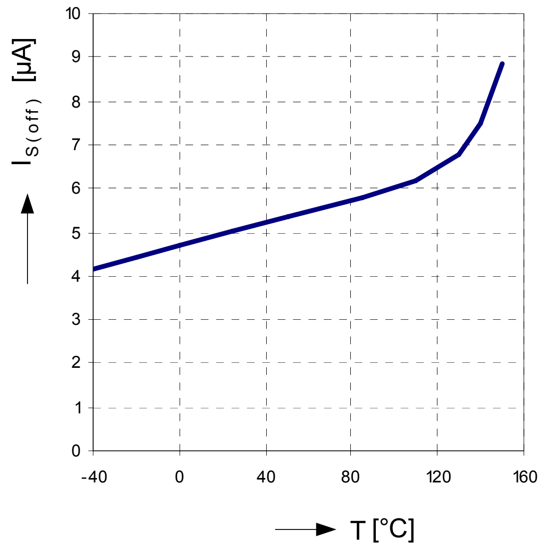


Figure 6 **Typical Quiescent Current vs. Junction Temperature (typ. @ V_S = 13.5V)**

6.2 Power Stages

The power stages of the BTM7755G consist of p-channel vertical DMOS transistors for the high side switches and n-channel vertical DMOS transistors for the low side switches. All protection and diagnostic functions are located in a separate control chip. Both switches, high side and low side, allow active freewheeling and thus minimize power dissipation in the forward operation of the integrated diodes.

The on state resistance R_{ON} is dependent on the supply voltage V_S as well as on the junction temperature T_j. The typical on state resistance characteristics are shown in **Figure 7**.

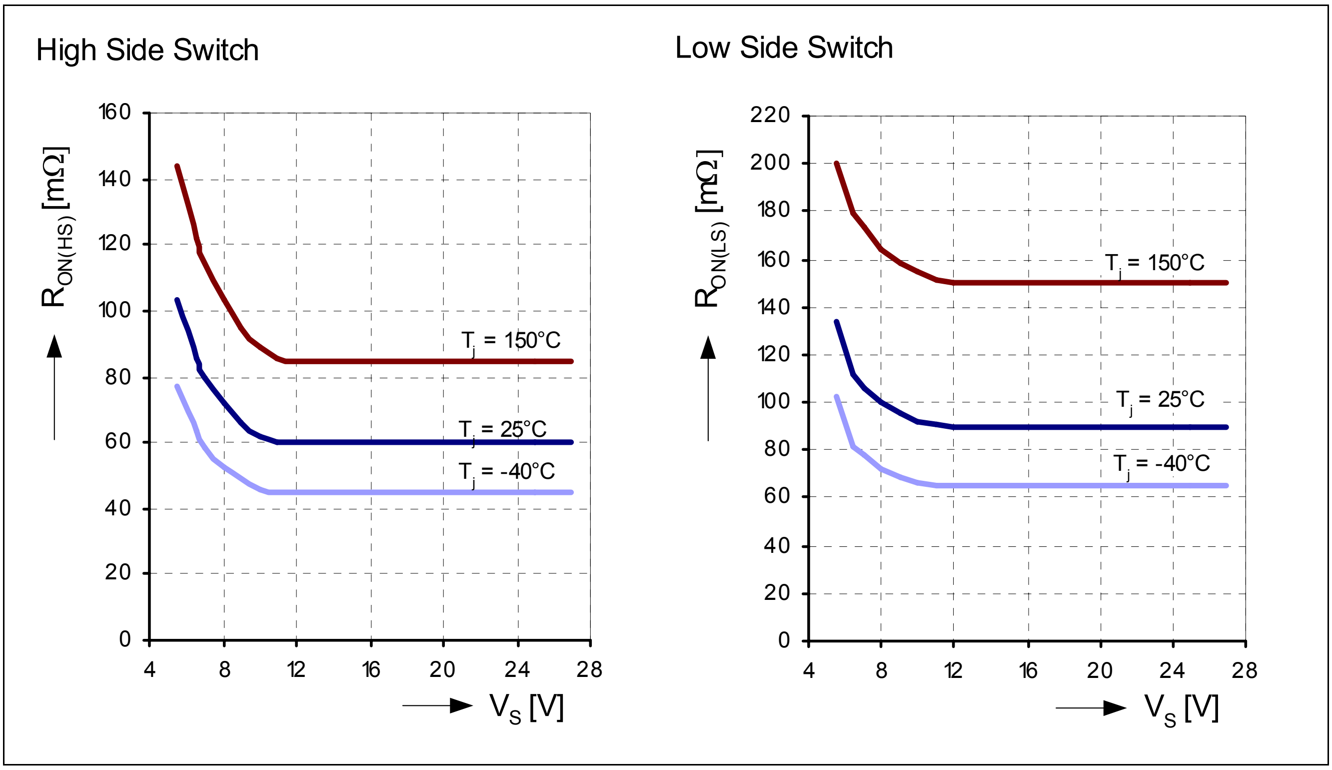


Figure 7 Typical On State Resistance vs. Supply Voltage

6.2.1 Power Stages - Static Characteristics

V_S = 8 V to 18 V, **T_j = -40 °C to +150 °C**, VS pins shorted, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
High Side Switch - Static Characteristics							
6.2.1	On state high side resistance	$R_{ON(HS)}$				mΩ	I_{OUT} = 1 A V_S = 13.5 V
			–	60	–		T_j = 25 °C; 1)
			–	85	115		T_j = 150 °C
6.2.2	Leakage current high side	$I_{L(LKHS)}$				µA	V_{INH} = V_{IN1} = V_{IN2} = 0 V V_{OUT} = 0 V
			–	–	1		T_j < 85 °C; 1)
			–	–	5		T_j = 150 °C
6.2.3	Reverse diode forward-voltage high side 2)	$V_{DS(HS)}$				V	I_{OUT} = -1 A
			–	0.9	–		T_j = -40 °C; 1)
			–	0.8	–		T_j = 25 °C; 1)
			–	0.6	0.8		T_j = 150 °C
Low Side Switch - Static Characteristics							
6.2.4	On state low side resistance	$R_{ON(LS)}$				mΩ	I_{OUT} = -1 A V_S = 13.5 V
			–	90	–		T_j = 25 °C; 1)
			–	150	180		T_j = 150 °C
6.2.5	Leakage current low side	$-I_{L(LKLS)}$				µA	V_{INH} = V_{IN1} = V_{IN2} = 0 V V_{OUT} = V_S
			–	–	1		T_j < 85 °C; 1)
			–	–	3		T_j = 150 °C
6.2.6	Reverse diode forward-voltage low side 2)	$V_{SD(LS)}$				V	I_{OUT} = 1 A
			–	0.9	–		T_j = -40 °C; 1)
			–	0.8	–		T_j = 25 °C; 1)
			–	0.6	0.8		T_j = 150 °C

1) Not subject to production test, specified by design.

2) Due to active freewheeling diode is conducting only until related switch is on

6.2.2 Switching Times

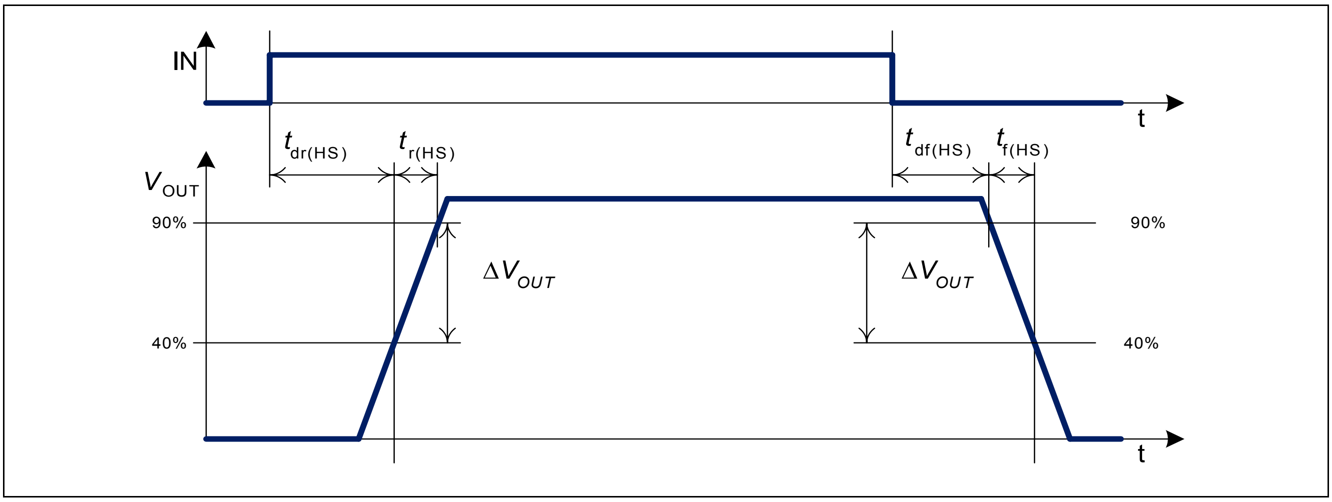


Figure 8 Definition of switching times high side (R_{load} to GND)

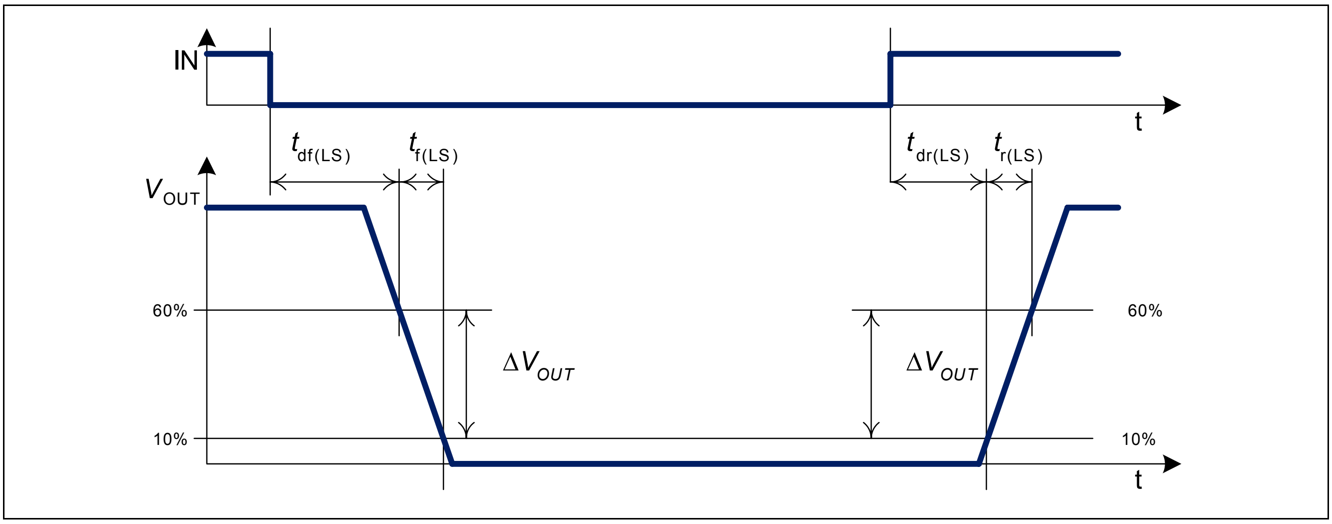


Figure 9 Definition of switching times low side (R_{load} to VS)

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse. It can be calculated using the following formulas:

- $\Delta t_{HS} = (t_{dr(HS)} + 0.2\ t_{r(HS)}) - (t_{df(HS)} + 0.8\ t_{f(HS)})$
- $\Delta t_{LS} = (t_{df(LS)} + 0.2\ t_{f(LS)}) - (t_{dr(LS)} + 0.8\ t_{r(LS)})$.

6.2.3 Power Stages - Dynamic Characteristics

V_S = 13.5V, T_j = +150 °C, R_{Load} = 12 Ω, V_{INH} = 5V, VS pins shorted, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
High Side Switch Dynamic Characteristics							
6.2.7	Rise-time of HS	$t_{r(HS)}$	5	15	25	µs	–
6.2.8	Slew rate HS on	$\Delta V_{OUT}/t_{r(HS)}$	–	0.4	–	V/µs	–
6.2.9	Switch on delay time HS	$t_{dr(HS)}$	50	95	140	µs	–
6.2.10	Fall-time of HS	$t_{f(HS)}$	5	15	25	µs	–
6.2.11	Slew rate HS off	$-\Delta V_{OUT}/t_{f(HS)}$	–	0.4	–	V/µs	–
6.2.12	Switch off delay time HS	$t_{df(HS)}$	25	55	80	µs	–
Low Side Switch Dynamic Characteristics							
6.2.13	Rise-time of LS	$t_{r(LS)}$	10	20	30	µs	–
6.2.14	Slew rate LS switch off	$\Delta V_{OUT}/t_{r(LS)}$	–	0.4	–	V/µs	–
6.2.15	Switch off delay time LS	$t_{dr(LS)}$	30	60	90	µs	–
6.2.16	Fall-time of LS	$t_{f(LS)}$	10	20	30	µs	–
6.2.17	Slew rate LS switch on	$-\Delta V_{OUT}/t_{f(LS)}$	–	0.4	–	V/µs	–
6.2.18	Switch on delay time LS	$t_{df(LS)}$	40	80	120	µs	–

6.3 Protection Functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation, with the exception of the current limitation (**Chapter 6.3.4**). Overvoltage, overtemperature and overcurrent are indicated by switching the open drain output ST to low. Although the slew rate is defined as above (**Chapter 6.2.3**), in case of overvoltage and overcurrent the device will have a higher slew rate of typically 11V/µs.

In the following the protection functions are listed in order of their priority. Overvoltage lock out overrides all other error modes.

6.3.1 Overvoltage Lock Out

To assure a high immunity against overvoltages (e.g. load dump conditions) the device shuts both lowside MOSFETs off and turns both highside MOSFET on, if the supply voltage V_S is exceeding the over voltage protection level $V_{OV(OFF)}$. The IC operates in normal mode again with a hysteresis $V_{OV(HY)}$ if the supply voltage decreases below the switch-on voltage $V_{OV(ON)}$. This behavior of the BTM7755G will lead to freewheeling in highside during over voltage.

6.3.2 Undervoltage Shut Down

To avoid uncontrolled motion of the driven motor at low voltages the device shuts off (both outputs are tri-state), if the supply voltage V_S drops below the switch-off voltage $V_{UV(OFF)}$. In this case all latches will be reset. The IC becomes active again with a hysteresis $V_{UV(HY)}$ if the supply voltage rises above the switch-on voltage $V_{UV(ON)}$.

6.3.3 Overtemperature Protection

The BTM7755G is protected against overtemperature by integrated temperature sensors. Each half bridge, which consists of one high side and one low side switch, is protected by one temperature sensor located in the high side switch. Both temperature sensors function independently. A detection of overtemperature through temperature sensor leads to a shut down of both switches in the half bridge. This state is latched until the device is reset by a low signal with a minimum length of t_{reset} simultaneously at the INH pin and both IN pins, provided that its temperature has decreased at least the thermal hysteresis ΔT in the meantime.

Overtemperature protection is available up to supply voltage V_S = 18V.

For sufficient over temperature protection please consider also operation below the limitations outlined in **Figure 4** and **Figure 5**.

Repetitive use of the overtemperature protection might reduce lifetime.

6.3.4 Current Limitation

The current in the bridge is measured in all four switches. As soon as the current in forward direction in one switch is reaching the limit I_{CLx}, this switch is deactivated for t_{CLS}. In case of INH = 5V (high) the other switch of the same half bridge is activated for the same time (t_{CLS}). During that time all changes at the related IN pin are ignored. However, the INH pin can still be used to switch all MOSFETs off. After t_{CLS} the switches return to their initial setting. The error signal at the ST pin is reset after 1.5 * t_{CLS} if no overcurrent state is detected in the meantime. Unintentional triggering of the current limitation by short current spikes (e.g. inflicted by EMI coming from the motor) is suppressed by internal filter circuitry. Due to thresholds and reaction delay times of the filter circuitry the effective current limitation level I_{CLx} depends on the slew rate of the load current di/dt as shown in **Figure 11**.

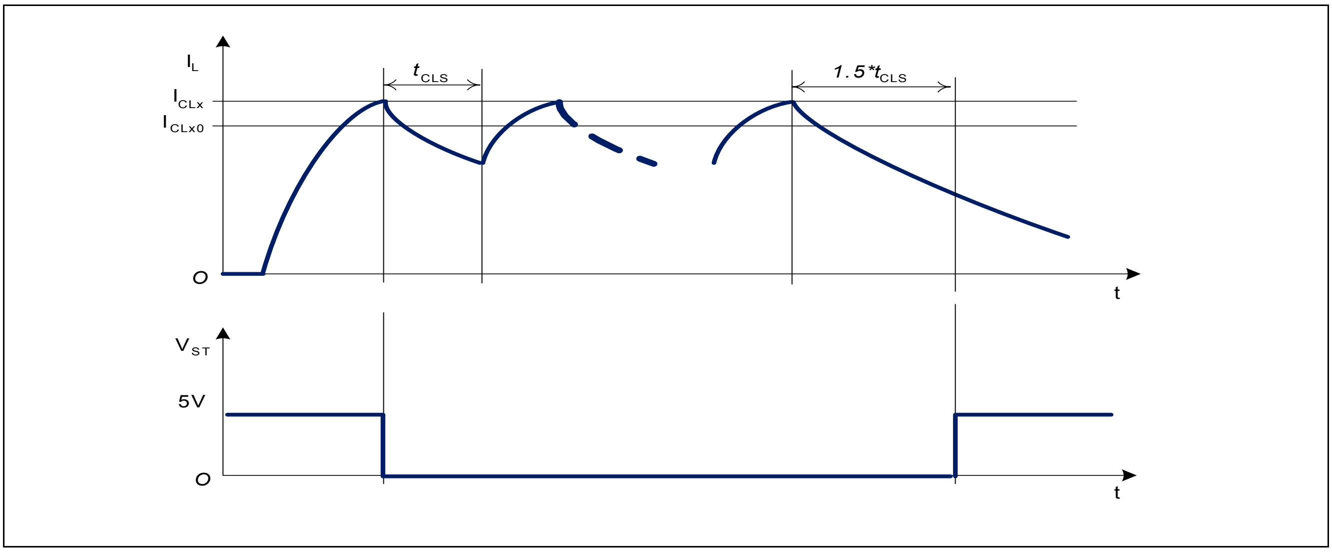


Figure 10 Timing Diagram Current Limitation and Status Flag

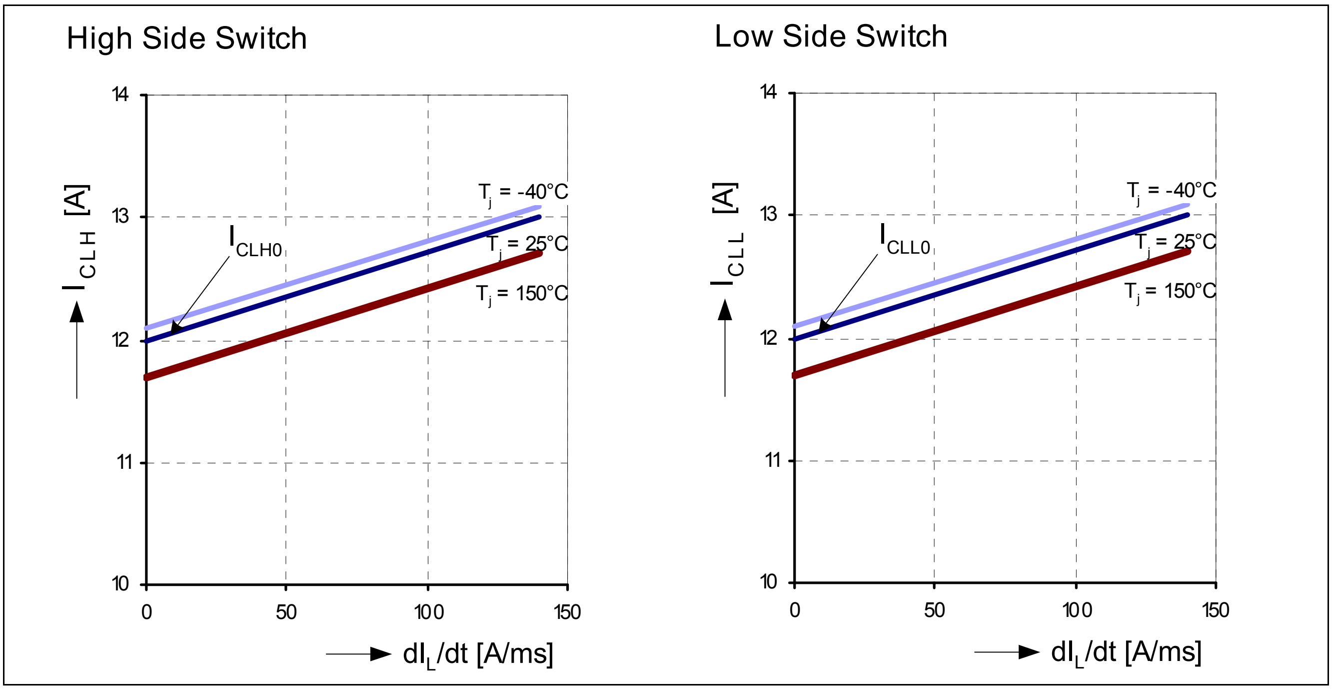


Figure 11 **Current Limitation Level vs. Current Slew Rate dI_L/dt**

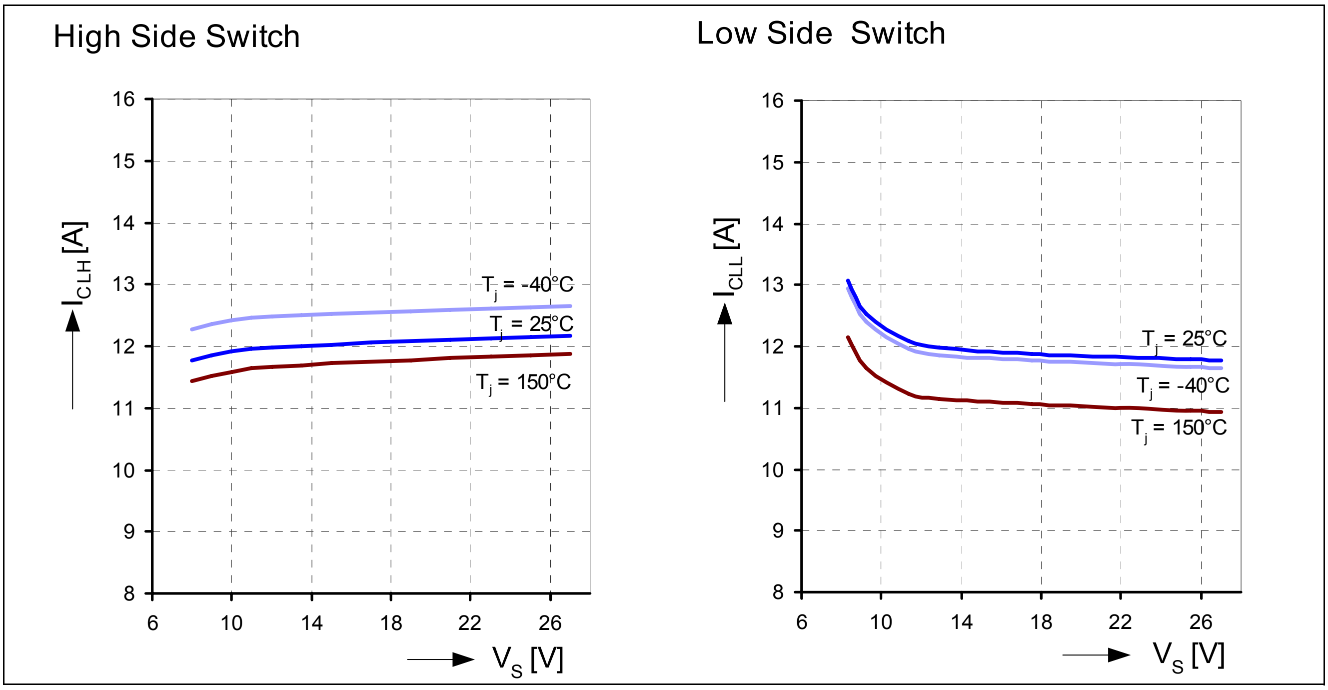


Figure 12 **Typical Current Limitation Detection Levels vs. Supply Voltage**

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. This method of limiting the current has the advantage that the power dissipation in the BTM7755G is much smaller than by driving the MOSFETs in linear mode. Therefore it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

6.3.5 Short Circuit Protection

The device provides embedded protection functions against

- output short circuit to ground
- output short circuit to supply voltage
- short circuit of load

The short circuit protection is realized by the previously described current limitation in combination with the over-temperature shut down (see **Chapter 6.3.3**) of the device.

6.3.6 Electrical Characteristics - Protection Functions

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, VS pins shorted, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Over Voltage Lock Out							
6.3.1	Switch-ON voltage	$V_{OV(ON)}$	27.8	–	–	V	V_s decreasing
6.3.2	Switch-OFF voltage	$V_{OV(OFF)}$	28	–	30	V	V_s increasing
6.3.3	ON/OFF hysteresis	$V_{OV(HY)}$	–	0.2	–	V	[1]
Under Voltage Shut Down							
6.3.4	Switch-ON voltage	$V_{UV(ON)}$	–	–	5.5	V	V_S increasing
6.3.5	Switch-OFF voltage	$V_{UV(OFF)}$	4.0	–	5.4	V	V_S decreasing
6.3.6	ON/OFF hysteresis	$V_{UV(HY)}$	–	0.2	–	V	[1]
Thermal Shut Down							
6.3.7	Thermal shut down junction temperature	T_{jSD}	155	175	200	°C	[1]; $V_S \leq 18$ V
6.3.8	Thermal switch on junction temperature	T_{jSO}	153	–	190	°C	[1]
6.3.9	Thermal hysteresis	ΔT	–	7	–	°C	[1]
6.3.10	Reset pulse at INH and IN pin (INH, IN1 and IN2 low)	t_{reset}	8	–	–	μs	[1]
Current Limitation							
6.3.11	Current limitation detection level high side	I_{CLH0}	8	12	16	A	V_S = 13.5 V
6.3.12	Current limitation detection level low side	I_{CLL0}	8	12	16	A	V_S = 13.5 V
6.3.13	Shut off time for HS and LS	t_{CLS}	50	100	200	μs	V_S = 13.5 V, T_j = 25 °C

[1] Not subject to production test, specified by design.

6.4 Control and Diagnostics

6.4.1 Input Circuit

The control inputs INx and INH consist of TTL/CMOS compatible schmitt triggers with hysteresis which control the integrated gate drivers for the MOSFETs. To set the device in stand-by mode, INH and INx pins need to be all connected to GND. When the INH is high, in each half bridge one of the two power switches (HSx or LSx) is switched on, while the other power switch is switched off, depending on the status of the INx pin. When INH is low, a high INx signal will turn the corresponding highside switches on. This provides customer the possibility to switch on one high side switch while keeping the other switches off and therefore to do an open load detection together with external circuitry (see also **Chapter 7** - Application Information). A low on all INx and INH signal will turn off both power switches. To drive the logic inputs no external driver is needed, therefore the BTM7755G can be interfaced directly to a microcontroller.

6.4.2 Dead Time Generation

In bridge applications it has to be assured that the highside and lowside MOSFET are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver IC, which senses the status of the MOSFETs to ensure that the high or low side switch can be switched on only if the corresponding low or high side switch is completely turned off.

6.4.3 Status Flag Diagnosis

The status pin provides diagnostic signal of the device. It is an open drain output which requires a pull-up resistor. In case of overvoltage, overtemperature and overcurrent situation the status output is switched to low. In case of current limitation the status output is activated for 1.5 * t_{CLS}.

6.4.4 Truth Table

Device State	**Inputs**			**Outputs**					**Mode**
	INH	**IN1**	**IN2**	**HS1**	**LS1**	**HS2**	**LS2**	**ST**	
Normal operation	0	0	0	OFF	OFF	OFF	OFF	1	Stand-by mode, reset
	1	0	0	OFF	ON	OFF	ON	1	–
	1	0	1	OFF	ON	ON	OFF	1	–
	1	1	0	ON	OFF	OFF	ON	1	–
	1	1	1	ON	OFF	ON	OFF	1	–
Open-Load detection mode	0	0	1	OFF	OFF	ON	OFF	1	Enable Open-load detection
	0	1	0	ON	OFF	OFF	OFF	1	Enable Open-load detection
	0	1	1	ON	OFF	ON	OFF	1	
Over-voltage (OV)	X	X	X	ON	OFF	ON	OFF	0	Shut-down of LSS, HSS activated, error detected
Under-voltage (UV)	X	X	X	OFF	OFF	OFF	OFF	1	UV lockout, reset
Overtemperature or short circuit of HSS or LSS[1]	0	0	0	OFF	OFF	OFF	OFF	1	Stand-by mode, reset of latch
	1	X	X	OFF	OFF	OFF	OFF	0	Shut-down with latch, error detected
	X	1	X						
	X	X	1						
Current limitation mode half bridge 1	1	0	X	ON	OFF	X	X	0	Short Circuit in LS1 detected, half bridge 2 operates in normal mode
	1	1	X	OFF	ON	X	X	0	Short Circuit in HS1 detected, half bridge 2 operates in normal mode
	0	1	X	OFF	OFF	X	X	0	Short Circuit in HS1 detected
Current limitation mode half bridge 2	1	X	0	X	X	ON	OFF	0	Short Circuit in LS2 detected, half bridge 1 operates in normal mode
	1	X	1	X	X	OFF	ON	0	Short Circuit in HS2 detected, half bridge 1 operates in normal mode
	0	X	1	X	X	OFF	OFF	0	Short Circuit in HS2 detected

[1] In short circuit of HSS or LSS, the junction temperature will arise and as soon as the over temperature shut down threshold is reached the device will shut down and latch the status. Short circuit of HSS and LSS itself won't be detected as failure.

Inputs:	**Switches**	**Status Flag ST:**
0 = Logic LOW	OFF = switched off	0 = Logic LOW (error)
1 = Logic HIGH	ON = switched on	1 = Logic HIGH (normal operation)
X = 0 or 1	X = switched on or off	

6.4.5 Electrical Characteristics - Control and Diagnostics

V_S = 8 V to 18 V, T_j = -40 °C to +150 °C, VS pins shorted, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Control Inputs (IN and INH)							
6.4.1	High level threshold voltage INH, IN1, IN2	$V_{INH(H)}$, $V_{IN1(H)}$, $V_{IN2(H)}$	–	1.6	2	V	–
6.4.2	Low level threshold voltage INH, IN1, IN2	$V_{INH(L)}$, $V_{IN1(L)}$, $V_{IN2(L)}$	1.1	1.4	–	V	–
6.4.3	Input voltage hysteresis	V_{INHHY}, V_{INHY}	–	200	–	mV	[1]
6.4.4	Input current	$I_{INH(H)}$, $I_{IN1(H)}$, $I_{IN2(H)}$	–	30	200	µA	V_{IN1}, V_{IN2}, V_{INH} = 5.5 V
6.4.5	Input current	$I_{INH(L)}$, $I_{IN1(L)}$, $I_{IN2(L)}$	–	25	125	µA	V_{IN1}, V_{IN2}, V_{INH} = 0.4 V
Status Signal							
6.4.6	Status Low output voltage	$V_{ST(LOW)}$	–	–	0.4	V	I_{ST} = 1.6 mA
6.4.7	Status leakage current	$I_{ST(LK)}$	–	–	1	µA	V_{ST} = 0...28 V

1) Not subject to production test, specified by design.

7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

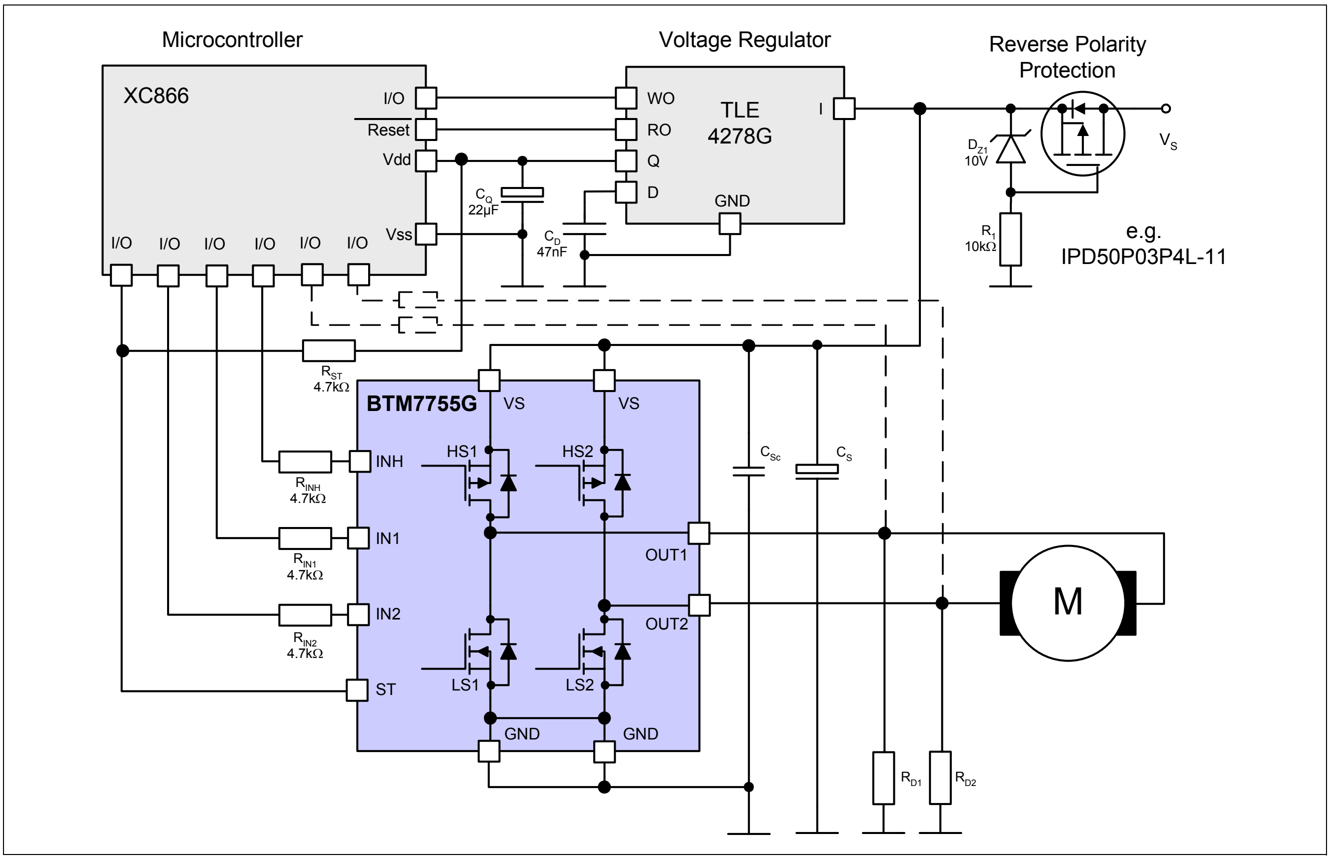


Figure 13 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

7.1 Application and Layout Considerations

Due to the fast switching times for high currents, special care has to be taken during the PCB layout. Stray inductances have to be minimized in the power bridge design as it is necessary in all switched high power bridges. The BTM7755G has no separate pin for power ground and logic ground. **Therefore it is recommended to assure that the offset between power ground and logic ground pins of the device is minimized. It is also necessary to ensure that all VS pins are at the same voltage level. Therefore the VS pins need to be shorted together.** Voltage differences between the VS pins may cause parameter deviations (such as reduced current limits) up to a latched shutdown of the device with error signal on the ST pin, similar to overtemperature shutdown.

Due to the fast switching behavior of the device in current limitation mode or overvoltage lock out a low ESR electrolytic capacitor C_S of at least 100 µF from VS to GND is recommended. This prevents destructive voltage peaks and drops on VS. This is recommended for both PWM and non PWM controlled applications. The value of the capacitor must be verified in the real application.

In addition a ceramic capacitor C_{SC} from VS to GND close to each device is recommended to provide current for the switching phase via a low inductance path and therefore reducing noise and ground bounce. A reasonable value for this capacitor would be about 470 nF.

It is recommended to do the freewheeling in the low side path to ensure a proper function and avoid unintended overtemperature detection and shutdown. For proper operation it is also recommended to put a pull-down resistor R_{Dx} on each output OUTx to GND with a value in the range of e.g. 1...10 kΩ. These resistors can also be used for open load detection.

Considerations for Open Load Detection Mode

As mentioned in **Chapter 6.4.1** both high side switches can be switched on independently while all other switches are off. This will be realized by setting the corresponding IN signal to high while INH and the other IN are low.

Device State	**Inputs**			**Outputs**					**Mode**
	INH	**IN1**	**IN2**	**HS1**	**LS1**	**HS2**	**LS2**	**ST**	
Open-Load detection mode	0	0	1	OFF	OFF	ON	OFF	1	HS2 active
	0	1	0	ON	OFF	OFF	OFF	1	HS1 active
	0	1	1	ON	OFF	ON	OFF	1	both HSx are active

Together with the recommended pull-down resistors on the outputs OUTx to GND this provides the possibility to do an open load detection in H-bridge configuration.

In case of one high side is active while the other half bridge is off (HS off and LS off) a current of up to 2mA will be sourced out of the OUT of the high ohmic half bridge. This has to be considered while choosing the right value of the pull-down resistor.

8 Package Outlines

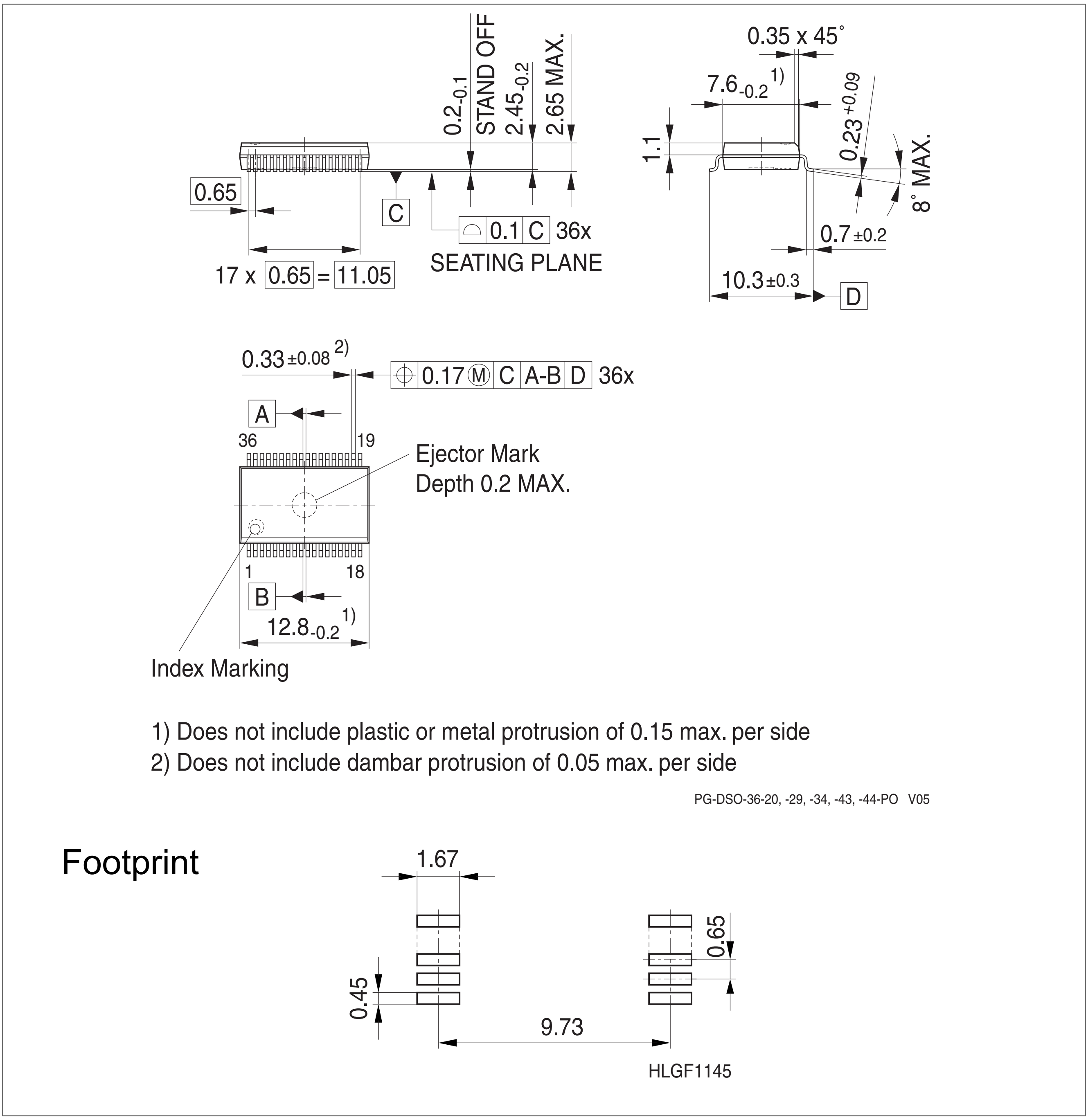


Figure 14 **PG-DSO-36-29 (Plastic Green Dual Small Outline Package)**

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
2.0	2010-05-28	Initial version Data Sheet

Edition 2010-05-28

Published by
Infineon Technologies AG
81726 Munich, Germany

© 2010 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.