BTM8605

Bluetooth Module Data Sheet

Document Type:	Bluetooth Module Datasheet
Document Version:	V1.0
Release Date:	December 04, 2012

Copyright 2012 by Buddies Technology Limited. All Rights Reserved.

Reproduction of this document, in part of in whole, by any means is prohibited without written permission from Buddies Technology Limited. The information contained herein is believed to be accurate as of the date of publication. However, Buddies is not liable for any damages, including indirect or consequential from the use of software this document represents, or any reliance of the accuracy of this document. Buddies reserves the right to change the contents of this document at any time without notice.

This document contains proprietary confidential trade secrets and may be subject to additional restrictions contained in the licensing agreement under which this document was obtained.

Revision History

Date	Version	Description	Author
2012-12-04	V1.0	■ First Release	

CONTENT

1. INTRODUCTION

The BTM8605 Bluetooth® module is a perfect solution for enhanced audio applications, such as headphones. It can be connected with any Bluetooth® devices in an operating range. It is slim and light so the designers can have better flexibilities for the product shapes.

The BTM8605 Bluetooth® module complies with Bluetooth® specification version 4.0. It supports A2DP(mono),AVRCP profiles. It integrates RF Baseband controller, antenna,… etc. and programmable I/O, speaker output… etc.

The detail information of BTM8605 Bluetooth® module is presented in this document below.

1.1 Block Diagram

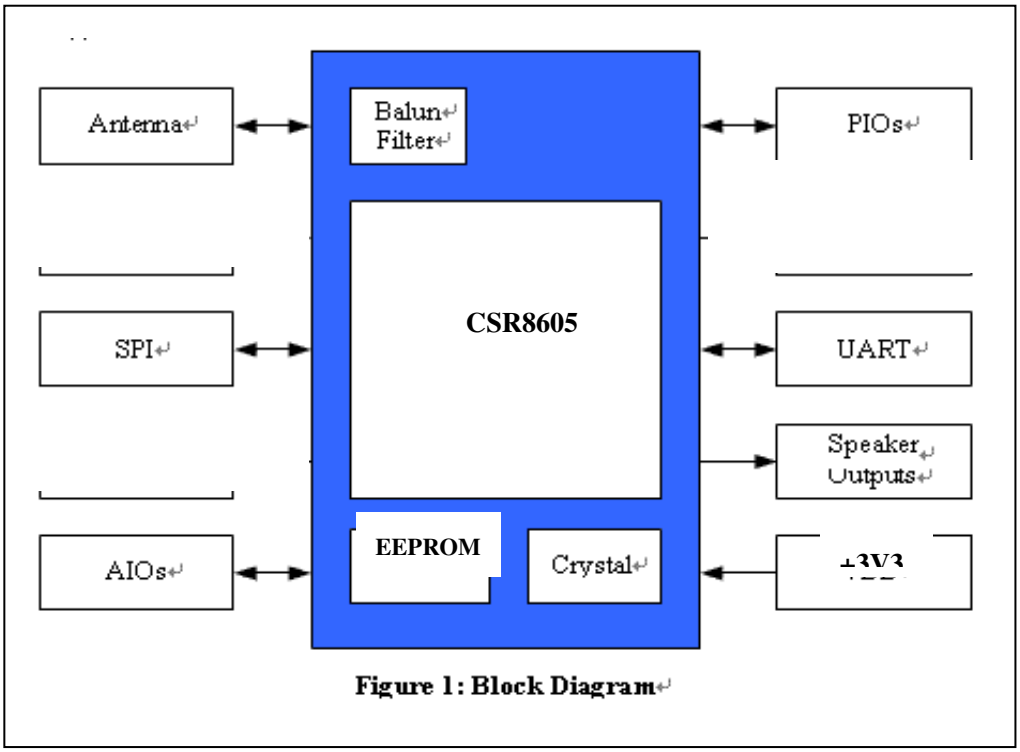


Figure 1: Block Diagram

1.2 Features

- ✓ Small overall dimension(14mm x 16mm x 2mm)
- ✓ Bluetooth Specification V4.0
- ✓ Class 2 support
- ✓ Physical connection as SMD type
- ✓ Built-in RF combo filter, Integrated 26M Crystal.
- ✓ Support A2DP(mono),AVRCP profile.
- ✓ No radio signal interference, support for 802.11 co-existence

※ ***Some features are optional for customization on demand.***

1.3 Application

- ✓ High Quality Mono Bluetooth Headphone
- ✓ Bluetooth Speakers(mono)

2. GENERAL SPECIFICATION

Bluetooth Specification	
Chip Set	CSR 8605 (ROM)
Module ID	BTM8605
BT Standard	Bluetooth® V4.0
RF TX Output Power	4dBm (Class II)
Sensitivity	-86dBm@0.1%BER
Frequency Band	2.402GHz~2.480GHz ISM Band
Baseband Crystal OSC	26MHz
Hopping	1600hops/sec, 1MHz channel space
RF Input Impedance	50 ohms
Major Interface	• Microphone : Input (Differential) • Speaker : Output (Differential) • PCM : Output • UART : Tx/Rx (for test) • PIOs • Antenna
Profile	A2DP,AVRCP
Voice Processor	80MIPS Kalimba with cVc support
Power	
Supply Voltage	3.3V ~ 4.2V DC
Working Current	30mA typical,Depends on profiles
Standby Current	<1mA
Operating Environment	
Temperature	-40C to +85
Humidity	10%~90% Non-Condensing
Environmental	RoHS Compliant

3. PHYSICAL CHARACTERISTIC

Dimension:

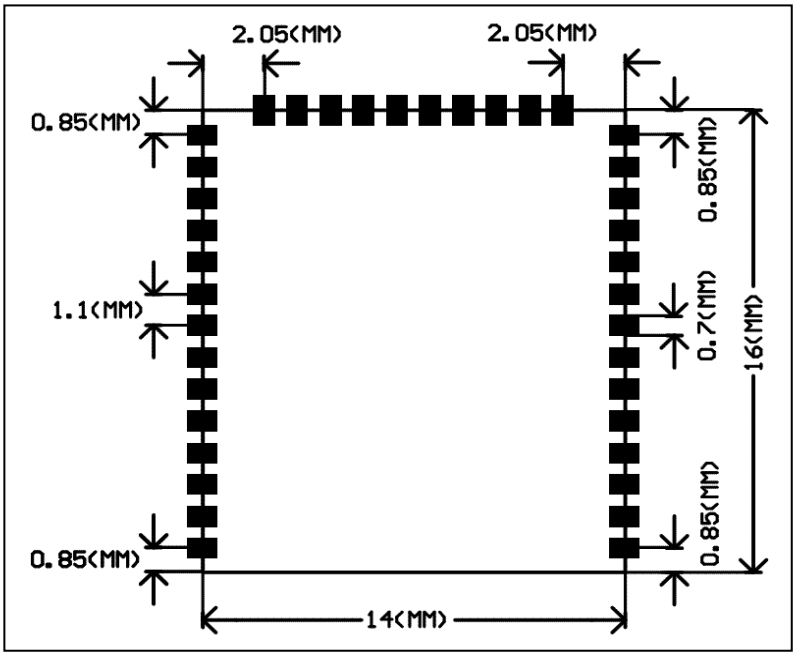


Figure 2

Pin Definition:

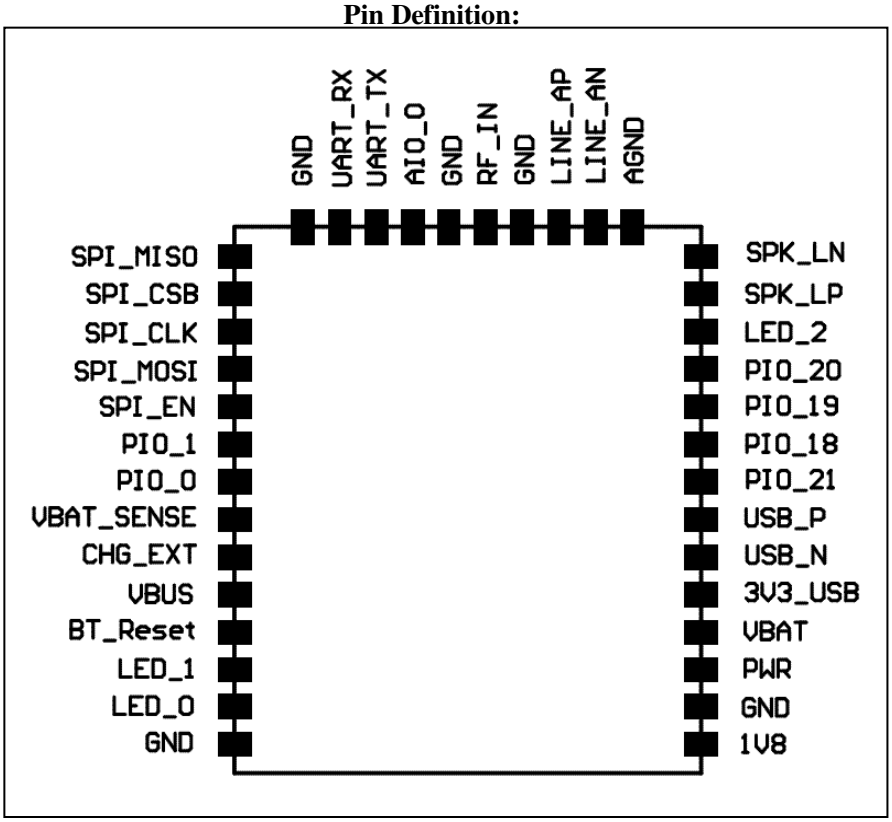


Figure 3

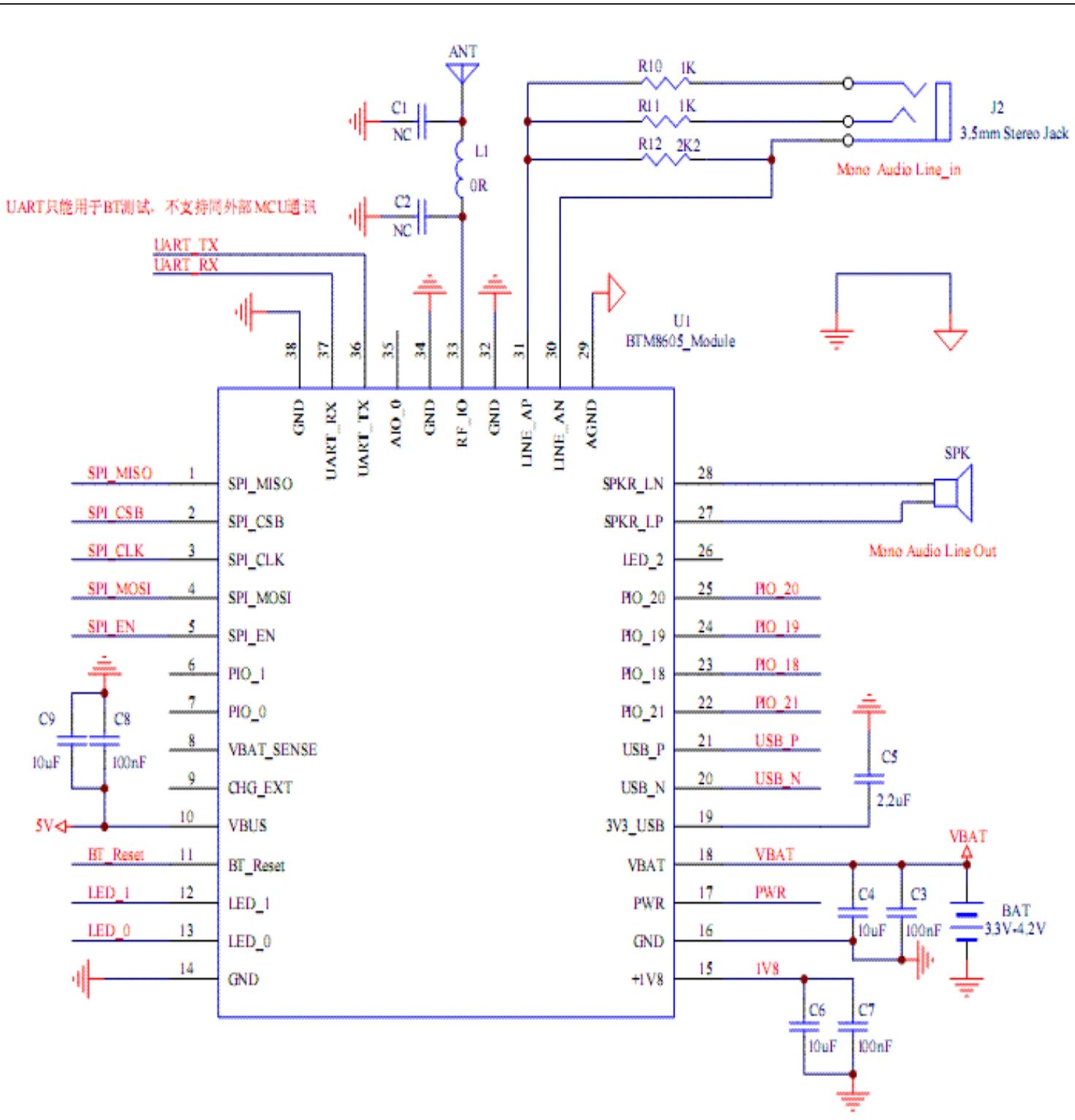
3.1 Pin Description

Pin#	Pin Name	Pad Type	Description
1	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	SPI data output
2	SPI_CSB	Input with weak internal pull-up	Chip select for Serial Peripheral Interface (SPI),active low
3	SPI_CLK	Input with weak internal pull-down	SPI clock
4	SPI_MOSI	CMOS input, with weak internal pull-down	SPI data input
5	SPI_EN	Input with weak pull-down	SPI select input
6	PIO_1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
7	PIO_0	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
8	VBAT_SENSE	Battery charger sense input	Connect directly to the battery positive pin
9	CHG_EXT	Exernal battery charger control	External battery charger transistor base control
10	VBUS	Power supply	Alternative supply via bypass regulator for 1.8V and 1.35V switchmode power supply regulator inputs. Must be connected to the same potential as VOUT_3V3.
11	BT_Reset	Input with strong pull-up	Reset if low.Pull low for minimum 5ms to cause a reset
12	LED_1	Open drain output	LED driver
13	LED_0	Open drain output	LED driver
14	GND	Ground	Digital Ground
15	1V8	Open drain output	LED driver
16	GND	Ground	Digital Ground
17	PWR	Input enable	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on

			internally and the button used as a multifunction input.
18	VBAT	Power supply	Battery positive terminal
19	3V3_USB	Power supply	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
20	USB_N	Bidirectional	USB data minus
21	USB_P	Bidirectional	USB data plus with selectable internal 1.5kohm pull-up resistor
22	PIO_21	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
23	PIO_18	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
24	PIO_19	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
25	PIO_20	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
26	LED_2	Open drain output	LED driver
27	SPKR_LP	Analogue out	Speaker output positive
28	SPKR_LN	Analogue out	Speaker output negative
29	AGND	Ground	Analogue Ground
30	LINE_AP	Analogue in	Line input positive
31	LINE_AN	Analogue in	Line input negative
32	GND	Ground	Digital Ground
33	RF_IO	RF	Bluetooth 50ohm transmitter output/receiver input
34	GND	Ground	Digital Ground
35	AIO_0	Bidirectional	Analogue programmable input/output line 0
36	UART_TX	Bidirectional with strong pull-up	UART Data Output
37		Bidirectional with strong	UART Data Input

	UART_RX	pull-up	
38	GND	Ground	Digital Ground

4. REFERENCE SCHEMATIC



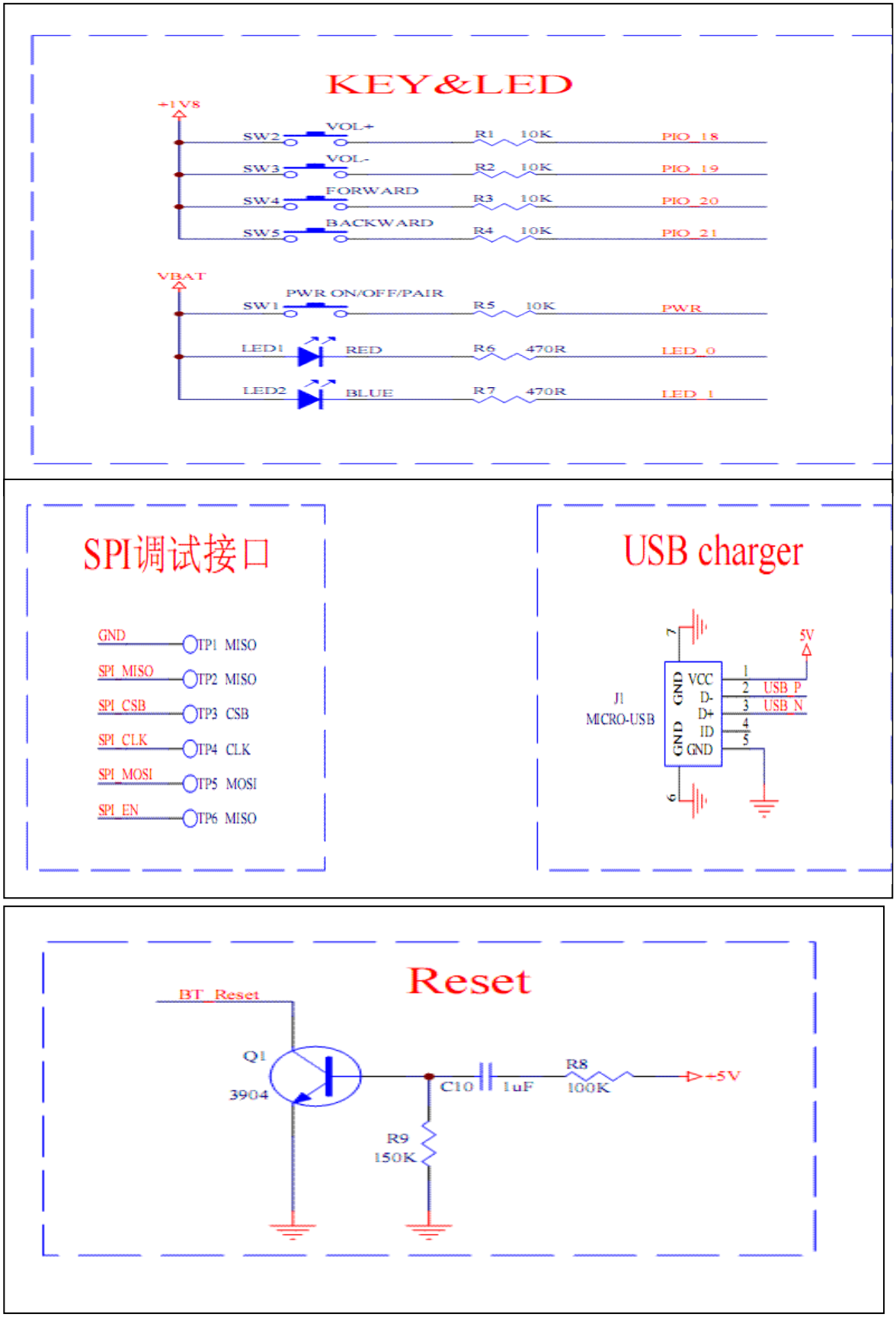

KEY&LED
+1V8
SW2
VOL+
R1
10K
PIO_18
SW3
VOL-
R2
10K
PIO_19
SW4
FORWARD
R3
10K
PIO_20
SW5
BACKWARD
R4
10K
PIO_21
VBAT
SW1
PWR ON/OFF/PAIR
R5
10K
PWR
LED1
RED
R6
470R
LED_0
LED2
BLUE
R7
470R
LED_1
SPI调试接口
GND
TP1 MISO
SPI_MISO
TP2 MISO
SPI_CSB
TP3 CSB
SPI_CLK
TP4 CLK
SPI_MOSI
TP5 MOSI
SPI_EN
TP6 MISO
USB charger
J1
MICRO-USB
GND
VCC
D-
D+
ID
GND
5V
USB_P
USB_N
Reset
BT_Reset
Q1
3904
C10
1uF
R8
100K
+5V
R9
150K

Figure 4

5.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less.

5.2 Audio Interfaces

Audio interface as following features:

- Mono analogue line input for audio band
- Mono analogue output for audio band
- Support for digital audio bus standards such as I²S
- Support for PCM interfaces including PCM master codecs that require an external system clock

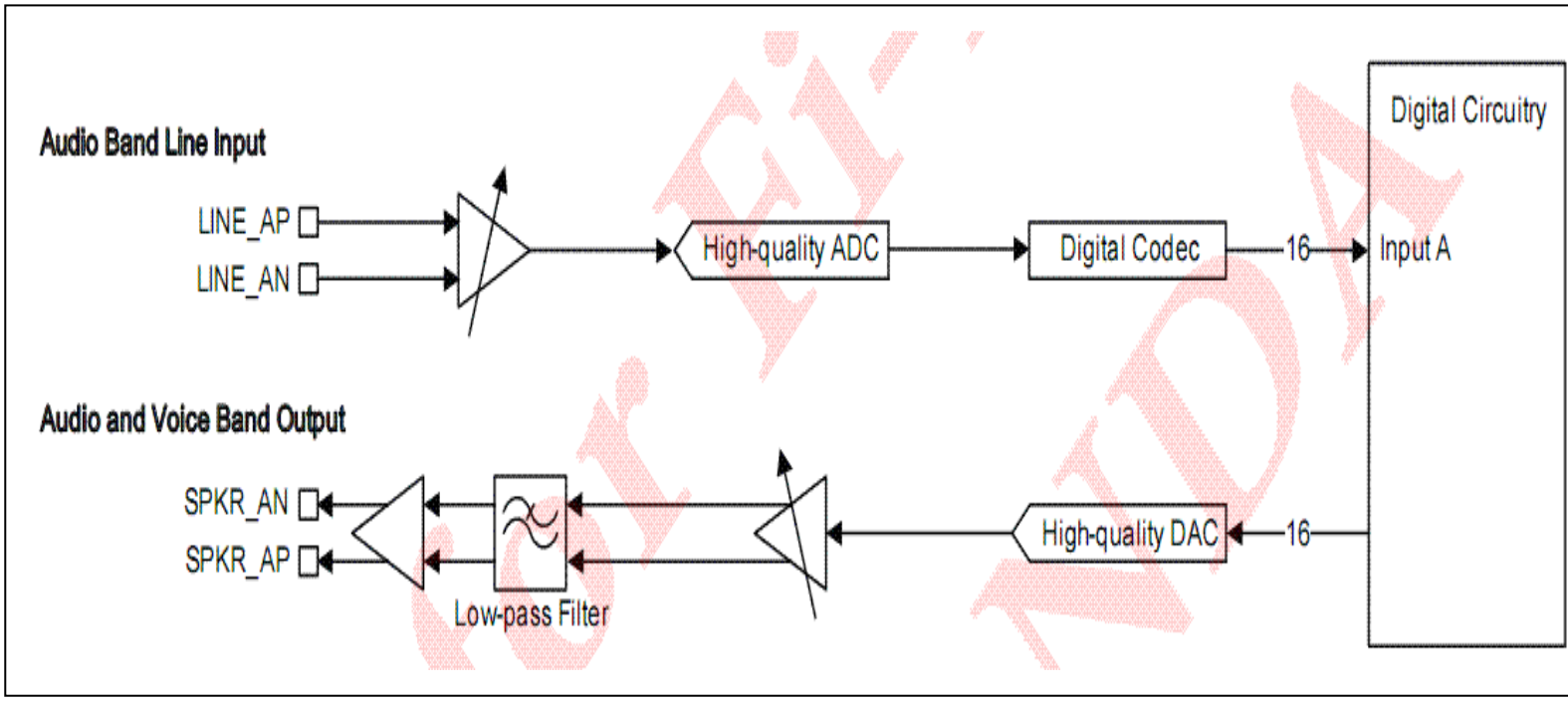


Figure 5

The CSR8605 QFN audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO for the audio circuits and VDD_AUDIO_DRV for the audio driver circuits.

5.2.1 ADC

- The ADC has a second-order Sigma-Delta converter.
- There are 2 gain stages for the ADC, 1 of which is an analogue gain stage

and the other is a digital gain stage.

5.2.2 ADC Pre-amplifier and ADC Analogue Gain

CSR8605 QFN has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

■ The ADC pre-amplifier has 4 gain settings: 0dB, 9dB, 21dB and 30dB

■ The ADC analogue amplifier gain is -3dB to 12dB in 3dB steps

■ The overall analogue gain for the pre-amplifier and analogue amplifier is -3dB to 42dB in 3dB steps.

■ Us a low gain levels for an audio line level amplifier

5.2.3 ADC Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see Table 9.2. There is also a fine gain interface

with a 9-bit gain setting allowing gain changes in 1/32 steps, for more information contact

CSR. The firmware controls the audio input gain.

5.2.4 DAC

The DAC consists of:

■ 1 fourth-order Sigma-Delta converter, see Figure 9.2

■ 2 gain stages, 1 of which is an analogue gain stage and the other is a digital gain stage

5.2.5 DAC Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB, see Table 9.3. There is also a fine gain interface
with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact CSR.

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

5.2.6 Line Input

In the line input mode the input impedance varies from 6kΩ to 30kΩ, depending on the volume setting. Figure 9.4 and Figure 9.5 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

5.2.7 Audio Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 9.6 shows that the output is available as a differential signal between SPKR_AN and SPKR_AP.

5.3 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

5.4 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

5.5 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

5.6 Serial Interfaces

5.6.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

Note: The serial port interface(UART)can be used for system debugging. Don't support to use command set for profile function application by UART, such as HFP/A2DP/AVRCP and so on. These profiles function application can be controlled only by PIO ,such as pairing/connect/answer/play/pause/next/previous function application and so on.

5.6.2 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

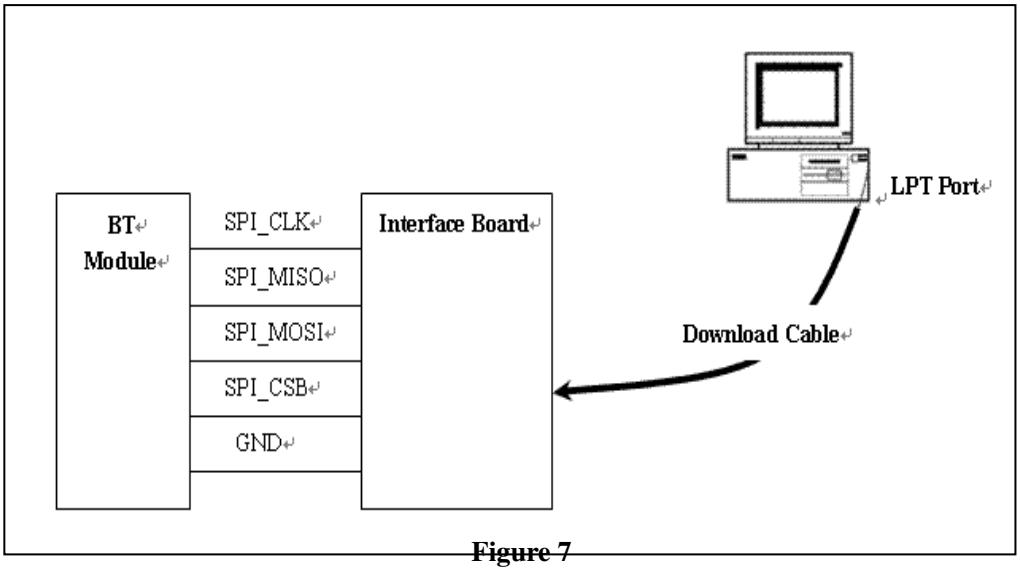


Figure 7

6. ELECTRICAL CHARACTERISTIC

Note:

For all I/O terminal characteristics:

■ Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

6.1 Absolute Maximum Rating

Rating		Mi	Max	Uni
Storage temperature		-40	105	°C
Supply Voltage				
Charger	VCHG	-0.4	5.75 / 6.50(a)	V
LEDs	LED[2:0]	-0.4	4.40	V
Battery	VBAT	-0.4	4.40	V
	VREGENABLE	-0.4	4.40	V
USB	VDD_USB	-0.4	3.6	V
1.8V	VDD_AUDIO_DRV	-0.4	1.95	V
	VDD_AUX_1V8	-0.4	1.95	V
	VDD_PADS_1	-0.4	3.60	V
	VDD_PADS_2	-0.4	3.60	V
	VDD_AUX_1V8	-0.4	1.95	V
1.35V	SMPS_1V35_SENSE	-0.4	1.45	V
	VDD_AUDIO	-0.4	1.45	V
	VREGIN_DIG	-0.4	1.95	V
Other terminal voltages		VSS - 0.4	VDD + 0.4	V

Table 1

6.2 Recommended Operating Conditions

Rating		Mi	Typ	Max	Uni
Operating temperature range		-40	20	85	°C
Supply Voltage					
Charger	VCHG	4.75 / 3.10(a)	5.00	5.75 / 6.50(b)	V
LEDs	LED[2:0]	1.10	3.70	4.30	V
Battery	VBAT	0	3.70	4.25	V
	VREGENABLE	0	3.70	4.25	V
USB	VDD_USB	3.1	3.3	3.6	V
1.8V	VDD_AUDIO_DRV	1.70	1.80	1.95	V
	VDD_AUX_1V8	1.70	1.80	1.95	V
	VDD_PADS_1	1.70	1.80	3.60	V
	VDD_PADS_2	1.70	1.80	3.60	V
	VDD_AUX_1V8	1.25 Table 2	1.80	1.95	V
1.35V	SMPS_1V35_SENSE	1.30	1.35	1.45	V
	VDD_AUDIO	1.30 Table 2	1.35	1.45	V
	VREGIN_DIG	1.30	1.35 or 1.80(c)	1.95	V

6.3 Input/output Terminal Characteristics

6.3.1 Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	Conditions		Mi	Typ	Max	Uni
Resolution	-		-	-	16	Bits
Input Sample Rate,	-		8	-	48	kHz
Maximum ADC	0dB = 1600mV$_{pk-pk}$		13	-	2260	mV$_{pk-pk}$
SNR	f_{in} = 1kHz B/W = 20Hz→F_{sample}/2 (20kHz max) A-Weighted	F_{sample}				
		8kHz	-	93.5	-	dB
		16kHz	-	92.5	-	dB
		32kHz	-	91.4	-	dB
		44.1kHz	-	90.4	-	dB
		48kHz	-	89.6	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz→F_{sample}/2 (20kHz max)	F_{sample}				
		8kHz	-	0.0041	-	%
		48kHz	-	0.0072	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB		-3	-	42	dB

Table 3

6.3.2 Codec: Digital to Analogue Converter

Digital to Analogue Converter							
Parameter	Conditions			Mi	Typ	Max	Uni
Resolution	-			-	-	16	Bits
Output Sample Rate Frequency	-			8	-	96	kHz
SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.1%	F_{sample}	Load				
		48kHz	100kΩ	-	95.6	-	dB
		48kHz	32Ω	-	95.8	-	dB
		48kHz	16Ω	-	95.6	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz→20kHz 0dBFS input	F_{sample}	Load				
		8kHz	100kΩ	-	0.0025	-	%
		8kHz	32Ω	-	0.0056	-	%
		8kHz	16Ω	-	0.0108	-	%
		48kHz	100kΩ	-	0.0027	-	%
		48kHz	32Ω	-	0.0067	-	%
		48kHz	16Ω	-	0.0122	-	%
Digital Gain	Digital Gain Resolution = 1/32			-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB			-21	-	0	dB
Output voltage full- scale swing	-			-	-	778	mV rms

Table 4

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

2F Friday March 09, 2012 10:21:21

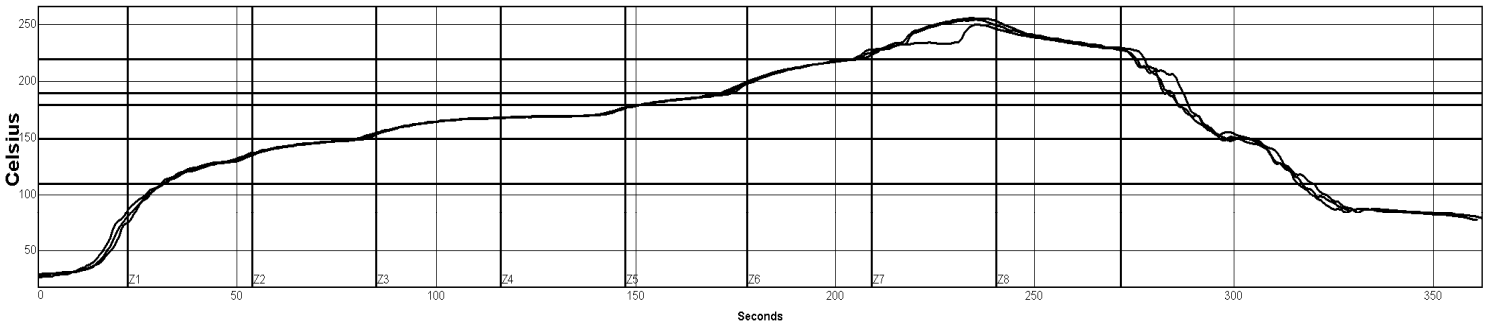
Site:

Oven Name: WQ Process Window Name: 无铅

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8
Top	140	150	170	170	190	225	265	230
Bottom	140	150	170	170	190	225	265	230

Conveyor Speed (cm/min): 75.0



PWI= 304%	Max Rising Slope		Preheat 110-190C		Soak Time 150-180C		Reflow Time /220C		Peak Temp	
2	3.9	189%	141.4	157%	70.4	-296%	71.1	111%	254.8	97%
3	4.0	197%	139.7	149%	70.6	-294%	70.3	103%	250.6	11%
4	3.9	192%	142.1	160%	69.6	-304%	71.2	112%	256.5	130%

Process Window:

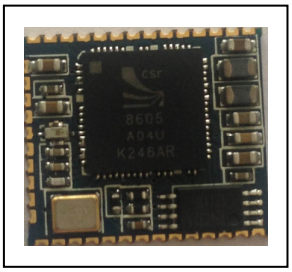
Solder Paste: SYSTEM DEFAULT

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.0)	0.0	3.0	Degrees/Second
Preheat Time 110-190C	90	130	Seconds
Soak Time 150-180C	90	110	Seconds
Time Above Reflow - 220C	50	70	Seconds
Peak Temperature	245	255	Degrees Celsius

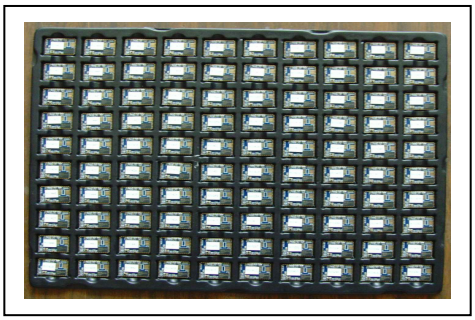
Description:

8. PACKAGING INFORMATION

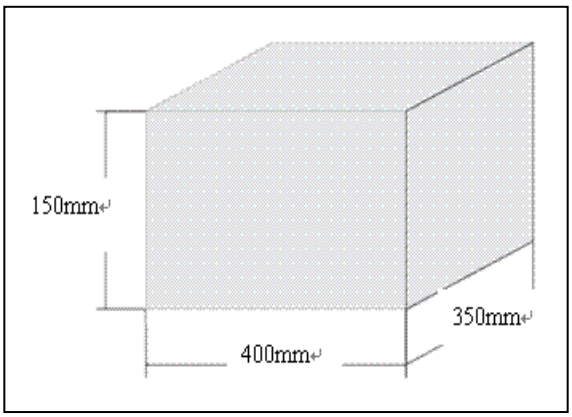
1. BLUETOOTH® Module: BTM8605



2. Assembly



3. Dimension



All rights are strictly reserved. Any portion of this paper shall not be reproduced, copied, or translated to any other forms without permission from Buddies Technology Limited.