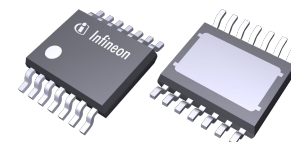


MOTIX™ full-bridge ICs for BDC motors

Features

- Path resistance of typ. 175 mΩ at 25°C
- Pulse current:
 - 5.2 A for $t_{\text{pulse}} \leq 1$ s at 85°C
 - 4.2 A for $t_{\text{pulse}} \leq 10$ s at 85°C
- Supply voltage range from 7 V to 18 V
- Extended supply voltage range from 4.5 V to 40 V
- Current limitation of min. 10 A
- Slew rate selection
- Protection and diagnostics: overcurrent, undervoltage, overtemperature, open load detection, current sense, cross current protection
- Status flag diagnosis with feedback of current sense
- SPI interface in BTM9011EP
- Half-bridge mode
- Green product (RoHS compliant)
- ISO ready



Potential applications

- Automotive unidirectional and bidirectional brushed DC motors
- Door modules
- Mirror modules
- Body control modules
- Other inductive or resistive loads in the automotive field

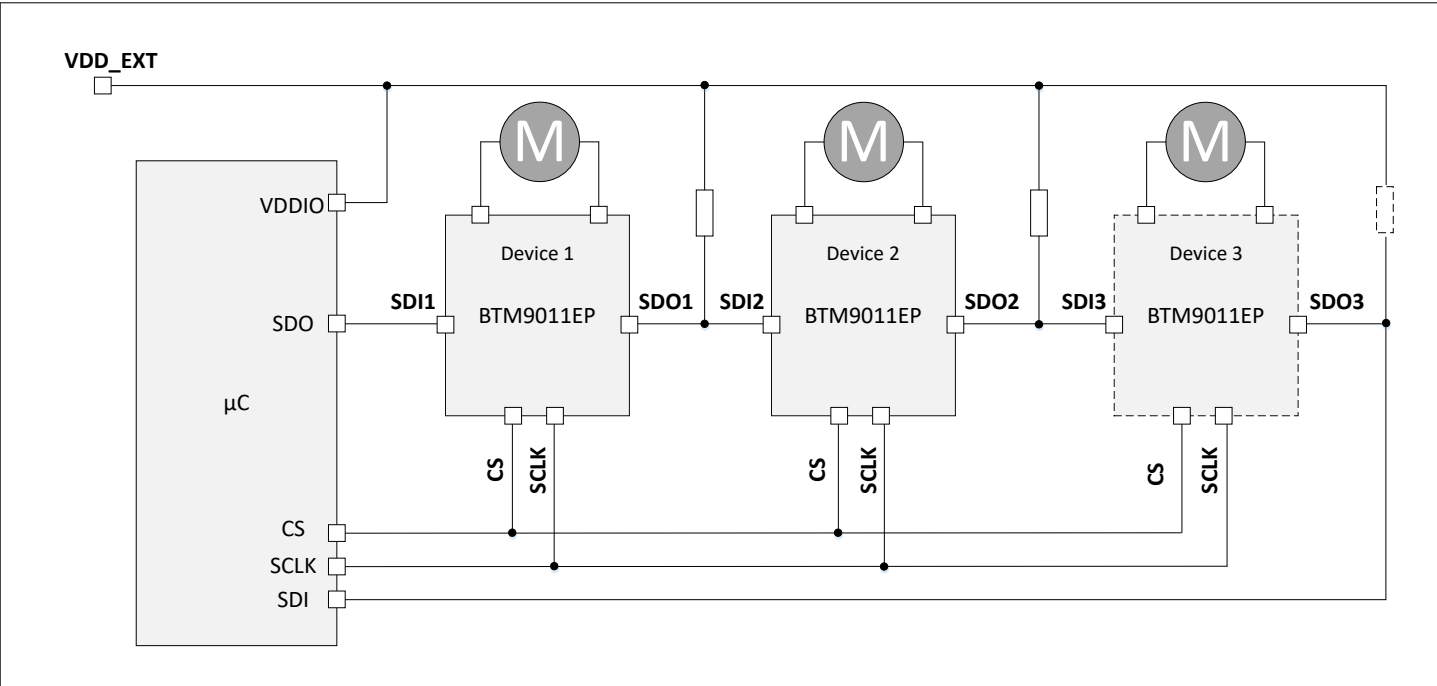
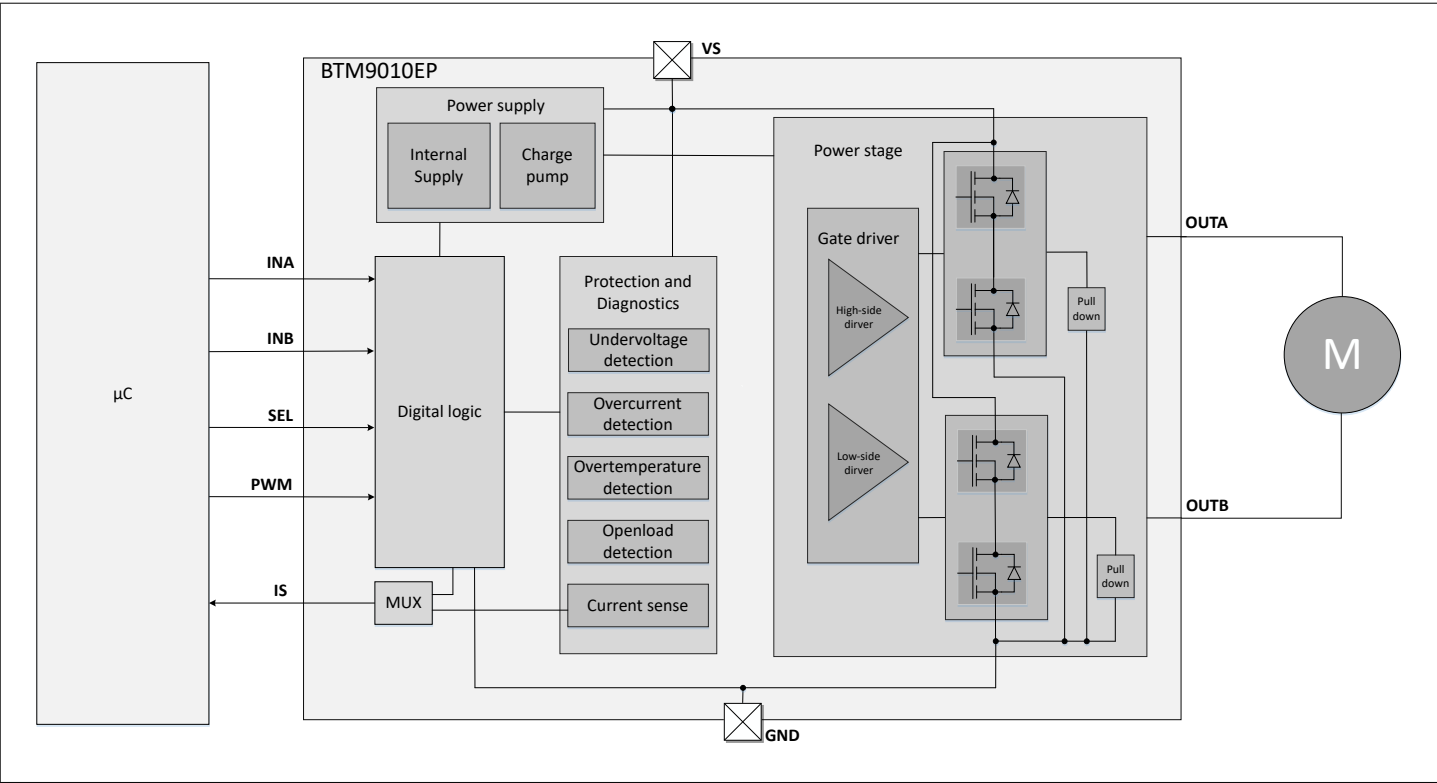
Product validation

- Qualified for automotive applications
- Product validation according to AEC-Q100

Product description

MOTIX™ BTM9010EP/BTM9011EP integrated full-bridge IC is an integrated full-bridge for automotive motor drive applications. This monolithic device is implemented in BCD technology, and assembled in PG-TSDSO-14 which has an exposed pad to ensure better thermal performance.

The device provides intelligent protection features against overtemperature, undervoltage, overcurrent, short circuit and crosscurrent. Moreover, the device also provides current sense and open load diagnostic as diagnosis features. The information of the output current and the error flag is presented at IS pin.



Product type	Package	Marking
BTM9010EP	PG-TSDSO-14	BTM9010
BTM9011EP	PG-TSDSO-14	BTM9011

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1 Device comparison

This table summarizes the differences between BTM9010EP and BTM9011EP.

	HW variant (BTM9010EP)	SPI variant (BTM9011EP)
Package	PG-TSDSO-14	PG-TSDSO-14
Digital interface	INA, INB, SEL, PWM	SDI, SCLK, CS, SDO
Path resistance	175 mΩ at 25°C	175 mΩ at 25°C
Current limitation	Min. 10 A	Min. 10 A
Overcurrent protection	Error flag at IS pin; Latched	Error flag at IS pin; OCx bit latched in the status byte; Dedicate bit for each half-bridge
Slew rate selection	2 configurable slew rate levels: - Selected via input sequence - Read out at IS pin	2 configurable slew rate levels: - Selected via SR bit in the control byte - Read out the control byte at SDO pin
Undervoltage shutdown	No sense current flowing out from IS pin; No error flag; Unlatched	No sense current flowing out from IS pin; No error flag; UV bit set but unlatched in the status byte
Overtemperature protection	Error flag at IS pin; Unlatched	Error flag at IS pin; TSDx bit set but unlatched in the status byte; Dedicate bit for each half-bridge
Open load detection	Error flag at IS pin; Unlatched	Error flag at IS pin; OL bit set but unlatched in the status byte
Current sense	Provided at IS pin	Provided at IS pin
Enter to standby mode	All inputs (INA, INB, SEL and PWM) are set to Low	EN bit is set to Low

2 Block diagram

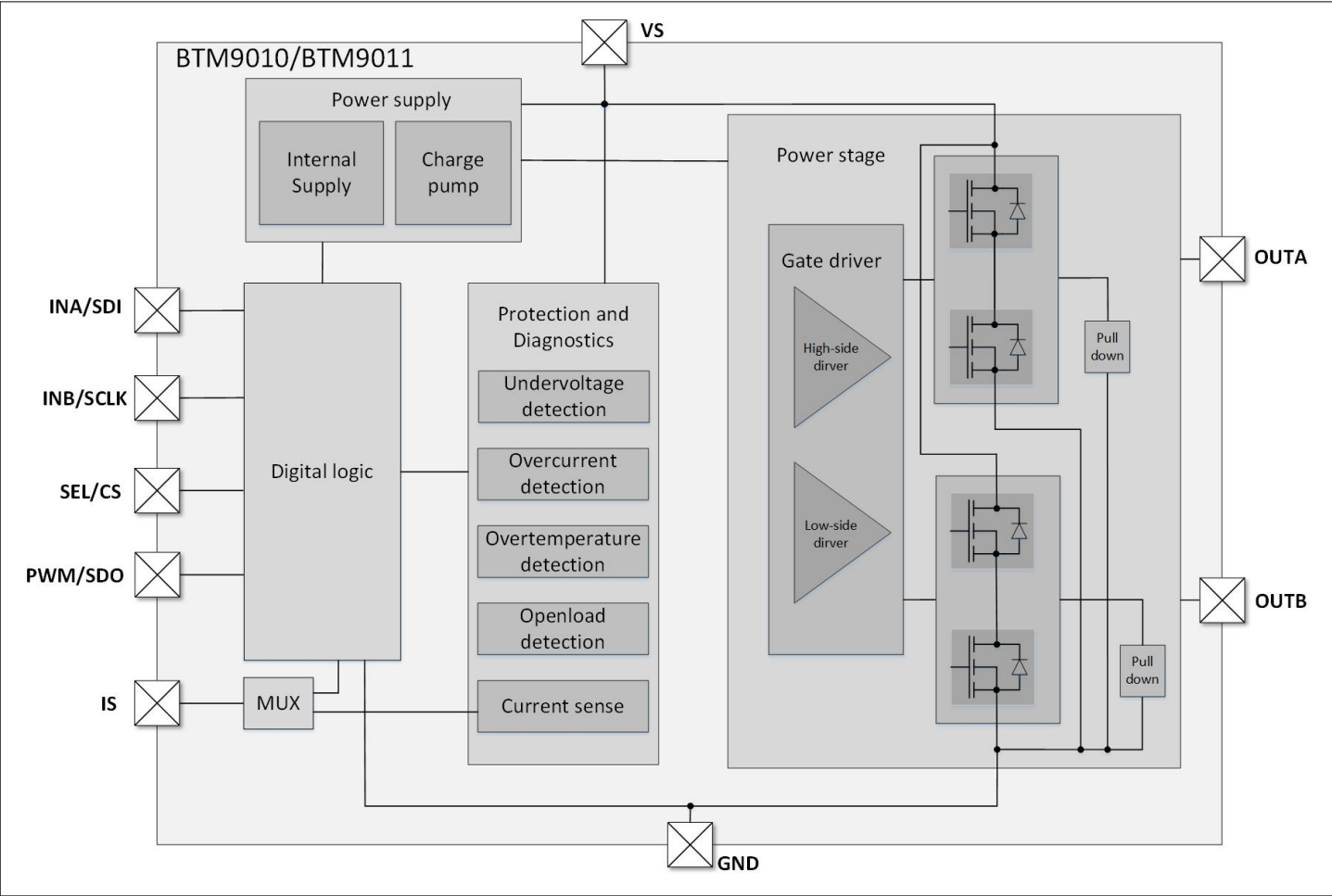


Figure 1 Block diagram

3 Pin configuration

3.1 HW variant

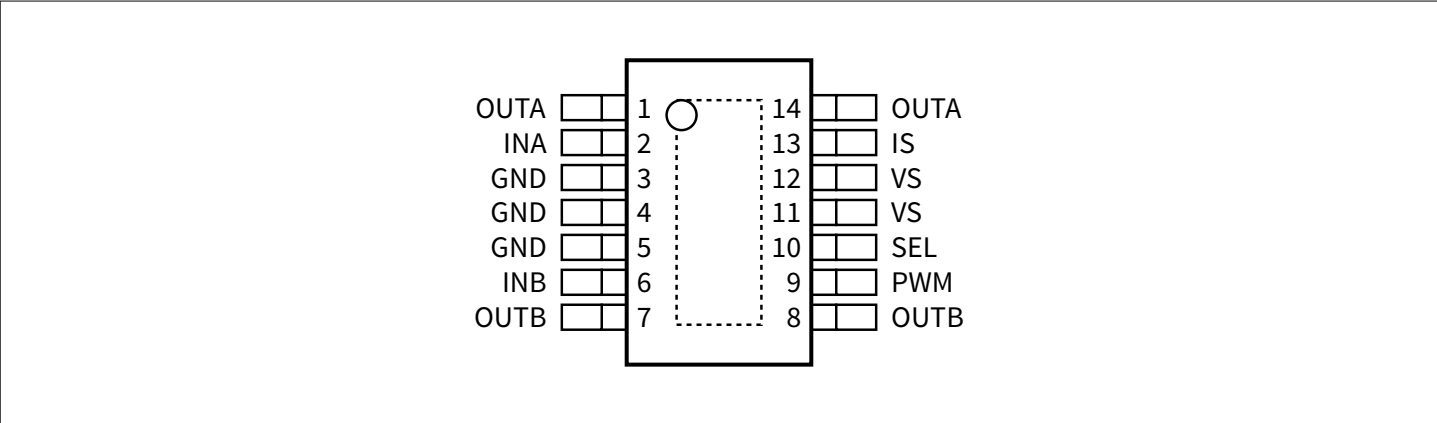


Figure 2 Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Function
1, 14	OUTA	Power output of the half-bridge A. All OUTA pins should be externally connected together.
2	INA	Input control combine with INB and PWM, refer to operative condition table
3, 4, 5	GND	Power ground. All ground pins should be externally connected together.
6	INB	Input control combine with INA and PWM, refer to operative condition table
7, 8	OUTB	Power output of the half-bridge B. All OUTB pins should be externally connected together.
9	PWM	Input control combine with INA and PWM, refer to operative condition table
10	SEL	Current sense selection pin
11, 12	VS	Power supply. All VS pins should be externally connected together.
13	IS	Current sense and error flag pin
EDP	–	Exposed die pad. For cooling and EMC purposes only. Not usable as electrical ground. Electrical ground must be provided by pins 3, 4 and 5. It is recommended to connect the EDP to ground.

3.2 SPI variant

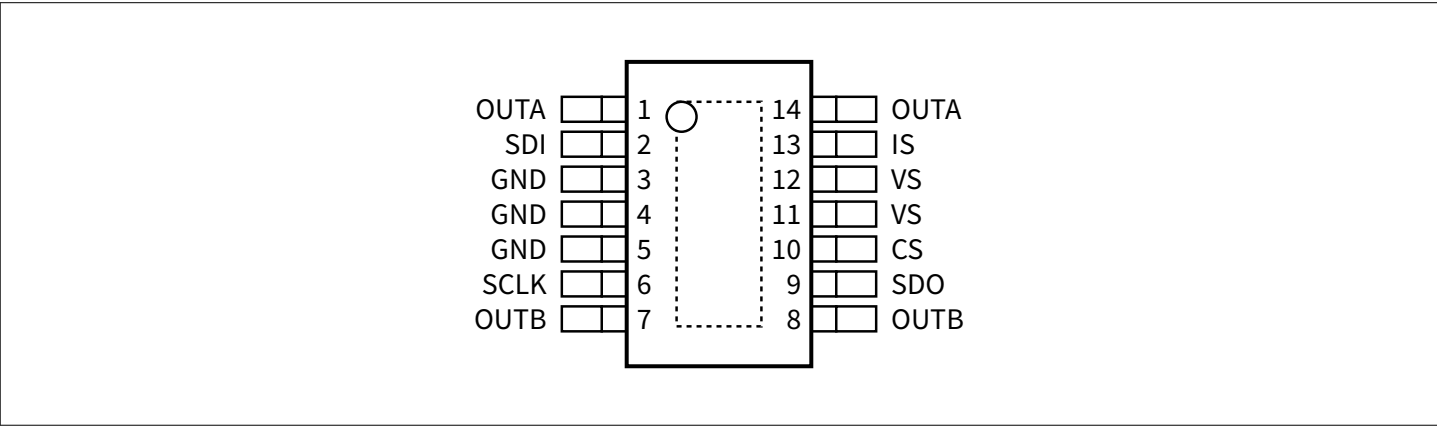


Figure 3 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	Function
1, 14	OUTA	Power output of the half-bridge A; All OUTA pins should be externally connected together.
2	SDI	Serial data input with internal pull down
3, 4, 5	GND	Power ground; All ground pins should be externally connected together.
6	SCLK	Serial clock input with internal pull down
7, 8	OUTB	Power output of the half-bridge B; All OUTB pins should be externally connected together.
9	SDO	Serial data output with open drain
10	CS	Chip select input with internal pull down
11, 12	VS	Power supply; All VS pins should be externally connected together.
13	IS	Current sense and error flag pin
EDP	–	Exposed die pad; For cooling and EMC purposes only; Not usable as electrical ground; Electrical ground must be provided by pins 3, 4 and 5. It is recommended to connect the EDP to ground.

4 General product characteristics

The device is intended to be used in an automotive environment.

4.1 Absolute maximum ratings

Stress above the absolute maximum ratings listed in this chapter may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum rating

$T_j = -40^{\circ}\text{C}$ to 150°C ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	P_GPC_01_1
Output voltage	V_{OUTX}	-0.3	–	$V_S + 0.3$	V	–	P_GPC_01_02
Voltage of logic pins	$V_{\text{INA}} / V_{\text{SDI}},$ $V_{\text{INB}} / V_{\text{SCKL}},$ $V_{\text{SEL}} / V_{\text{CS}},$ $V_{\text{PWM}} / V_{\text{SDO}}$	-0.3	–	$V_S + 6$	V	Note: Max. 40 V	P_GPC_01_03
Current sense pin	V_{IS}	-0.3	–	40	V	–	P_GPC_01_15
Voltage between VS and IS pin	V_{SIS}	-0.3	–	40	V	–	P_GPC_01_04
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_GPC_01_09
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_GPC_01_10
ESD susceptibility all pins (HBM)	$V_{\text{ESD(HBM, local)}}$	-2	–	2	kV	HBM ¹⁾	P_GPC_01_11
ESD susceptibility OUT vs GND, VS vs GND (HBM)	$V_{\text{ESD(HBM, global)}}$	-4	–	4	kV	HBM ¹⁾	P_GPC_01_12
ESD susceptibility all pins (CDM)	$V_{\text{ESD(CDM)}}$	-500	–	500	V	CDM ²⁾	P_GPC_01_13
ESD susceptibility corner pins (CDM)	$V_{\text{ESD(CDM, corner)}}$	-750	–	750	V	CDM ²⁾	P_GPC_01_14

1) ESD susceptibility, human body model (HBM), according to AEC Q100-002 (1.5 k Ω , 100 pF).

2) ESD susceptibility, charged device model (CDM), according to AEC Q100-011.

4.2 Functional range

The parameters of the functional range are listed in the table below:

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	7	–	18	V	–	P_GPC_02_01
Extended supply voltage range for operation	$V_{S(ext)}$	4.5	–	40	V	–	P_GPC_02_02
Junction temperature	T_j	-40	–	150	°C	–	P_GPC_02_03
HS / LS continous drain current	$I_{D(HS)}$ $I_{D(LS)}$	-3.4	–	3.4	A	¹⁾ $T_{amb} = 85^{\circ}\text{C}$	P_GPC_02_04
HS / LS pulsed drain current	$I_{pulse(HS)}$ $I_{pulse(LS)}$	-4.2	–	4.2	A	¹⁾ $t_{pulse} \leq 10\text{ s}$ $T_{amb} = 85^{\circ}\text{C}$	P_GPC_02_05
HS / LS pulsed drain current	$I_{pulse(HS)}$ $I_{pulse(LS)}$	-5.2	–	5.2	A	¹⁾ $t_{pulse} \leq 1\text{ s}$ $T_{amb} = 85^{\circ}\text{C}$	P_GPC_02_06
HS / LS pulsed drain current	$I_{pulse(HS)}$ $I_{pulse(LS)}$	-9.2	–	9.2	A	¹⁾ $t_{pulse} \leq 250\text{ ms}$ $T_{junc} = 25^{\circ}\text{C}$ ²⁾	P_GPC_02_07
Input voltage range for normal operation	$V_{INA(nor)} / V_{SDI(nor)}$, $V_{INB(nor)} / V_{SCLK(nor)}$, $V_{SEL(nor)} / V_{CS(nor)}$, $V_{PWM(nor)}$	-0.3	–	6.0	V	–	P_GPC_02_08

1) Based on thermal simulation using 2s2p with 600 mm² Cu (70 μm)

2) This pulsed drain current is defined for the inrush current when the load is at cold temperature $T_{Load} = -40^{\circ}\text{C}$

4.3 Thermal resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please go to [JEDEC](#) webpage.

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to ambient	R_{thJA}	–	33	–	K/W	¹⁾	P_GPC_03_01
Junction to case	R_{thJC}	–	2	–	K/W	–	P_GPC_03_02

4 General product characteristics

- 1) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Current consumption

Table 6 Current consumption

$V_S = 7\text{ V}$ to 18 V , $T_j = -40^\circ\text{C}$ to 150°C , $I_L = 0\text{ A}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply current in standby mode	I_{VS_STB}	–	–	5	μA	$V_{INA} = V_{INB} = 0\text{ V}$; $V_{SEL} = 0\text{ V}$; $V_{PWM} = 0\text{ V}$; $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$; $V_S = 13.5\text{ V}$	P_GPC_04_01
Supply current in standby mode	I_{VS_STB}	–	–	20	μA	$V_{INA} = V_{INB} = 0\text{ V}$; $V_{SEL} = 0\text{ V}$; $V_{PWM} = 0\text{ V}$; $T_j = 150^\circ\text{C}$; $V_S = 13.5\text{ V}$	P_GPC_04_03
Supply current in normal mode	$I_{VS(ON)}$	–	3	5	mA	In normal operation mode: $V_{INA} = 5\text{ V}$, $V_{INB} = 0\text{ V}$ or $V_{INA} = 0\text{ V}$, $V_{INB} = 5\text{ V}$; $V_{SEL} = X$; $V_{PWM} = 0\text{ V}$ or $V_{PWM} = 5\text{ V}$; No load is connected	P_GPC_04_04

5 Digital logic

INA is in general to control the high-side switch of the half-bridge A. INB is in general to control the high-side switch of the half-bridge B. PWM is used to control the low-side switches when the high-side is off. Please be informed that there are a few exceptions listed in the operative condition table to cover all use cases. Please check the input patterns refer to the [Table 7](#).

Table 7 Operative condition

Input pattern				Current sense/ Error flag	MOSFET status				Bridge mode
INA	INB	PWM	SEL	IS	HSA	LSA	HSB	LSB	
0	0	0	0	Hi-Z	off	off	off	off	pull-down resistance is connected; outputs are grounded ¹⁾
0	0	0	1	error flag: short to GND	off	off	off	off	pull-up resistance is connected short to GND diagnosis
0	0	1	0	current sense: LSB	off	on	off	on	slow decay/break LS
0	0	1	1	current sense: LSA	off	on	off	on	slow decay/break LS
0	1	0	0	current sense: HSB	off	off	on	off	fast decay HSB/off
0	1	0	1	error flag: open load	off	off	on	off	fast decay HSB/open load diagnosis; pull-down resistance at OUTA is connected
0	1	1	0	current sense: HSB	off	on	on	off	forward
0	1	1	1	current sense: LSA	off	on	on	off	forward
1	0	0	0	error flag: open load	on	off	off	off	fast decay HSA/open load diagnosis; pull-down resistance at OUTB is connected
1	0	0	1	current sense: HSA	on	off	off	off	fast decay HSA/off
1	0	1	0	current sense: LSB	on	off	off	on	reverse
1	0	1	1	current sense: HSA	on	off	off	on	reverse
1	1	0	0	current sense: HSB	on	off	on	off	slow decay/break HS
1	1	0	1	current sense: HSA	on	off	on	off	slow decay/break HS
1	1	1	0	current sense: LSB	off	off	off	on	Half-bridge A in tri-state
1	1	1	1	current sense: LSA	off	on	off	off	Half-bridge B in tri-state

Note: For SPI variant the inputs in the table are mapped to the dedicate bits in SPI protocol.
For SPI variant when EN bit is set to 0, the device will enter to standby mode.

1) $V_{SEL} \leq 0.25 \text{ V}$.

Table 8 Fault conditions

Digital input pins				IS	Comment
INA	INB	PWM	SEL		
0	0	0	1	$I_{IS(FAULT)}$	Short to GND is detected

(table continues...)

Table 8 (continued) Fault conditions

Digital input pins				IS	Comment
INA	INB	PWM	SEL		
0	0	1	0/1	$I_{IS(FAULT)}$	Error flagged; low side A/B latched off in OC condition
0	1	0	0	$I_{IS(FAULT)}$	Error flagged; high side B latched off in OC condition
0	1	0	1	$I_{IS(FAULT)}$	Open load is detected
0	1	1	0/1	$I_{IS(FAULT)}$	Error flagged; high side B or low side A latched off in OC condition
1	0	0	0	$I_{IS(FAULT)}$	Open load is detected
1	0	0	1	$I_{IS(FAULT)}$	Error flagged; high side A latched off in OC condition
1	0	1	0	$I_{IS(FAULT)}$	Error flagged; high side A or low side B latched off in OC condition
1	1	0	0	$I_{IS(FAULT)}$	Error flagged; high side A/B latched off in OC condition
1	1	1	0	$I_{IS(FAULT)}$	Error flagged; low side B latched off in OC condition
1	1	1	1	$I_{IS(FAULT)}$	Error flagged; low side A latched off in OC condition

Note: For SPI variant the inputs in the table are mapped to the dedicate bits in SPI protocol.
The error flags can be read out either at IS pin or via SDO pin.

5.1 Control inputs

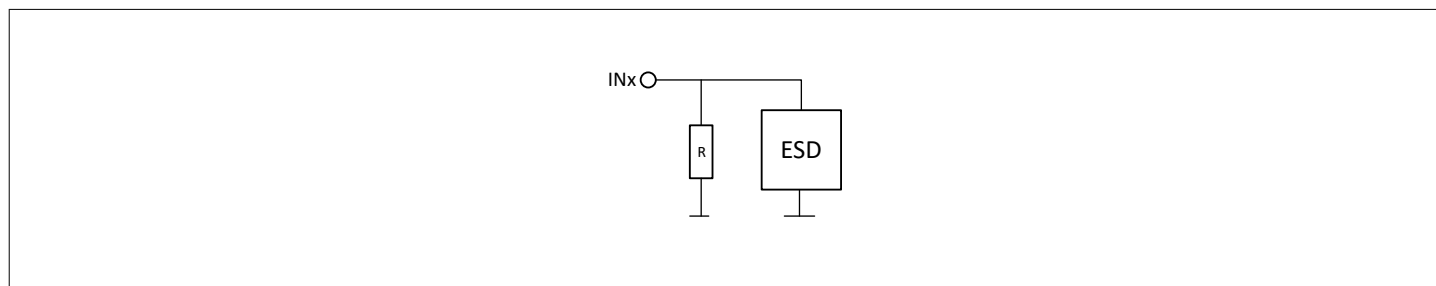


Figure 4 Input structure

Table 9 Electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level voltage INA / SDI, INB / SCLK, SEL / CS, PWM	$V_{INA(L)} / V_{SDI(L)}$, $V_{INB(L)} / V_{SCLK(L)}$, $V_{PWM(L)}$, $V_{SEL(L)} / V_{CS(L)}$	1.0	1.3	–	V	1)	P_INP_01_01
High level voltage INA / SDI, INB / SCLK, SEL / CS, PWM	$V_{INA(H)} / V_{SDI(H)}$, $V_{INB(H)} / V_{SCLK(H)}$, $V_{PWM(H)}$, $V_{SEL(H)} / V_{CS(H)}$	–	1.6	2.1	V	–	P_INP_01_02

(table continues...)

Table 9 (continued) Electrical characteristics

$V_S = 7\text{ V}$ to 18 V , $T_j = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input voltage hysteresis	$V_{\text{INA(HYS)}} / V_{\text{SDI(HYS)}},$ $V_{\text{INB(HYS)}} / V_{\text{SCLK(HYS)}},$ $V_{\text{SEL(HYS)}} / V_{\text{CS(HYS)}},$ $V_{\text{PWM(HYS)}}$	–	400	–	mV	–	P_INP_01_03
Input current low level	$I_{\text{INA(L)}} / I_{\text{SDI(L)}}, I_{\text{INB(L)}} /$ $I_{\text{SCLK(L)}},$ $I_{\text{PWM(L)}}, I_{\text{SEL(L)}} /$ $I_{\text{PWM(L)}}$	2	4	6	μA	$V_{\text{INA}} / V_{\text{SDI}} = V_{\text{INB}} /$ $V_{\text{SCLK}} = V_{\text{PWM}} = V_{\text{SEL}} /$ $V_{\text{PWM}} = 1.0\text{ V}$ Refer to Figure 4	P_INP_01_04
Input current high level	$I_{\text{INA(H)}} / I_{\text{SDI(H)}}, I_{\text{INB(H)}} /$ $I_{\text{SCLK(H)}},$ $I_{\text{PWM(H)}}, I_{\text{SEL(H)}} / I_{\text{PWM(H)}}$	–	10	20	μA	$V_{\text{INA}} / V_{\text{SDI}} = V_{\text{INB}} /$ $V_{\text{SCLK}} = V_{\text{PWM}} = V_{\text{SEL}} /$ $V_{\text{PWM}} = 2.1\text{ V}$ Refer to Figure 4	P_INP_01_05

1) When $V_{\text{INA}}, V_{\text{INB}}, V_{\text{PWM}}$, or $V_{\text{SEL(L)}}$ is higher than 0.8 V , the devices will enter the normal operation mode from the standby mode, and consume higher quiescent current.

6 Power stages

6.1 Functional description

The power stage of the BTM9010EP / BTM9011EP consists of two half-bridges. All protection and diagnostic functions are applicable for each half-bridge.

The on-state resistance R_{ON} depends mainly on the junction temperature T_j . The typical on-state resistance characteristics are shown in Figure 5

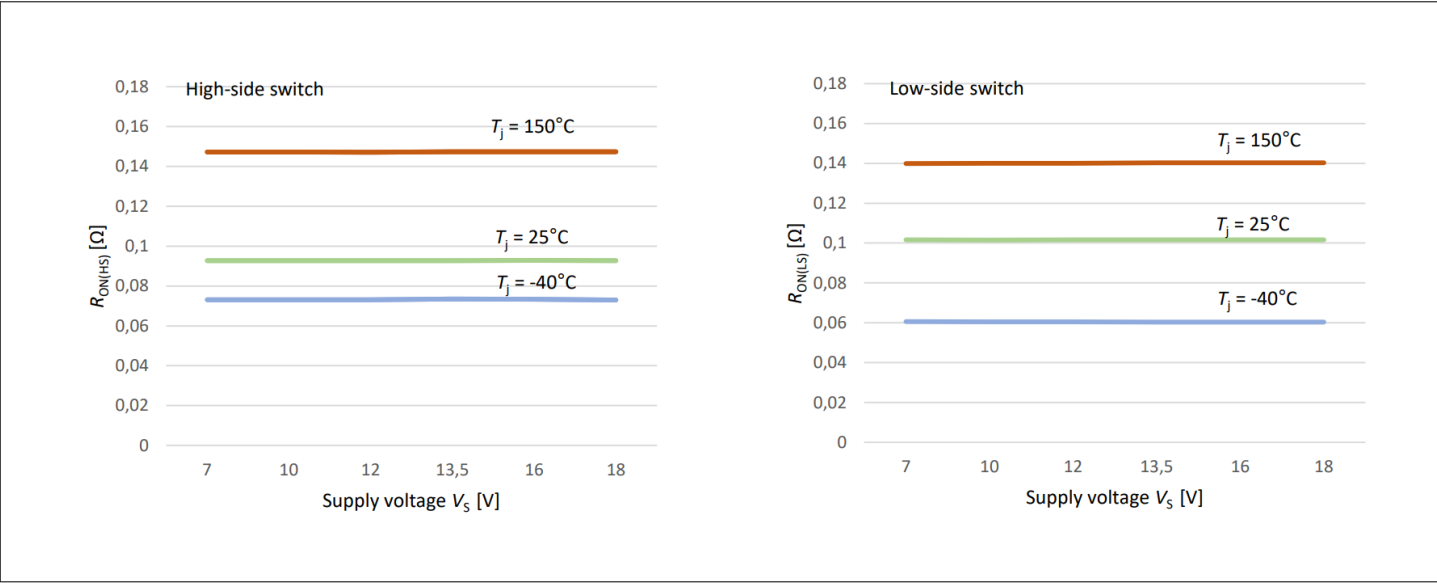


Figure 5 Typical ON-state resistance vs. supply voltage V_S

6.2 Switching time

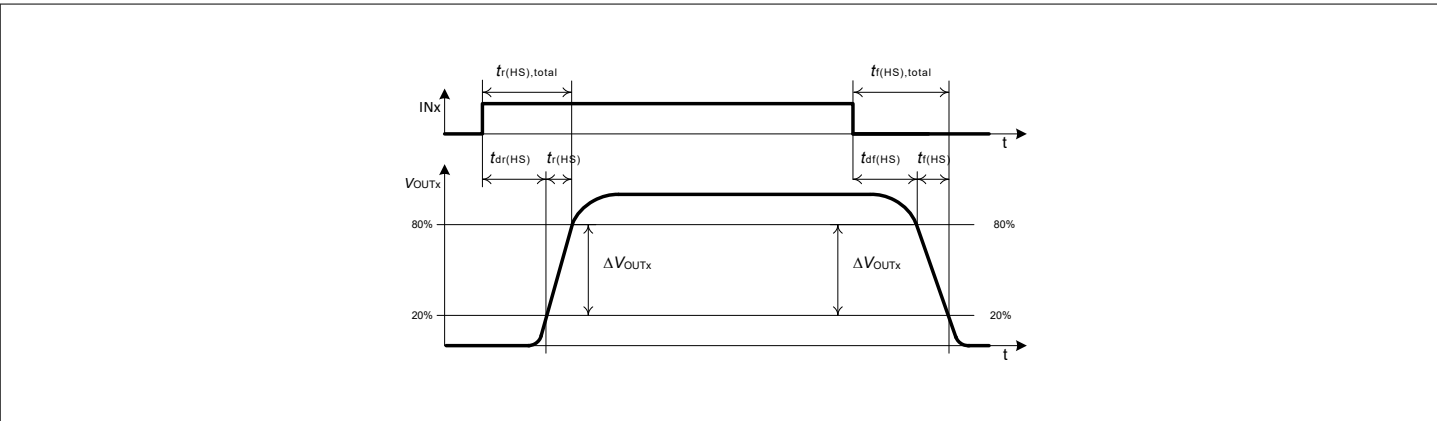


Figure 6 Definition of HS switching time without cross current protection time

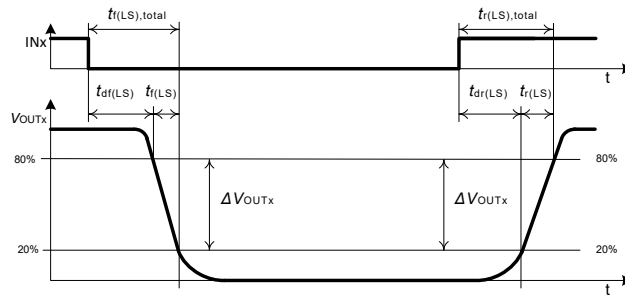


Figure 7 Definition of LS switching time without cross current protection time

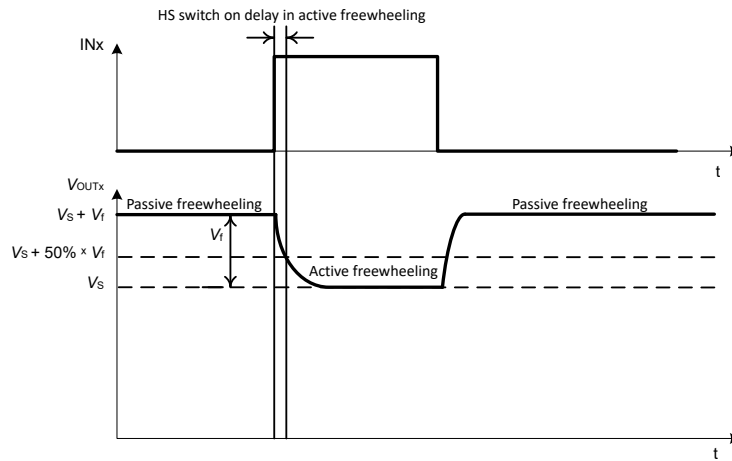


Figure 8 HS switch on delay in active freewheeling

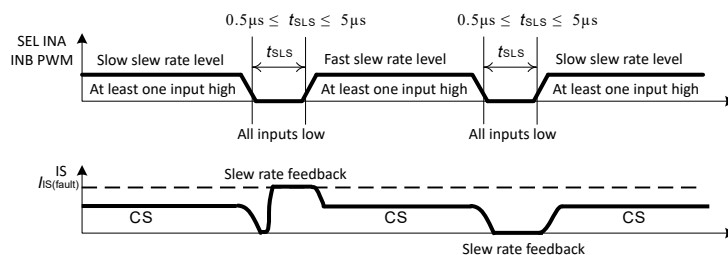
For SPI variant the INx signal in the figure is mapped to the input bits in SPI protocol. The INx will be updated at the CS falling edge.

6.3 Slew rate selection

6.3.1 HW variant

The slew rate is selected via input toggling as shown in [Figure 9](#). If more then one input signal is high, the next slew rate level will be selected when:

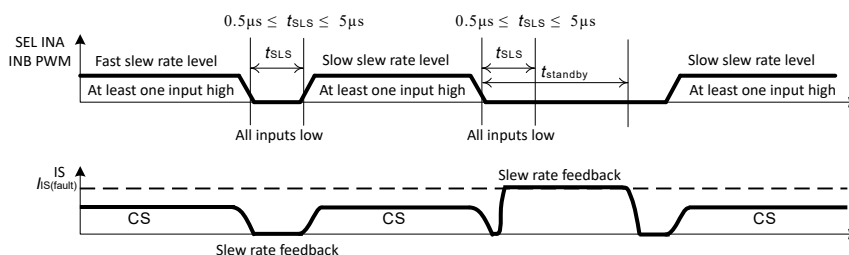
- All input signals are pulled down for the duration $0.5 \mu\text{s} \leq t_{\text{SLS}} \leq 5 \mu\text{s}$
- At least one input signal is pulled up after t_{SLS} expired


Figure 9 Slew rate selection

The slow slew rate is selected by default after power up.

As shown in [Figure 10](#) when all input signals are pulled down, the selected slew rate can be detected at IS pin before the standby mode blanking time is expired:

- Fast slew rate is selected, if the fault current $I_{IS(FAULT)}$ is present at IS pin
- Slow slew rate is selected, if no current is present at IS pin


Figure 10 Slew rate detection

6.3.2 SPI variant

The slew rate level is selected via the SR bit in the data byte sent to SDI:

- The fast slew rate is selected if the SR bit is set to 1
- The slow slew rate is selected if the SR bit is set to 0

The slew rate is reset to the slow slew rate level by default after power up.

The slew rate level is read out in the [control byte](#) via SDO when the SDO_SEL is set to 0.

6.4 Electrical characteristics

Table 10 Electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
On-state high-side resistance	$R_{ON(HS)}$	–	–	160	mΩ	$I_{OUT} = 2.5\text{ A}$; $V_S = 6\text{ V}$; $T_j = 150^\circ\text{C}$	P_PS_01_01

(table continues...)

Table 10 (continued) Electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
On-state high-side resistance	$R_{ON(HS)}$	–	87.5	–	m Ω	$I_{OUT} = 2.5\text{ A}$; $V_S = 6\text{ V}$; $T_j = 25^\circ\text{C}$	P_PS_01_25
On-state low-side resistance	$R_{ON(LS)}$	–	–	160	m Ω	$I_{OUT} = 2.5\text{ A}$; $V_S = 6\text{ V}$; $T_j = 150^\circ\text{C}$	P_PS_01_02
On-state low-side resistance	$R_{ON(LS)}$	–	87.5	–	m Ω	$I_{OUT} = 2.5\text{ A}$; $V_S = 6\text{ V}$; $T_j = 25^\circ\text{C}$	P_PS_01_26
Fast HS switch on delay time	$t_{dr1(HS)}$	0.3	0.6	1.1	μs	$R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_04
Slow HS switch on delay time	$t_{dr2(HS)}$	0.5	1	1.5	μs	$R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_23
Fast HS switch off delay time	$t_{df1(HS)}$	0.9	1.9	3.0	μs	$R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_05
Slow HS switch off delay time	$t_{df2(HS)}$	1.4	3.4	7.0	μs	$R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_22
Fast HS rise time	$t_{r1(HS)}$	0.35	0.6	1.1	μs	V_{OUTx} from 20% to 80% of V_S ; $R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_06
Slow HS rise time	$t_{r2(HS)}$	0.5	1.1	1.8	μs	V_{OUTx} from 20% to 80% of V_S ; $R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_20
Fast HS fall time	$t_{f1(HS)}$	0.07	0.25	0.5	μs	V_{OUTx} from 80% to 20% of V_S ; $R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_07
Slow HS fall time	$t_{f2(HS)}$	0.15	0.7	1.5	μs	V_{OUTx} from 80% to 20% of V_S ; $R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_21
Fast LS switch on delay time	$t_{df1(LS)}$	0.3	0.55	0.9	μs	$R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_08
Slow LS switch on delay time	$t_{df2(LS)}$	0.5	1	1.5	μs	$R_{Load} = 5.6\text{ }\Omega$; $V_S = 13.5\text{ V}$	P_PS_01_16

(table continues...)

Table 10 (continued) **Electrical characteristics**

$V_S = 7\text{ V}$ to 18 V , $T_j = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fast LS switch off delay time	$t_{dr1(LS)}$	1.0	1.8	2.6	μs	$R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_09
Slow LS switch off delay time	$t_{dr2(LS)}$	1.5	3.4	7.1	μs	$R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_17
Fast LS rise time	$t_{r1(LS)}$	0.15	0.4	0.7	μs	V_{OUTX} from 20% to 80% of V_S ; $R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_10
Slow LS rise time	$t_{r2(LS)}$	0.3	0.8	1.6	μs	V_{OUTX} from 20% to 80% of V_S ; $R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_18
Fast LS fall time	$t_{f1(LS)}$	0.15	0.45	0.7	μs	V_{OUTX} from 80% to 20% of V_S ; $R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_11
Slow LS fall time	$t_{f2(LS)}$	0.3	0.8	1.5	μs	V_{OUTX} from 80% to 20% of V_S ; $R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_19
Fast cross current protection time	t_{cross1}	2.5	3.3	5	μs	$R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_12
Slow cross current protection time	t_{cross2}	4.5	7	9.5	μs	$R_{Load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PS_01_24
Free wheeling diode forward voltage	V_f	–	0.8	0.9	V	$ I_{OUT} = 2\text{ A}$; $T_j = 150^\circ\text{C}$	P_PS_01_13
Slew rate selection time	t_{SLS}	0.5	–	5	μs	–	P_PS_01_15

7 Protection and diagnostics

7.1 HW variant

Both high-side and low-side switches are capable to detect an open load condition in their activated state.

7.1.1 Undervoltage shutdown

If the supply voltage drops below $V_{UV(OFF)}$ as shown in Figure 11, the device will

- Switch off the MOSFETs actively
- Keep the charge pump on
- Provide no output at current sense pin

Note: If the supply voltage drops below the power off reset voltage V_{S_POFFR} , the charge pump will be deactivated, and the slew rate will be set to default value.

If V_S rises above $V_{UV(ON)}$ as shown in Figure 11, the device will resume normal operation.

When the supply voltage rises above $V_{UV(ON)}$, the sense current I_S will be present at the I_S pin when the switch on delay and the current sense recovery time t_{IS} expires.

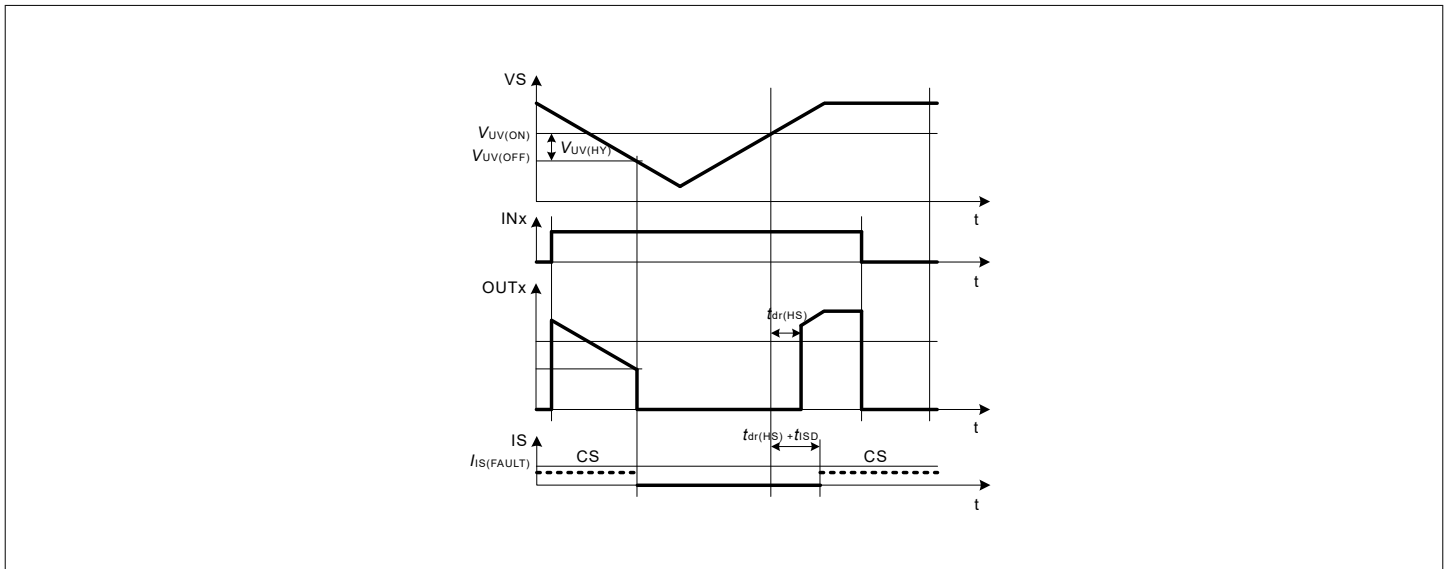


Figure 11 Timing diagram for undervoltage behavior

7.1.2 Overtemperature protection

This device is protected against overtemperature by the integrated temperature sensors. Overtemperature leads to a switch off of the output stages including the high-side and low-side switches.

If the temperature sensor reaches T_{JSD} for a duration longer than t_{OTF} , the device behaves as follows

- Switch off both high-side and low-side MOSFETs in dedicated half-bridge
- Keep the charge pump on
- Keep the switches off until the device resumes the normal operation when the junction temperature decreases below the threshold
- Provide $I_{IS(fault)}$ at I_S pin

The device resumes normal functionality once the temperature drops below thermal switch on junction temperature T_{Jso}

7.1.3 Overcurrent protection

7.1.3.1 Short circuit of output to supply or ground

The high-side switches are protected against short to ground whereas the low-side switches are protected against short to supply.

If the current within the switch exceeds the corresponding overcurrent detection threshold I_{SD_xx} , the device will

- Enter into an overcurrent condition
- Start the overcurrent shutdown filter time t_{dOC_xx}
- Limit the current to the current limitation I_{LIM_xx}

When the overcurrent shutdown is triggered, the device will

- Latch off
- Provide $I_{IS(fault)}$ at IS pin
- Switch on the MOSFETs by input pulse (PWM, INA and INB) as shown in [Figure 14](#)

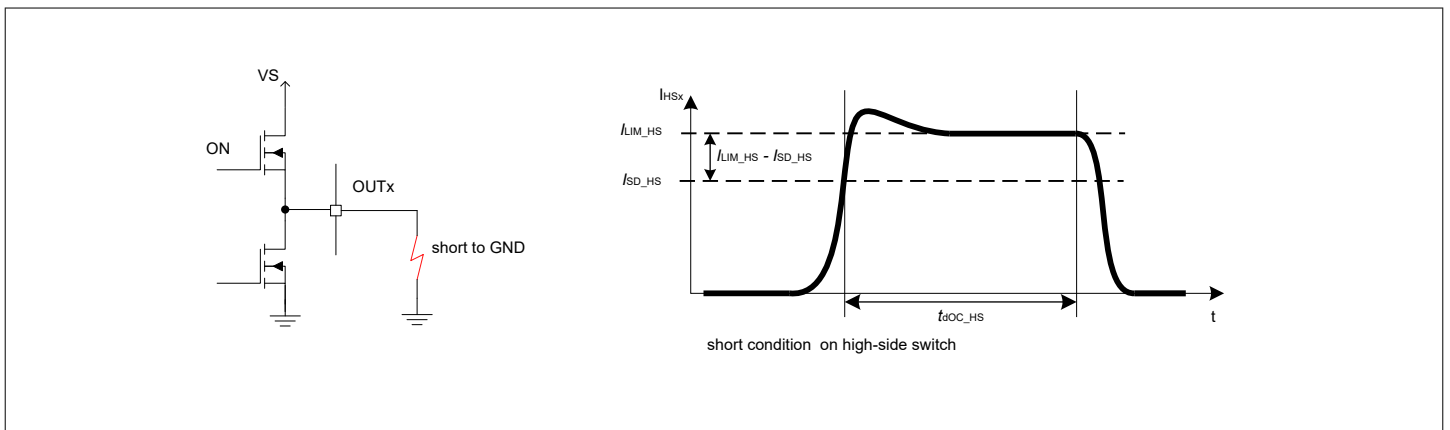


Figure 12 High-side switch short circuit and overcurrent protection

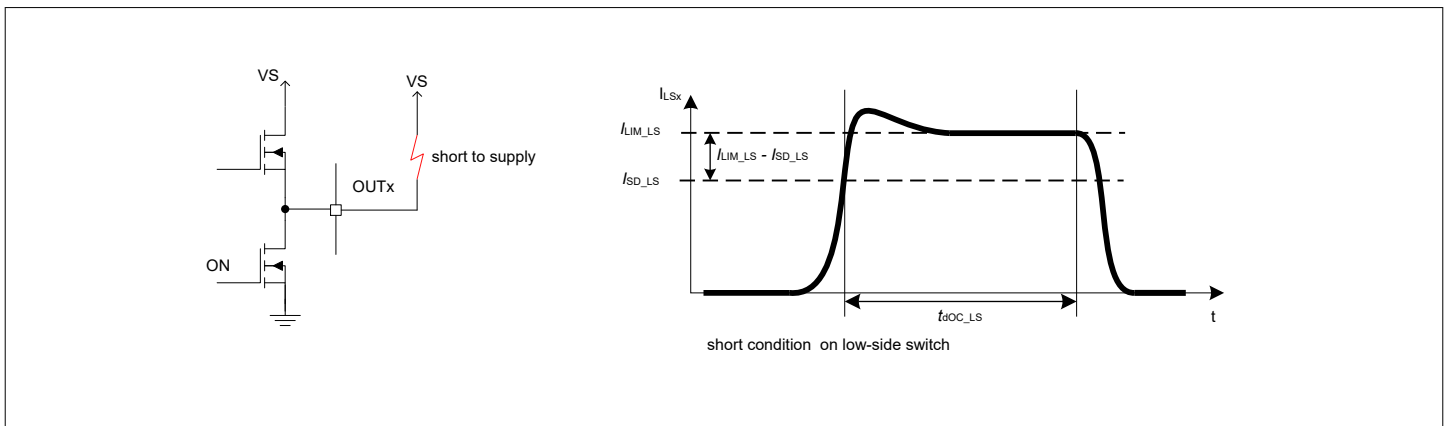


Figure 13 Low-side switch short circuit and overcurrent protection

The high-side current limitation is always higher than the low-side current limitation.

7.1.3.2 Recovery to normal operation

As shown in Figure 14 the recovery will be controlled by the input patterns.

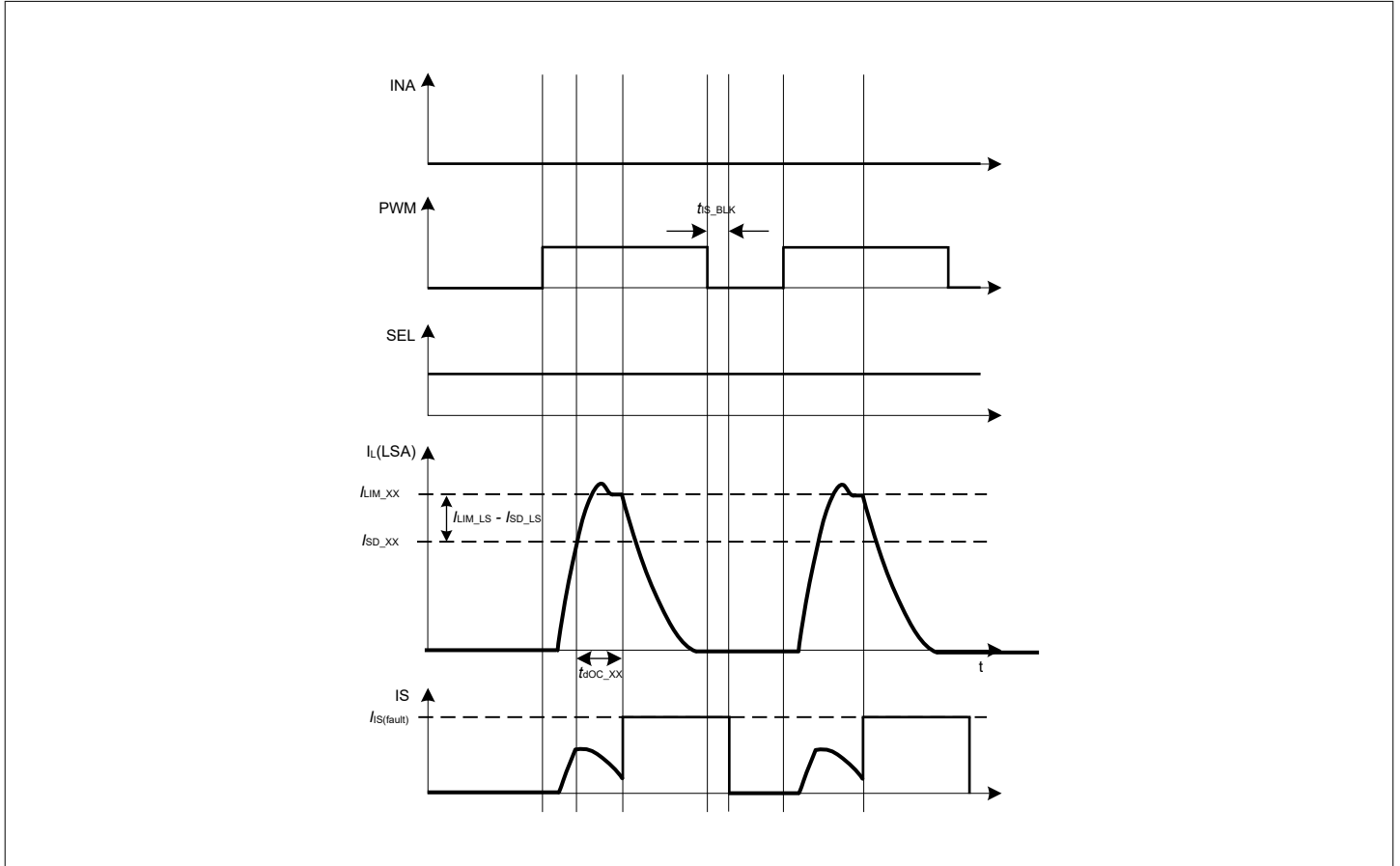
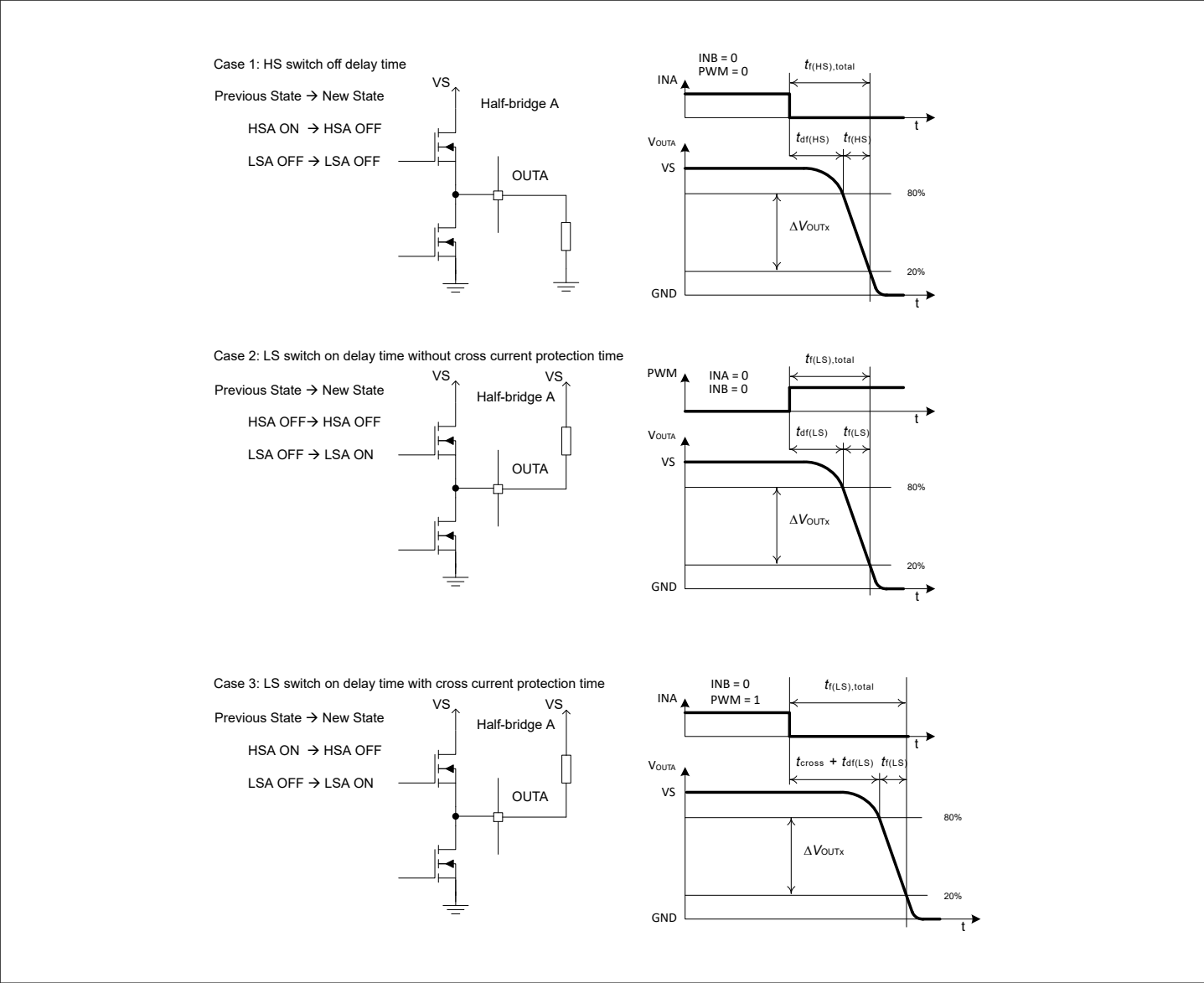


Figure 14 Recovery of short circuit and overcurrent protection by input pattern

7.1.4 Cross current protection

The high-side and low-side MOSFETs are ensured never to be simultaneously “ON” to avoid cross currents. This is achieved by integrating delays in the driver stage of the power outputs to create a cross current protection time between switching off one of the MOSFETs and switching on the adjacent MOSFET within the half-bridge. The cross current protection time, t_{cross1} and t_{cross2} , as shown in Figure 15 and Figure 16, have been specified to ensure that the switching slopes do not overlap with each other. This prevents a cross conduction event.



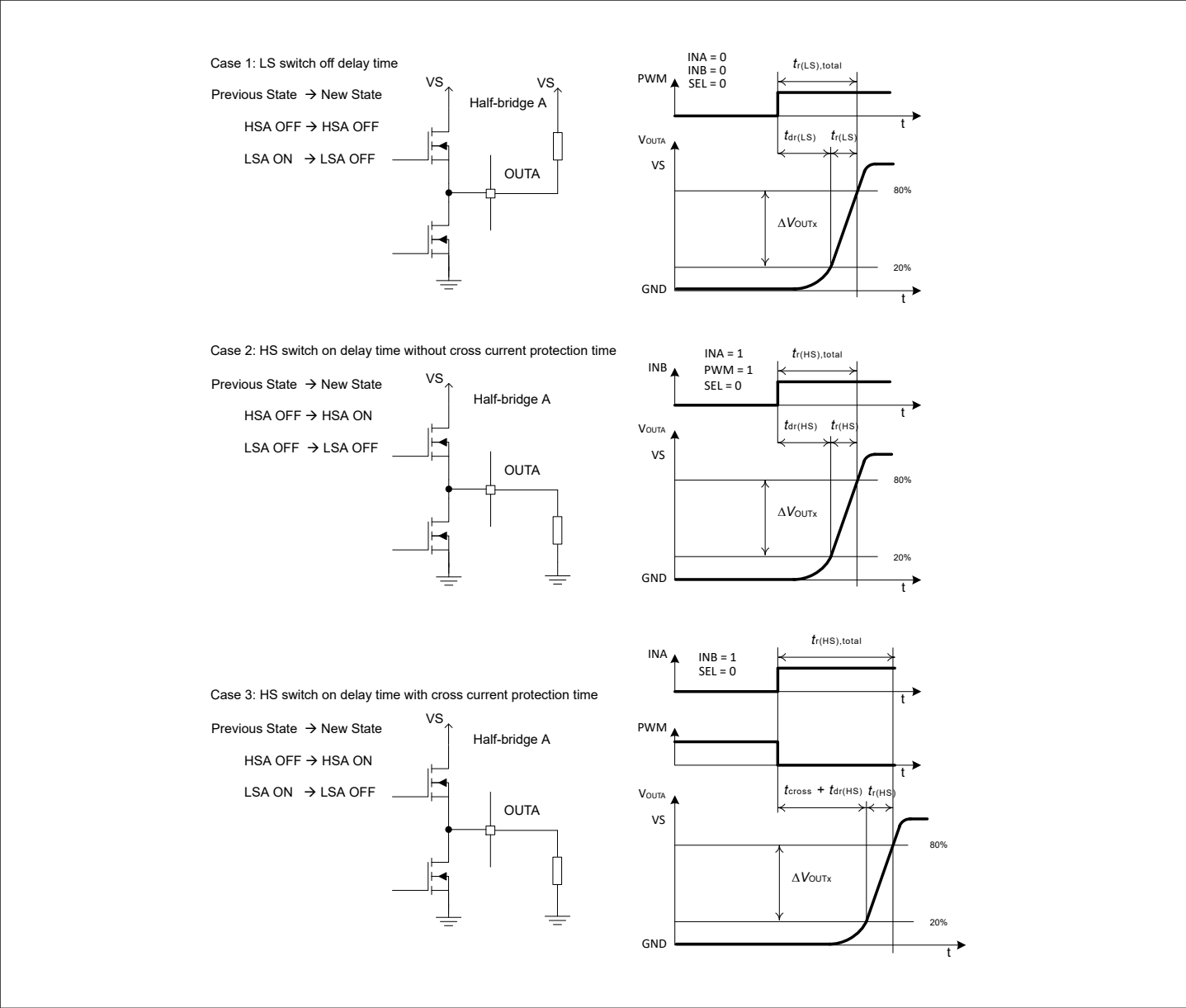


Figure 16 Half-bridge outputs switching times: low-side to high-side transition

7.1.5 Open load detection

In the following conditions this device provides open load detection without any external pull-down resistance, and the error flag will be present at IS pin.

- Open load at OUTA
- Open load at OUTB
- Short to GND at OUTA and / or OUTB

Table 11 Open load diagnostic

Digital input pins				OUTA	OUTB	IS	Comment
INA	INB	PWM	SEL				
1	0	0	0	High	Low	$I_{IS(FAULT)}$	Open load at OUTA or OUTB
0	1	0	1	Low	High	$I_{IS(FAULT)}$	Open load at OUTA or OUTB

(table continues...)

Table 11 (continued) Open load diagnostic

Digital input pins				OUTA	OUTB	IS	Comment
INA	INB	PWM	SEL				
0	0	0	1	Low	Low	$I_{IS(FAULT)}$	Short to GND

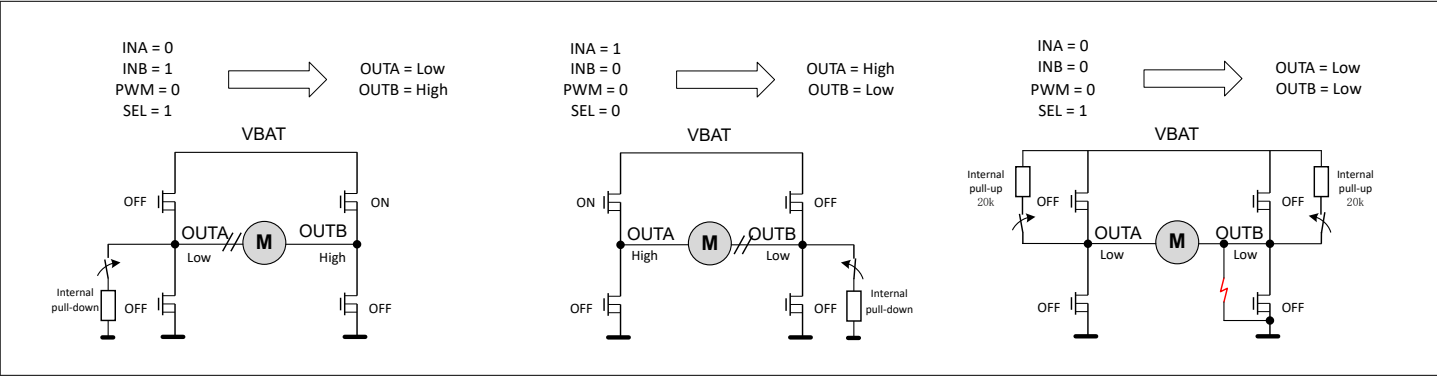


Figure 17 Example of open load detection and short to GND

7.1.6 Current sense

In normal operation (refer to Table 7) a current source is connected to IS pin to provide a current proportional to the forward current flowing through the switch selected by SEL pin as shown in Figure 18:

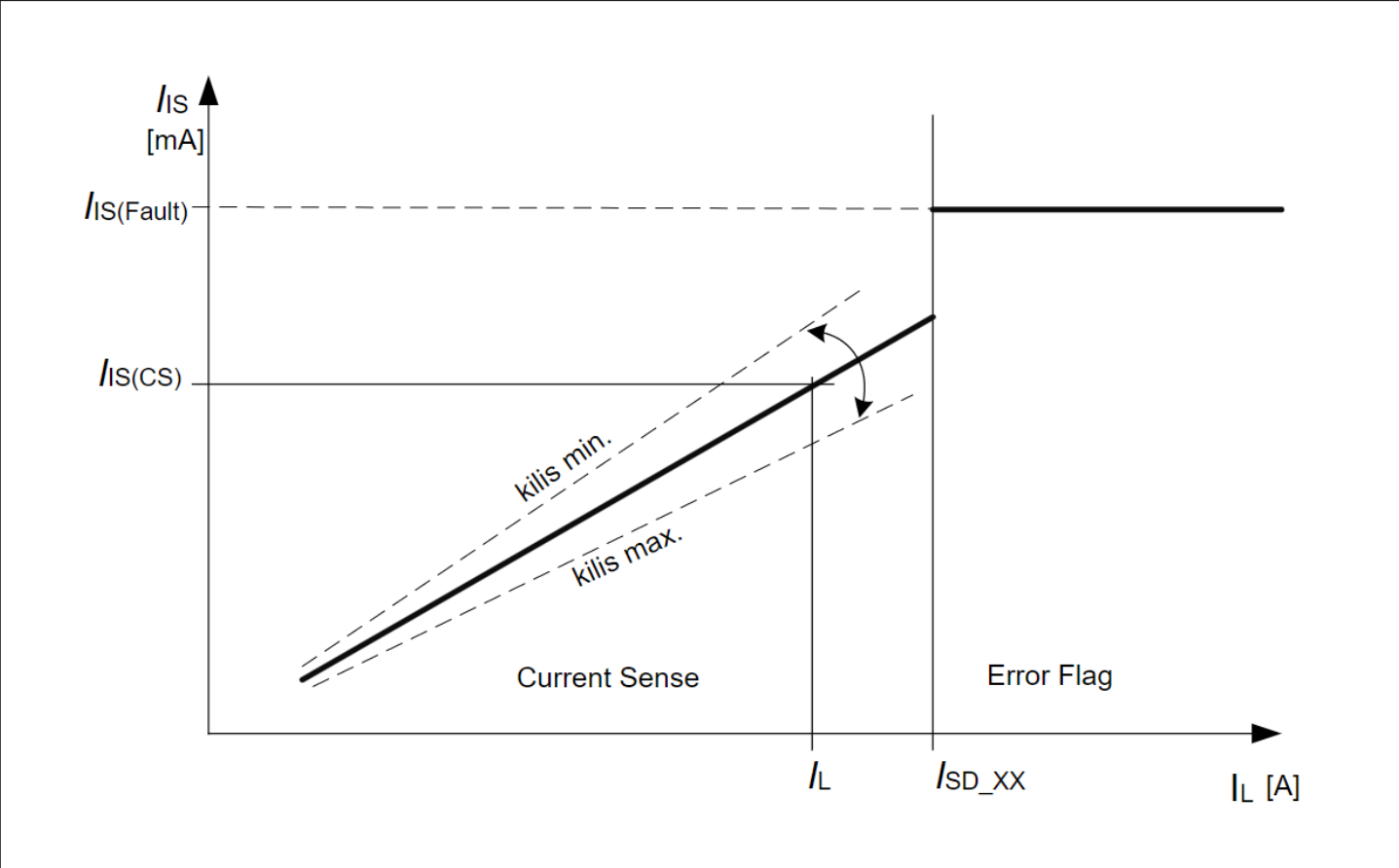


Figure 18 Sense current vs. load current

7.2 SPI variant

Both high-side and low-side switches are capable of detection an open load in their activated state.

7.2.1 Undervoltage shutdown

If the supply voltage drops below $V_{UV(OFF)}$ as shown in Figure 19, the device will

- Switch off the MOSFETs actively
- Keep the charge pump on
- Provide no output at current sense pin
- Set UV bit to 1

If V_S rises above $V_{UV(ON)}$ as shown in Figure 19, the device behaves as follows:

- Resume normal operation
- Clear the UV bit in the [status byte](#)

When the supply voltage rises above $V_{UV(ON)}$, the sense current I_S will be present at the IS pin when the switch on delay and the current sense recovery time t_{IS} expires.

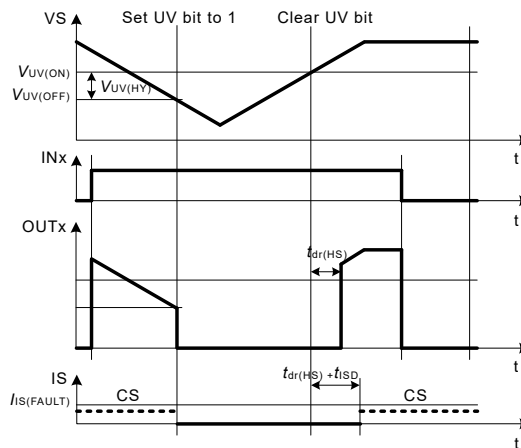


Figure 19 Timing diagram for undervoltage behavior

7.2.2 Overtemperature protection

This device is protected against overtemperature by the integrated temperature sensors. Overtemperature leads to switch off of the output stages including the high-side and low-side switches.

If the temperature sensor reaches T_{jSD} for a duration longer than t_{OTF} , the device behaves as follows

- Switch off both high-side and low-side MOSFETs in dedicated half-bridge
- Keep the charge pump on
- Keep the switches off until the device resumes the normal operation when the junction temperature decreases below the threshold
- Provide $I_{IS(fault)}$ at IS pin
- Set the dedicate overtemperature error flag TSDx bit to 1

When the temperature drops below thermal switch on junction temperature T_{jSO} , the device behaves as follows:

- Resume normal operation
- Clear TSDx bit in the [status byte](#)

7.2.3 Overcurrent protection

7.2.3.1 Short circuit of output to supply or ground

The high-side switches are protected against short to ground whereas the low-side switches are protected against short to supply.

If the current flowing through the switch exceeds the corresponding overcurrent detection threshold I_{SD_xx} , the device will

- Enter into an overcurrent condition
- Start the overcurrent shutdown filter time t_{dOC_xx}
- Limit the current to the current limitation I_{LIM_xx}

When the overcurrent shutdown is triggered, the device will

- Latch off
- Provide $I_{IS(fault)}$ at IS pin
- Switch on the MOSFETs by input pulse (PWM, INA and INB) as shown in [Figure 22](#)
- Set dedicated OCx bit to 1

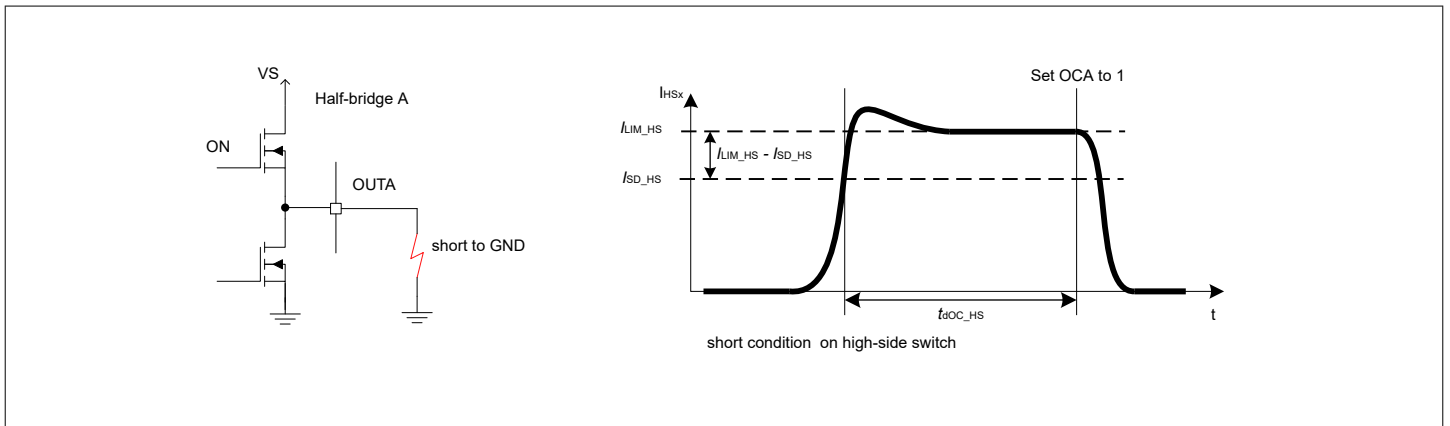


Figure 20 Short circuit between OUTA and GND to trigger overcurrent protection

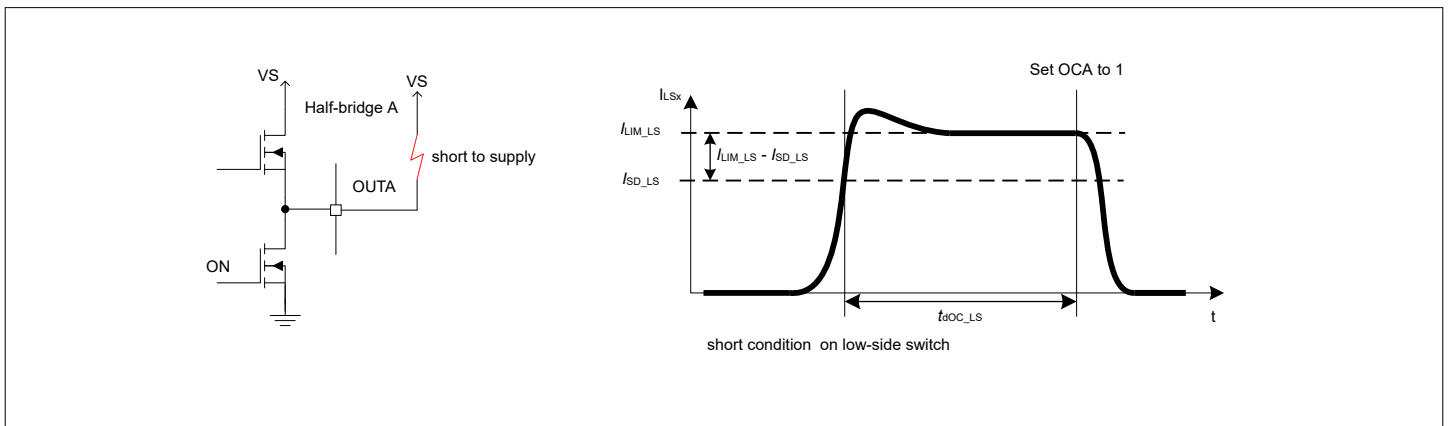


Figure 21 Short circuit between OUTA and VS to trigger overcurrent protection

The high-side current limitation is always higher than the low-side current limitation.

7.2.3.2 Recovery to normal operation

As shown in Figure 22 the recovery will be controlled by the input bits in the control byte. When the input bits to switch on the MOSFET is sent to the device, it behaves as follows:

- Recovery to normal operation
• Switch on the related MOSFET
• Clear the OCx bit

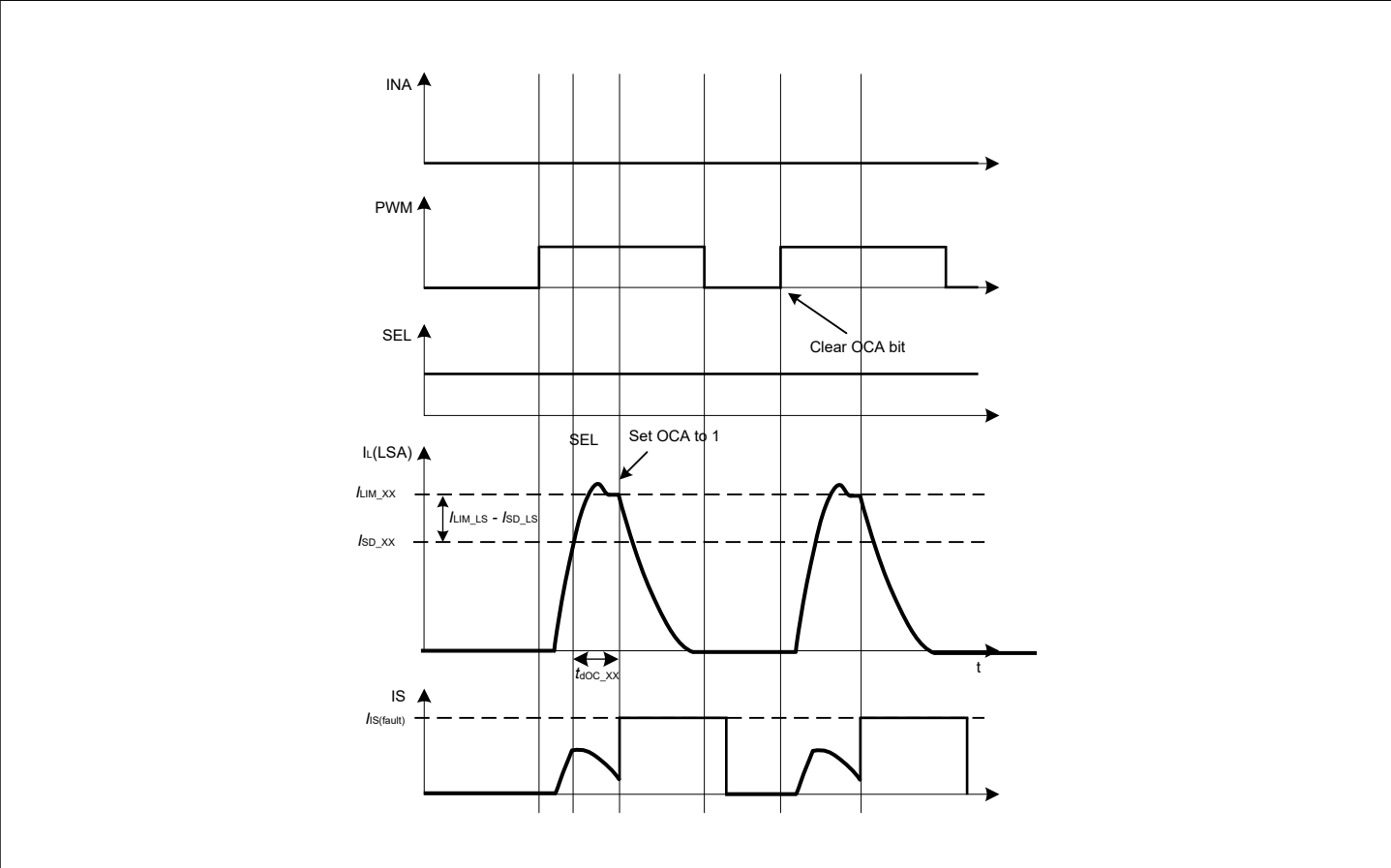


Figure 22 Recovery of short circuit and overcurrent protection by input bits

7.2.4 Open load detection

In the following conditions this device provides open load detection without any external pull-down resistance, and the error flag will be present at IS pin and OL bit in the status byte.

- Open load at OUTA
• Open load at OUTB
• Short to GND

Table 12 Open load diagnostic

Table with 9 columns: Input bits in the control byte (INA, INB, PWM, SEL), OUTA, OUTB, IS, OL bit, and Comment. It lists three conditions for open load detection and short to GND.

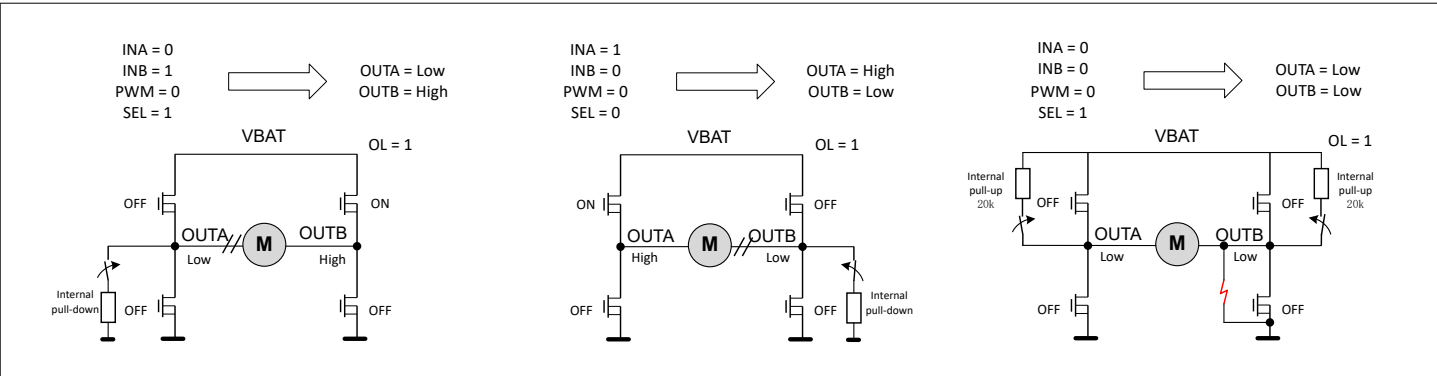


Figure 23 Example of open load detection and short to GND

7.2.5 Current sense

In normal operation (refer to Table 7) a current source is connected to IS pin to provide a current proportional to the forward current flowing through the switch selected by SEL bit as shown in Figure 24:

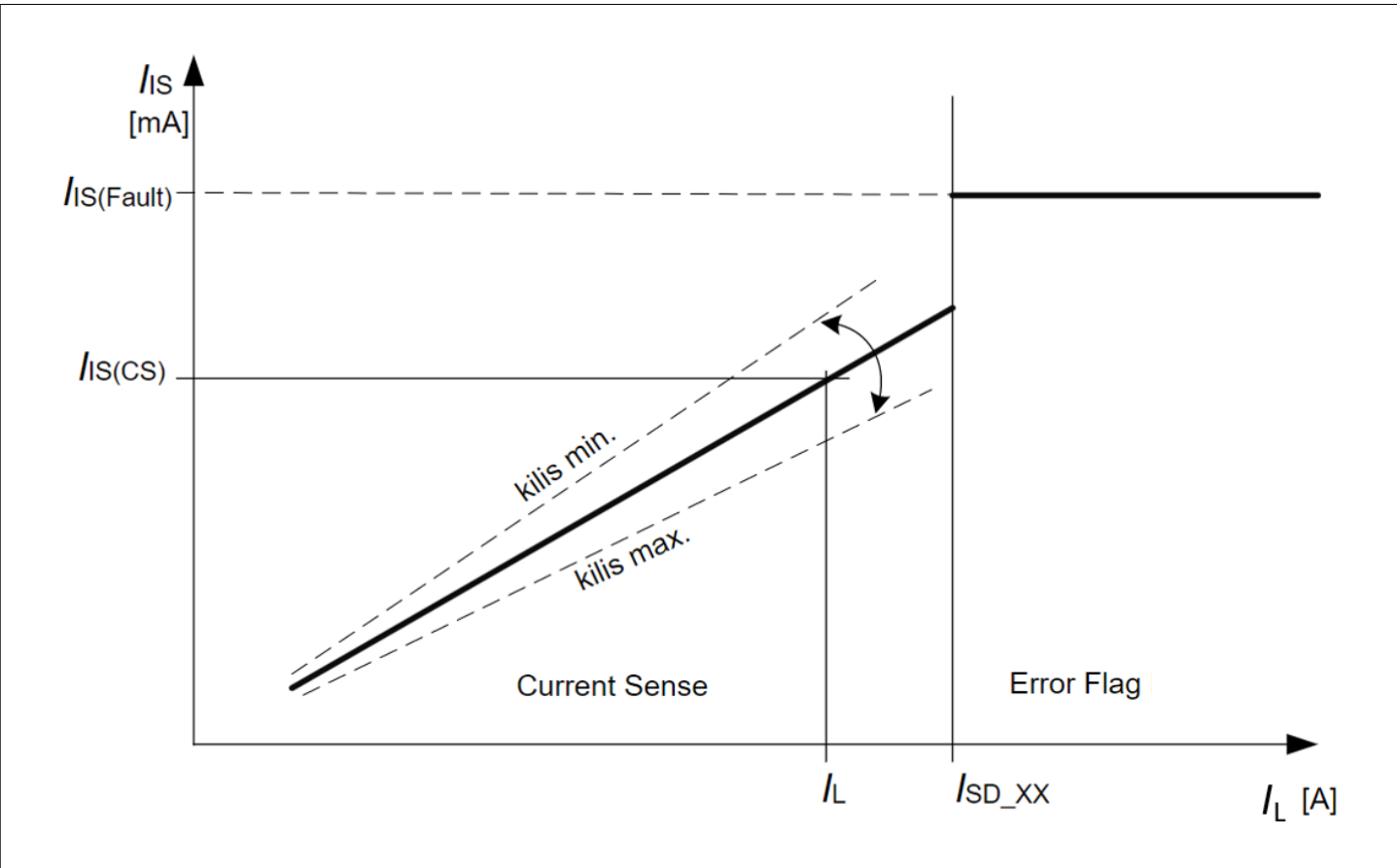


Figure 24 Sense current vs. load current

7.2.6 Cross current protection

The high-side and low-side MOSFETs are ensured never to be simultaneously “ON” to avoid cross currents. This is achieved by integrating delays in the driver stage of the power outputs to create a cross current protection time between switching off one of the MOSFETs and switching on the adjacent MOSFET within the half-bridge. The cross current protection time, t_{cross1} and t_{cross2} , as shown in Figure 25 and Figure 26, have been specified to ensure that the switching slopes do not overlap with each other. This prevents a cross conduction event.

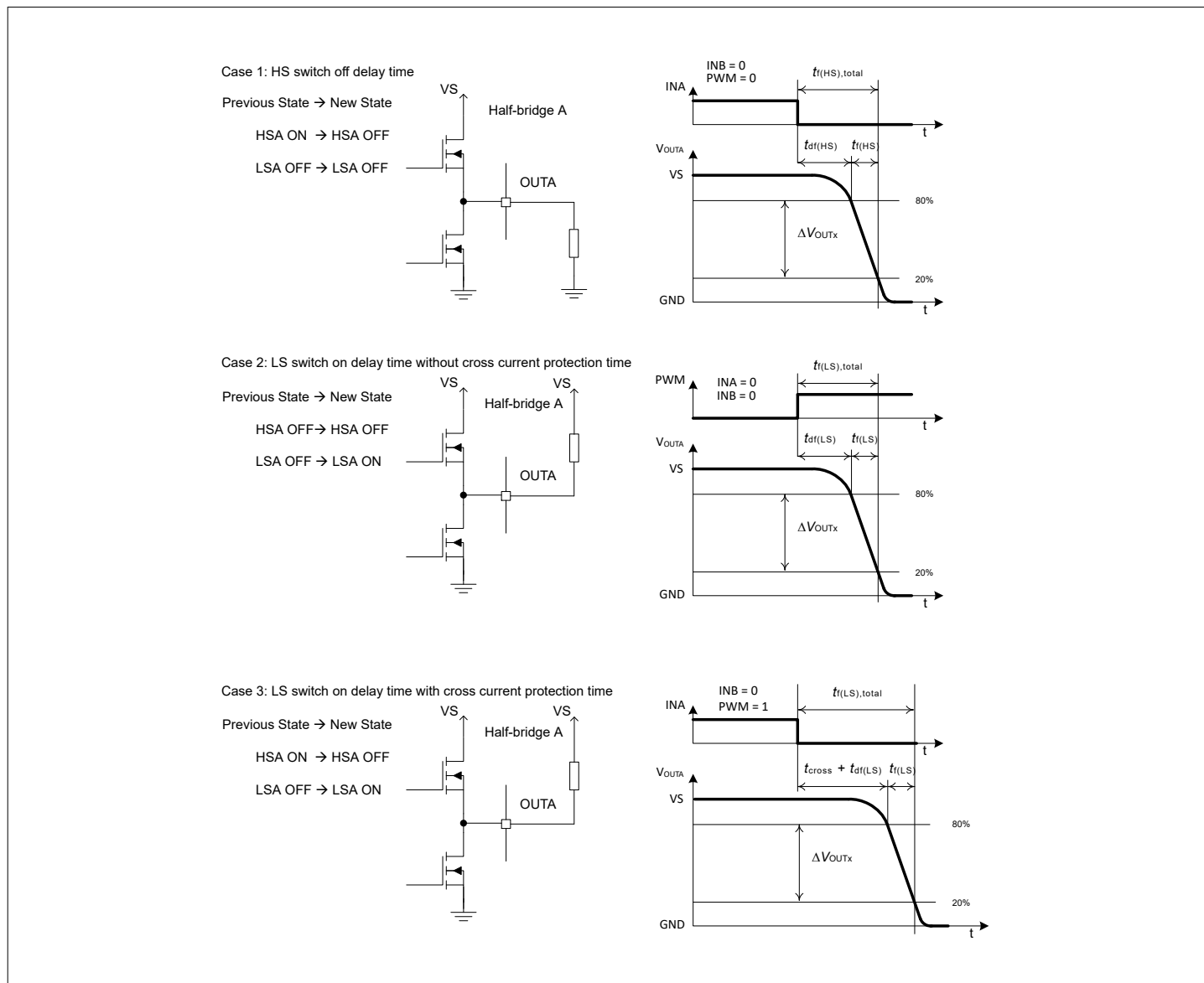


Figure 25 Half-bridge outputs switching times: high-side to low-side transition

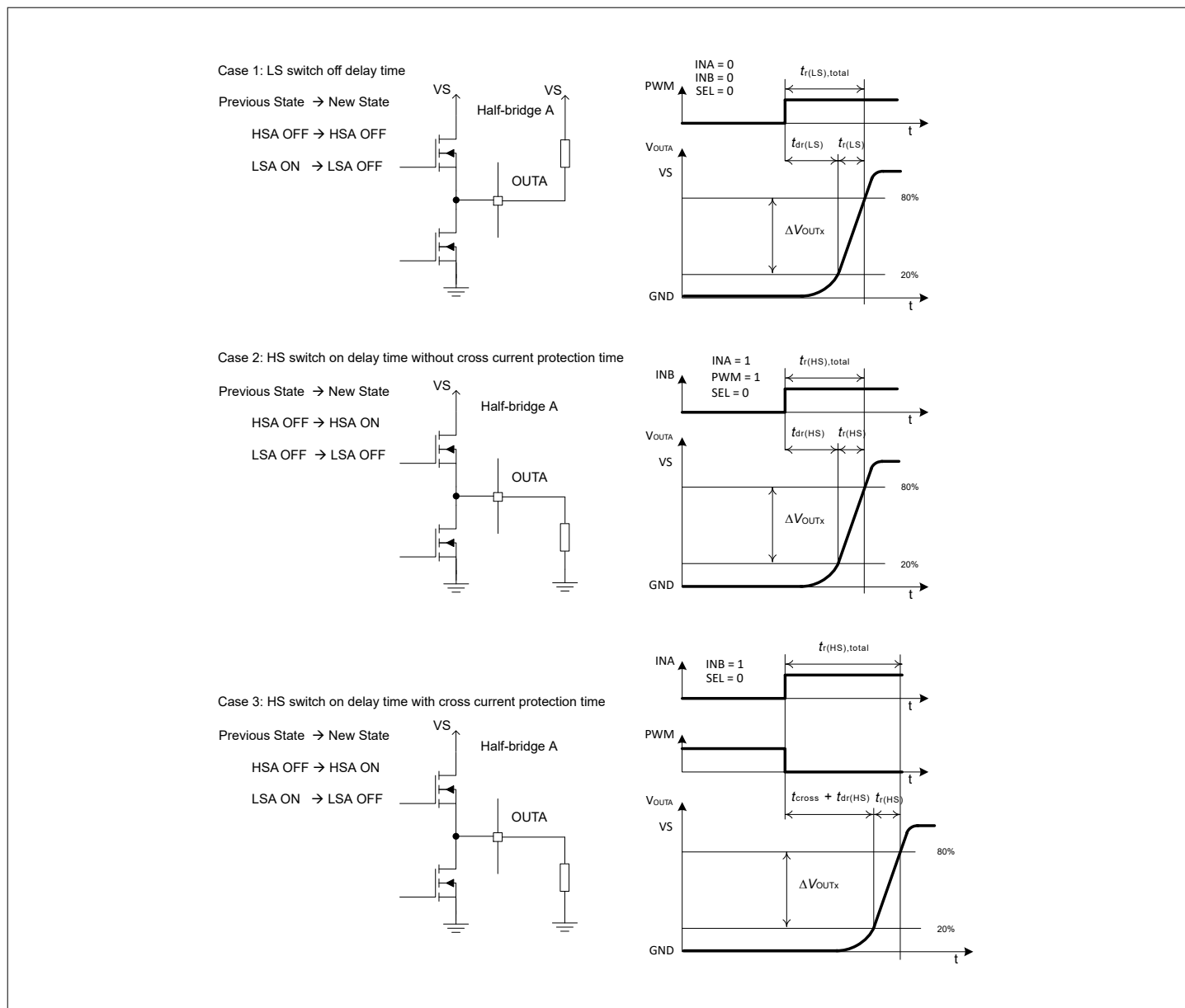


Figure 26 Half-bridge outputs switching times: low-side to high-side transition

7.3 Electrical characteristics

Table 13 Electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch on voltage	$V_{UV(ON)}$	–	–	5.0	V	V_S increasing	P_PRO_01_01
Switch off voltage	$V_{UV(OFF)}$	3.0	–	4.5	V	V_S decreasing	P_PRO_01_02
On/off hysteresis	$V_{UV(HY)}$	–	0.4	–	V	–	P_PRO_01_03

(table continues...)

Table 13 (continued) Electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current sense recovery time	t_{IS}	1	4	10	μs	–	P_PRO_01_04
VS power on reset	V_{S_POR}	3.8	–	–	V	V_S increasing	P_PRO_01_28
VS power off reset	V_{S_POFFR}	–	–	2.0	V	V_S decreasing	P_PRO_01_29
VS power on / off hysteresis	$V_{S_POR_HY}$	–	0.02	–	V	$V_{S_POR} - V_{S_POFFR}$	P_PRO_01_30

Thermal shutdown

Thermal shutdown junction temperature	T_{jSD}	155	175	200	$^\circ\text{C}$	–	P_PRO_01_05
Thermal switch on junction temperature	T_{jSO}	150	–	190	$^\circ\text{C}$	–	P_PRO_01_06
Thermal hysteresis	ΔT	–	12	–	K	–	P_PRO_01_07

Overcurrent shutdown

HS/LS overcurrent detection threshold	I_{OC_HS} I_{OC_LS}	7.5	10	13.5	A	–	P_PRO_01_09
HS/LS current limitation	I_{LIM_HS} I_{LIM_LS}	10.0	14.0	19.5	A	–	P_PRO_01_10
HS/LS overcurrent shutdown filter time	t_{dOC_HS} t_{dOC_LS}	5	7	11	μs	–	P_PRO_01_11

Open load detection

Open load detection current	I_{OLD}	2.5	4	5.5	mA	Input patterns: INA = 1, INB = 0, PWM = 0, SEL = 0; INA = 0, INB = 1, PWM = 0, SEL = 0;	P_PRO_01_12
Open load detection filter time	t_{D_OL}	5	–	–	μs	Input patterns: INA = 1, INB = 0, PWM = 0, SEL = 0; INA = 0, INB = 1, PWM = 0, SEL = 1; INA = 0, INB = 0, PWM = 0, SEL = 1	P_PRO_01_13

(table continues...)

Table 13 (continued) **Electrical characteristics**

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Short to ground detection voltage	V_{STG}	0.7	–	1.25	V	–	P_PRO_01_27
Current sense							
High-side current sense ratio	$Kilis1(HS)$	2010	2250	2490	–	$I_{OUT} = 2.5\text{ A}$	P_PRO_01_14
High-side current sense ratio	$Kilis2(HS)$	1320	2300	3300	–	$I_{OUT} = 0.4\text{ A}$	P_PRO_01_15
Low-side current sense ratio	$Kilis1(LS)$	2010	2250	2490	–	$I_{OUT} = 2.5\text{ A}$	P_PRO_01_16
Low-side current sense ratio	$Kilis2(LS)$	1410	2860	4310	–	$I_{OUT} = 0.4\text{ A}$	P_PRO_01_17
Max. analog sense current	$I_{IS(CS)}$	–	–	5.5	mA	In normal operation condition	P_PRO_01_18
Error sense current	$I_{IS(FAULT)}$	5.9	7.2	8.6	mA	In fault condition	P_PRO_01_19
Timing							
Input reset time for HS latched faults	t_{RST_HS}	300	–	–	ns	$V_{INX} = 5\text{ V to }0\text{ V}$; HSX is in fault condition	P_PRO_01_20
Input reset time for LS latched faults	t_{RST_LS}	300	–	–	ns	$V_{PWM} = 5\text{ V to }0\text{ V}$; LSX is in fault condition	P_PRO_01_21
Standby mode blanking time	$t_{standby}$	–	–	50	μs	–	P_PRO_01_22
Current sense blank time for slow slew rate	t_{IS_BLK}	1.5	–	10	μs	I_{IS} from 0 to 40%; $R_{load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PRO_01_23
Current sense blank time for fast slew rate	t_{IS_BLK}	1.0	–	8.5	μs	I_{IS} from 0 to 40%; $R_{load} = 5.6\ \Omega$; $V_S = 13.5\text{ V}$	P_PRO_01_24
Recovery time from latched fault	t_{rec}	7	–	25	μs	–	P_PRO_01_25

8 Serial peripheral interface - SPI

8.1 SPI description

The control input word is read via the serial data input pin SDI, which is synchronized with the clock input SCLK provided by microcontroller. The output word appears synchronously at the serial data output pin SDO, see [Figure 27](#). The transmission cycle begins when the chip is selected by the input CS (chip select), active high. After the CS input returns from high to low, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (high impedance) at this point, thereby releasing the SDO bus. The state of SDI is shifted into the input flip-flop with every falling edge on SCLK. The state of SDO is shifted out after every rising edge on SCLK. The SPI of the device is daisy chain capable.

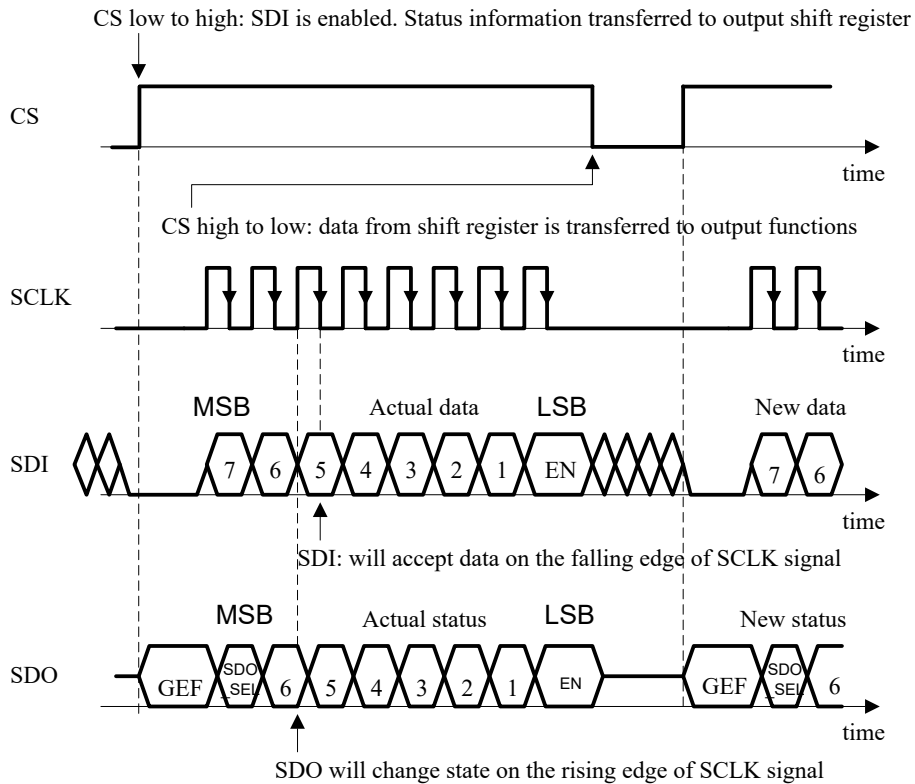


Figure 27 SPI data transfer timing

A SPI communication consists of 8-bit frames as shown in [Figure 28](#):

- SDI receives the data byte
- If SDO_SEL = 0, SDO transmits the global error flag and the Control byte
- If SDO_SEL = 1, SDO transmits the global error flag and the Status byte

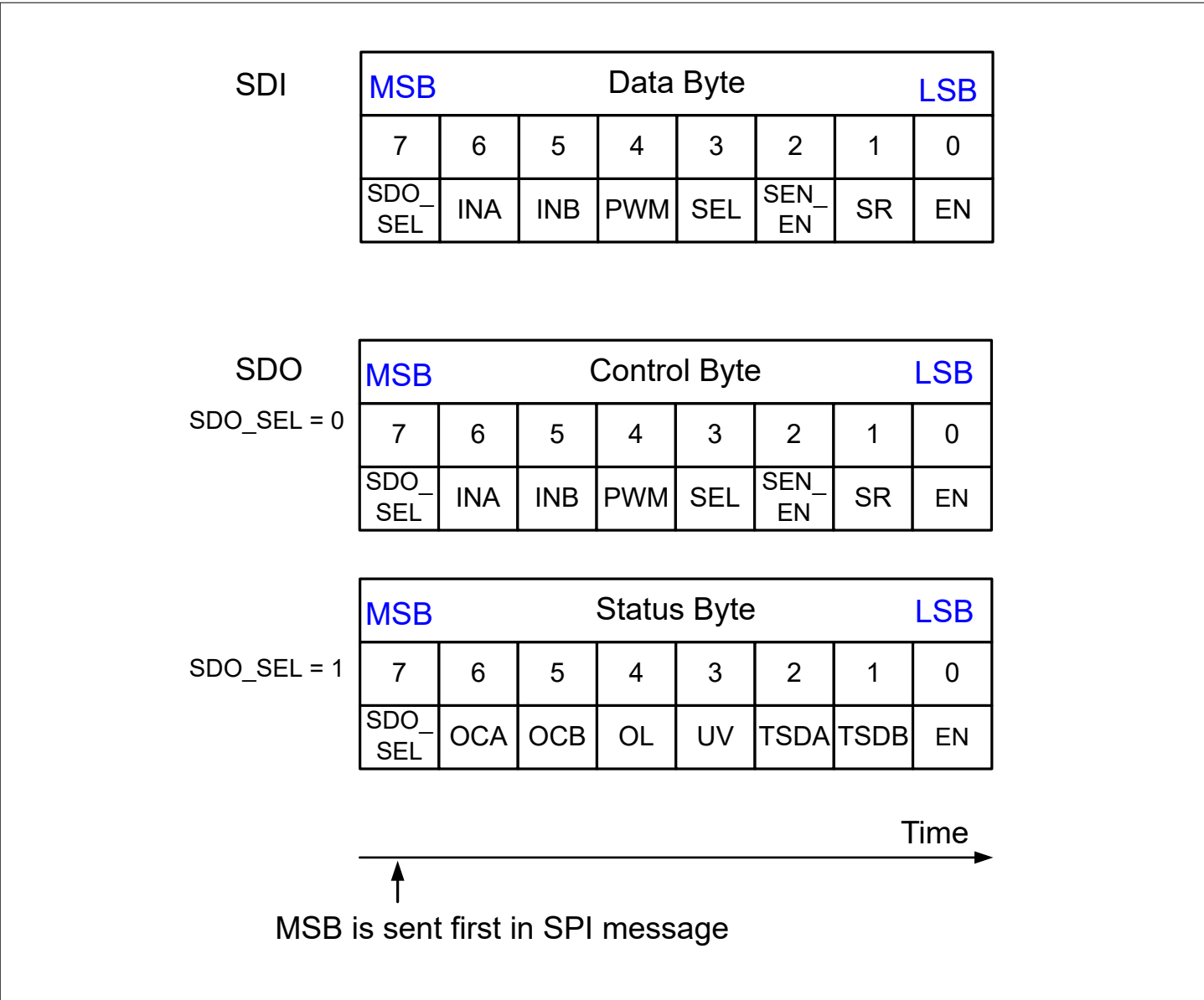


Figure 28 SPI response

8.2 Global error flag

The global error flag (GEF) bit is reported on SDO between the CS rising edge and the first SCLK rising edge. With global error flag the device is possible to have a quick diagnostic without any SPI clock pulse in following conditions:

- Overcurrent of half-bridge A
- Overcurrent of half-bridge B
- Open load
- Undervoltage
- Thermal shut down

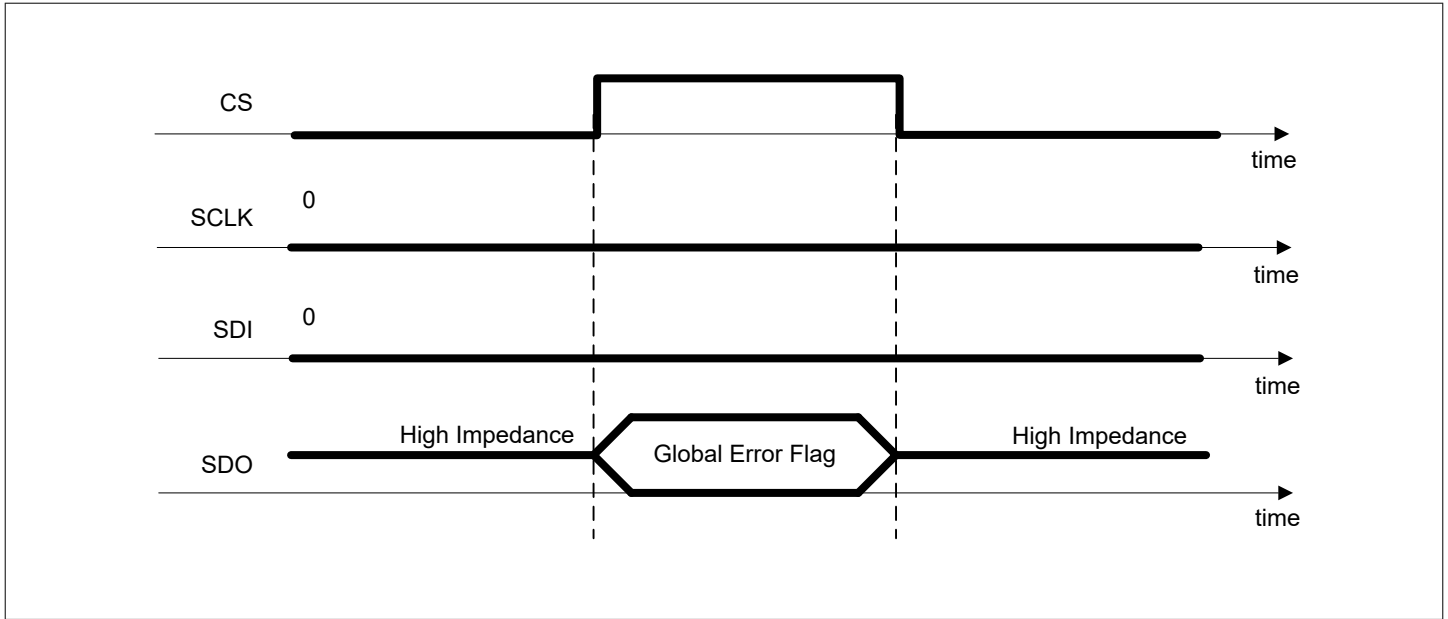


Figure 29 Global error flag - Diagnostic with 0 - clock cycle

8.3 Control byte

The control byte is sent to the device via SDI pin:

- Enable (EN bit):
 - EN is set to 1 to enable the device
 - EN is set to 0 to disable the device (default)
- Slew rate selection (SR bit):
 - SR is set to 1 to select the fast slew rate level
 - SR is set to 0 to select the slow slew rate level (default)
- Current sense enable (SEN_EN bit):
 - SEN_EN is set to 1 to enable the current sense
 - SEN_EN is set to 0 to disable the current sense (default)
- Current sense select (SEL bit):
 - SEL is set to 1 to provide the sensing current of half-bridge A at IS pin
 - SEL is set to 0 to provide the sensing current of half-bridge B at IS pin (default)
 - Combine with other input bits the error flags of open load and short to GND are provided to the IS pin (refer to [Table 7](#))
- PWM (PWM bit): Combine with INA, INB and SEL bit to select the operative mode (refer to [Table 7](#))
- INB (OCB bit): Combine with INA, SEL and PWM bit to select the operative mode (refer to [Table 7](#))
- INA (OCA bit): Combine with INB, SEL and PWM bit to select the operative mode (refer to [Table 7](#))
- Read out byte select (SDO_SEL bit):
 - SDO_SEL is set to 1 to read out the status byte at SDO pin
 - SDO_SEL is set to 0 to read out the control byte at SDO pin (default)

8.4 Status byte

The SDO shifts out the status register during the SCLK cycles to provide an overview of the device status shown in [Table 14](#) as following:

- Current operation mode of the device (EN bit): standby mode or normal operation mode
- Thermal shut down (TSDB bit): overtemperature shutdown of half-bridge B

- Thermal shut down (TSDA bit): overtemperature shutdown of half-bridge A
- Undervoltage of VS (UV bit): VS undervoltage shutdown
- Open load (OL bit): open load detection
- Overcurrent of half-bridge B (OCB bit): overcurrent protection of half-bridge B
- Overcurrent of half-bridge A (OCA bit): overcurrent protection of half-bridge A
- Read out byte (SDO_SEL bit): control byte or status byte

Note: The **global error flag** is a logic OR combination of error flags in the status byte: $GEF = (TSDB) \text{ OR } (TSDA) \text{ OR } (UV) \text{ OR } (OL) \text{ OR } (OCB) \text{ OR } (OCA)$.

Table 14 Failure reported in the global status byte and global error flag

Type of error	Failure reported in the global status byte	Global error flag
Thermal shut down of half-bridge A	TSDA = 1	1
Thermal shut down of half-bridge B	TSDB = 1	1
Undervoltage of VS	UV = 1	1
Open load	OL = 1	1
Overcurrent of half-bridge A	OCA = 1	1
Overcurrent of half-bridge B	OCB = 1	1
No error	TSD = 0 UV = 0 OL = 0 OCA = 0 OCB = 0	0

8.5 SPI timing

To ensure a correct SPI communication, the following conditions have to be fulfilled:

- SCLK must be low for a minimum t_{BEF} before CS rising edge and t_{lead} or t_{lead_EN} after CS rising edge
- SCLK must be low for a minimum t_{lag} before CS falling edge and t_{BEH} after CS falling edge

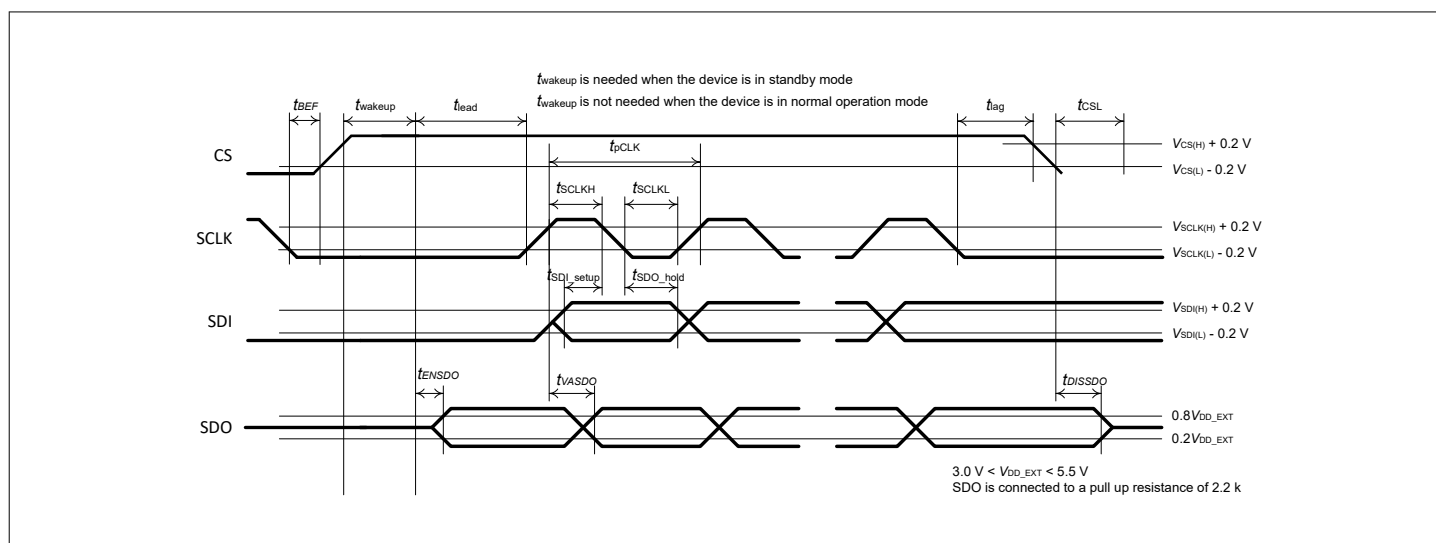


Figure 30 SPI timing parameters

8.6 Daisy chain

In daisy chain configuration the SDO pin of the microcontroller is connected to a slave SDI. The first slave SDO is connected to the next slave SDI in the chain. The SDO of the final device in the chain is connected to the SDI pin of the microcontroller. In daisy chain configuration, the microcontroller SCLK is connected to all the slave CS inputs as shown in [Figure 31](#).

In the daisy chain an external VDDIO supply and a pull-up resistance is needed to drive the push-pull stage of the SDO pins. For the last device in the daisy chain no external resistance is required if the microcontroller has an internal pull-up resistance connected to it's SDI pin.

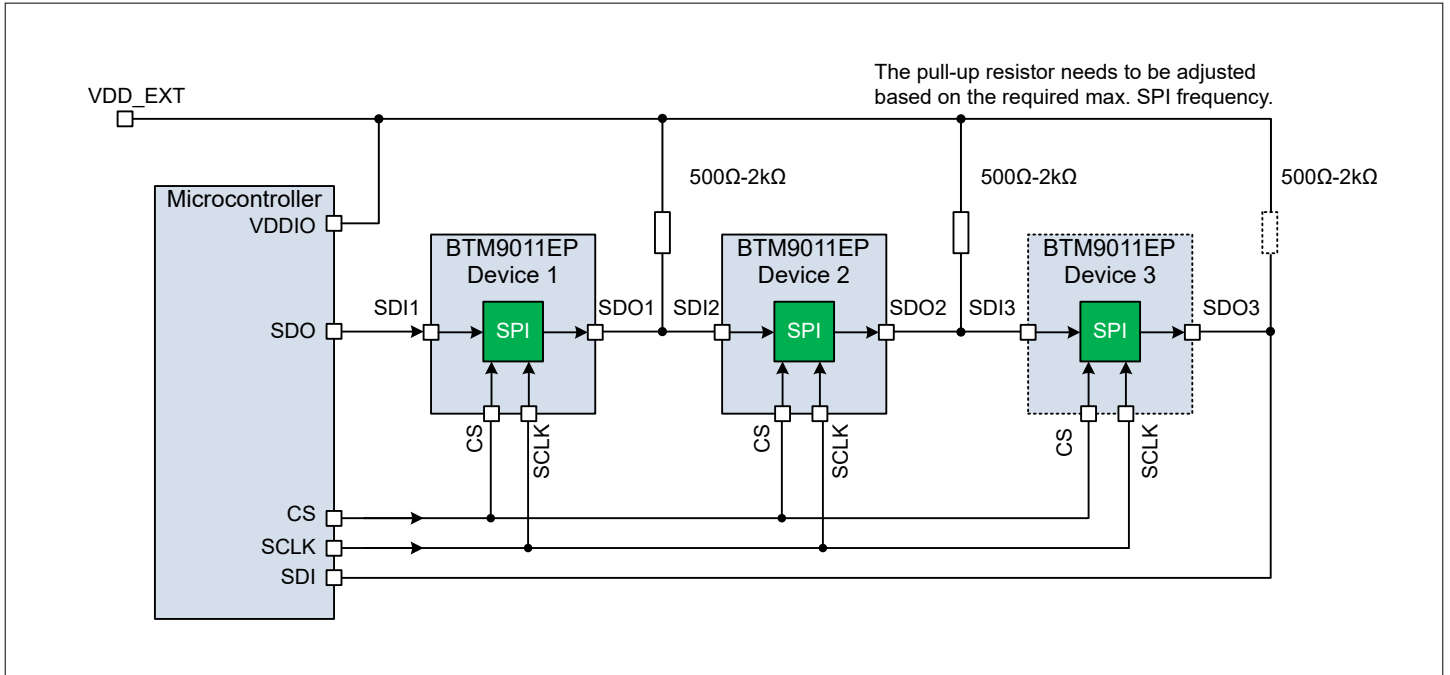


Figure 31 Daisy chain configuration with three BTM9011EP devices

The BTM9011EP operates as a 8-bit shift register. The microcontroller must send the data bytes in reverse order as shown in [Figure 32](#):

- The data byte for the device 3 is sent first.
- Then data byte for the device 2 is sent.
- Then data byte for the device 1 is sent.

The SDI of the microcontroller, which is connected to SDO of the last device in the daisy chain, receives:

- A logic OR combination of all Global Error Flags (GEF) at the beginning of the SPI frame, between CS rising edge and the first SCLK rising edge.
- The status byte or the control byte of each BTM9011EP in reverse order: The status byte 3 or the control byte 3 corresponding to the device 3 is received first, followed by the status byte 2 or the control byte 2 corresponding to the device 2, and finally the status byte 1 or the control byte 1 corresponding to the device 1 is received.

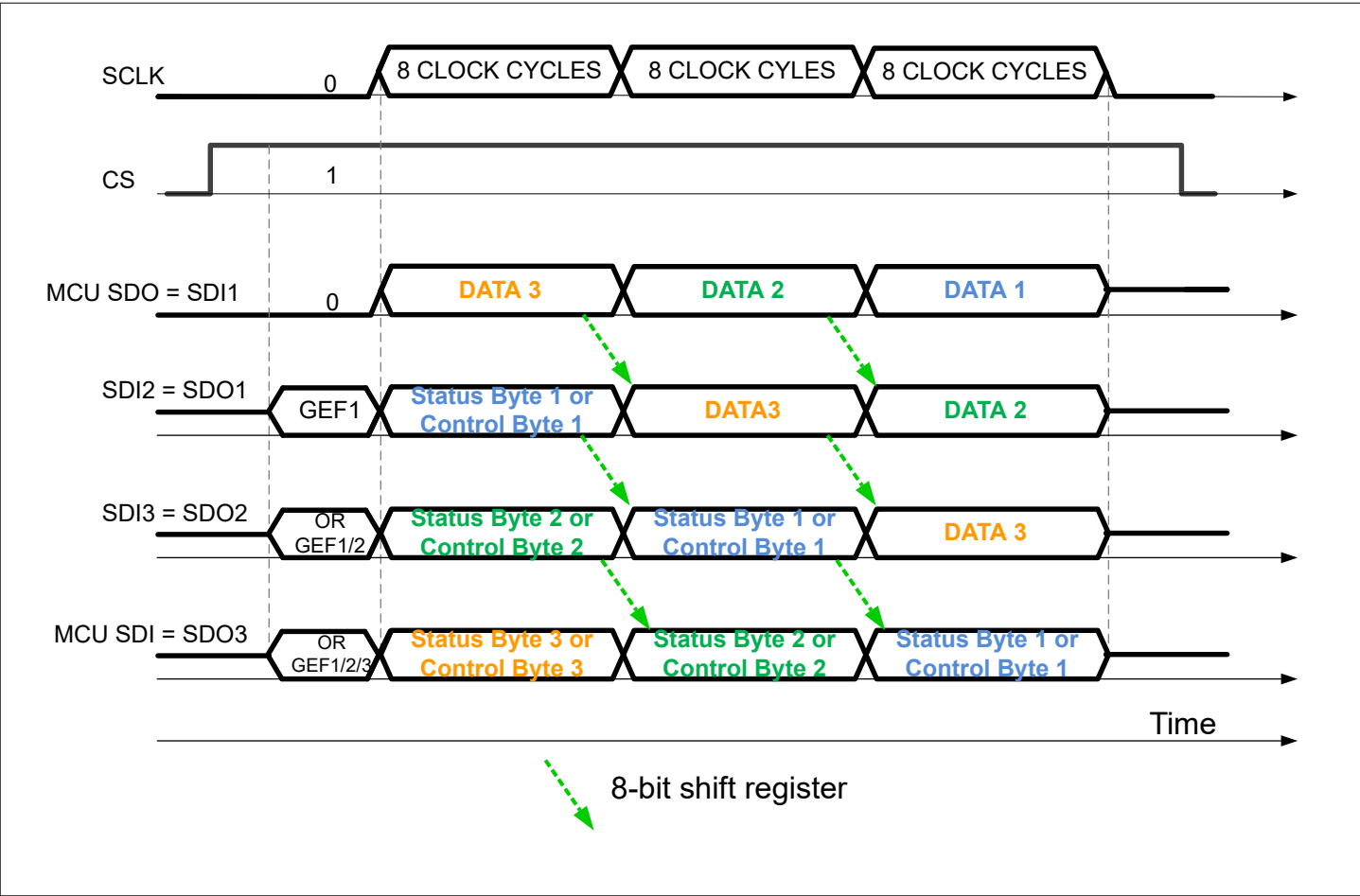


Figure 32 SPI frame in daisy chain configuration with three BTM9011EP devices

8.7 Electrical characteristics SPI

Table 15 SPI electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{\text{SPI,max}}$	–	–	4	MHz	–	P_SPI_01_01
Delay from CS rising edge to first rising edge of SCLK							
SPI interface wake-up time	t_{WAKEUP}	–	–	20	μs	–	P_SPI_01_02
SPI interface (SDI, SCLK, CS)							
Pull down resistor at pin CS, SDI and SCLK	$R_{\text{CS}}, R_{\text{PD_SDI}}, R_{\text{PD_SCLK}},$	100	250	300	$\text{k}\Omega$	–	P_SPI_01_07

(table continues...)

Table 15 (continued) SPI electrical characteristics

$V_S = 7\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input capacitance at pin CS, SDI and SCLK	C_I	–	–	15	pF	–	P_SPI_01_08

Input interface, logic outputs MISO

High output voltage level	$V_{SDO(H)}$	$V_{DD_EXT} - 0.4$	–	–	V	$R_{PULL_UP} = 2.2\text{ k}\Omega$; $V_{DD_EXT} = 5\text{ V}$	P_SPI_01_09
Low output voltage level	$V_{SDO(L)}$	–	–	0.6	V	$R_{PULL_UP} = 2.2\text{ k}\Omega$; $V_{DD_EXT} = 5\text{ V}$	P_SPI_01_10
Tri-state leakage current	I_{SDOLK}	-10	–	10	μA	$V_{CS} = V_{DD_EXT}$; $0\text{ V} < V_{SDO} < V_{DD_EXT}$; $R_{PULL_DOWN} = 200\text{ k}\Omega$	P_SPI_01_11
Tri-state input capacitance	C_{SDO}	–	–	15	pF	–	P_SPI_01_12

Data input timing

SCLK period	t_{pCLK}	250	–	–	ns	–	P_SPI_01_13
SCLK high time	t_{SCLKH}	$0.45 \cdot t_{pCLK}$	–	$0.55 \cdot t_{pCLK}$	ns	–	P_SPI_01_14
SCLK low time	t_{SCLKL}	$0.45 \cdot t_{pCLK}$	–	$0.55 \cdot t_{pCLK}$	ns	–	P_SPI_01_15
SCLK low before CS high	t_{BEF}	125	–	–	ns	–	P_SPI_01_16
CS setup time	t_{lead}	250	–	–	ns	–	P_SPI_01_17
SCLK setup time	t_{lag}	250	–	–	ns	–	P_SPI_01_18
SCLK low after CS low	t_{BEH}	125	–	–	ns	–	P_SPI_01_19
SDI setup time	t_{SDI_setup}	100	–	–	ns	–	P_SPI_01_20
SDI hold time	t_{SDI_hold}	50	–	–	ns	–	P_SPI_01_21
Input signal rise time at pin SDI, SCLK, CS	t_{rIN}	–	–	50	ns	–	P_SPI_01_22
Input signal fall time at pin SDI, SCLK, CS	t_{fIN}	–	–	50	ns	–	P_SPI_01_23
Minimum CS low time	t_{CSL}	4	–	–	μs	–	P_SPI_01_24

(table continues...)

Table 15 (continued) SPI electrical characteristics

$V_S = 7\text{ V}$ to 18 V , $T_j = -40^\circ\text{C}$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GEF valid time	$t_{\text{GEF_VAL}}$	–	–	$250 \cdot n$	ns	n = no. of devices in the same daisy chain;	P_SPI_01_30

Data output timing

SDO rise time	t_{rSDO}	–	50	250	ns	$C_{\text{Load}} = 50\text{ pF}$; $R_{\text{pullup}} = 2.2\text{ k}\Omega$; Max. values depends on R_{pullup}	P_SPI_01_25
SDO fall time	t_{fSDO}	–	50	110	ns	$C_{\text{Load}} = 50\text{ pF}$; $R_{\text{pullup}} = 2.2\text{ k}\Omega$	P_SPI_01_26
SDO enable time after CS rising edge	t_{ENSDO}	–	–	80	ns	–	P_SPI_01_27
SDO disable time after CS	t_{DISSDO}	–	–	200	ns	–	P_SPI_01_28
SDO valid time for $V_{\text{DD_EXT}} = 5\text{ V}$	t_{VASDO}	–	–	110	ns	$V_{\text{SDO}} < 0.2 \cdot V_{\text{DD_EXT}}$, $V_{\text{SDO}} > 0.8 \cdot V_{\text{DD_EXT}}$ $C_{\text{load}} = 50\text{ pF}$	P_SPI_01_29

9 Application Information

The following simplified [application figure](#) is given as a hint for the implementation of the device only and is not regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the applications.

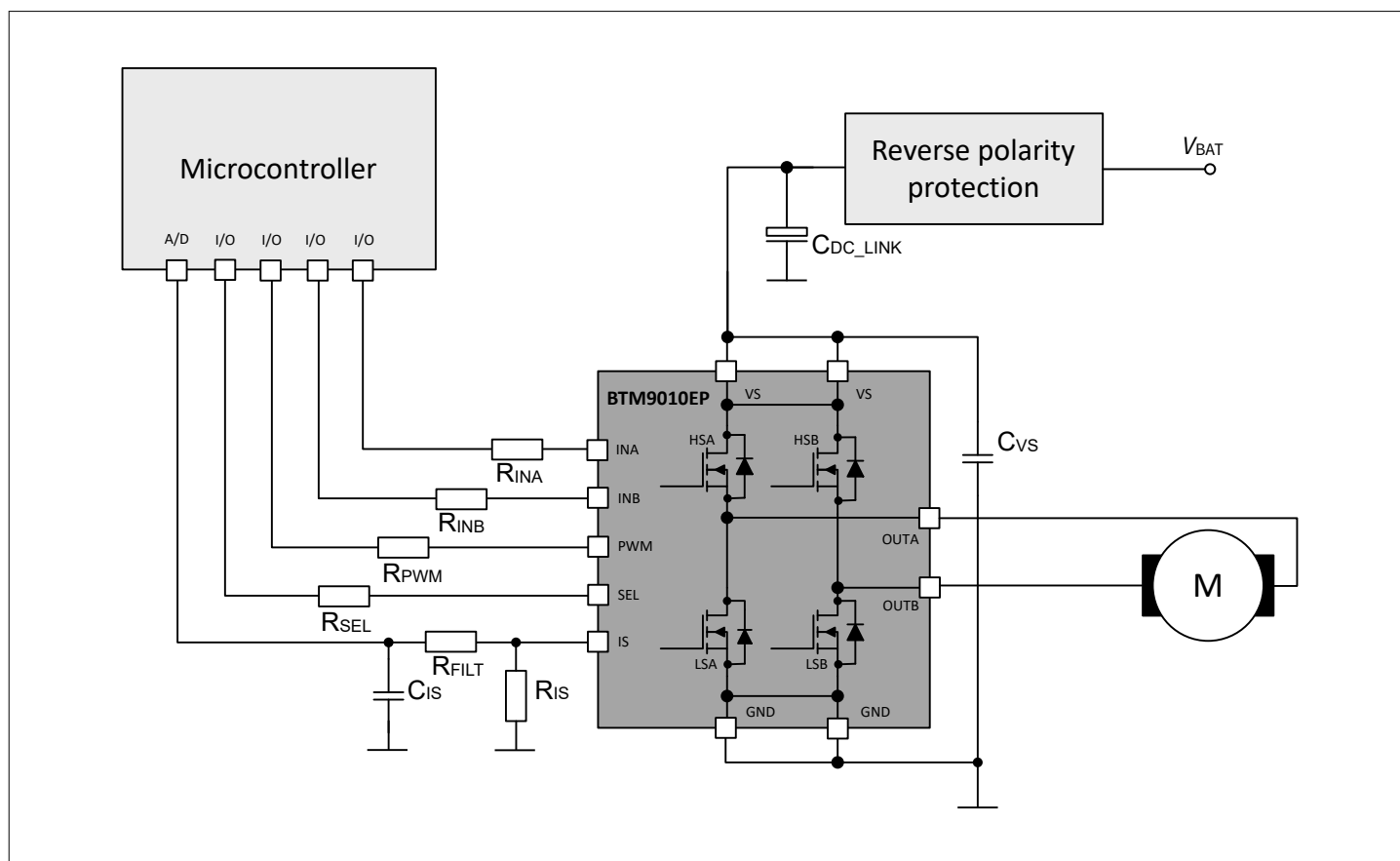


Figure 33 Application figure of BTM9010EP

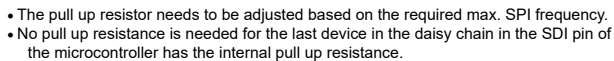


Figure 34 **Application figure of BTM9011EP in daisy chain**

10 Package

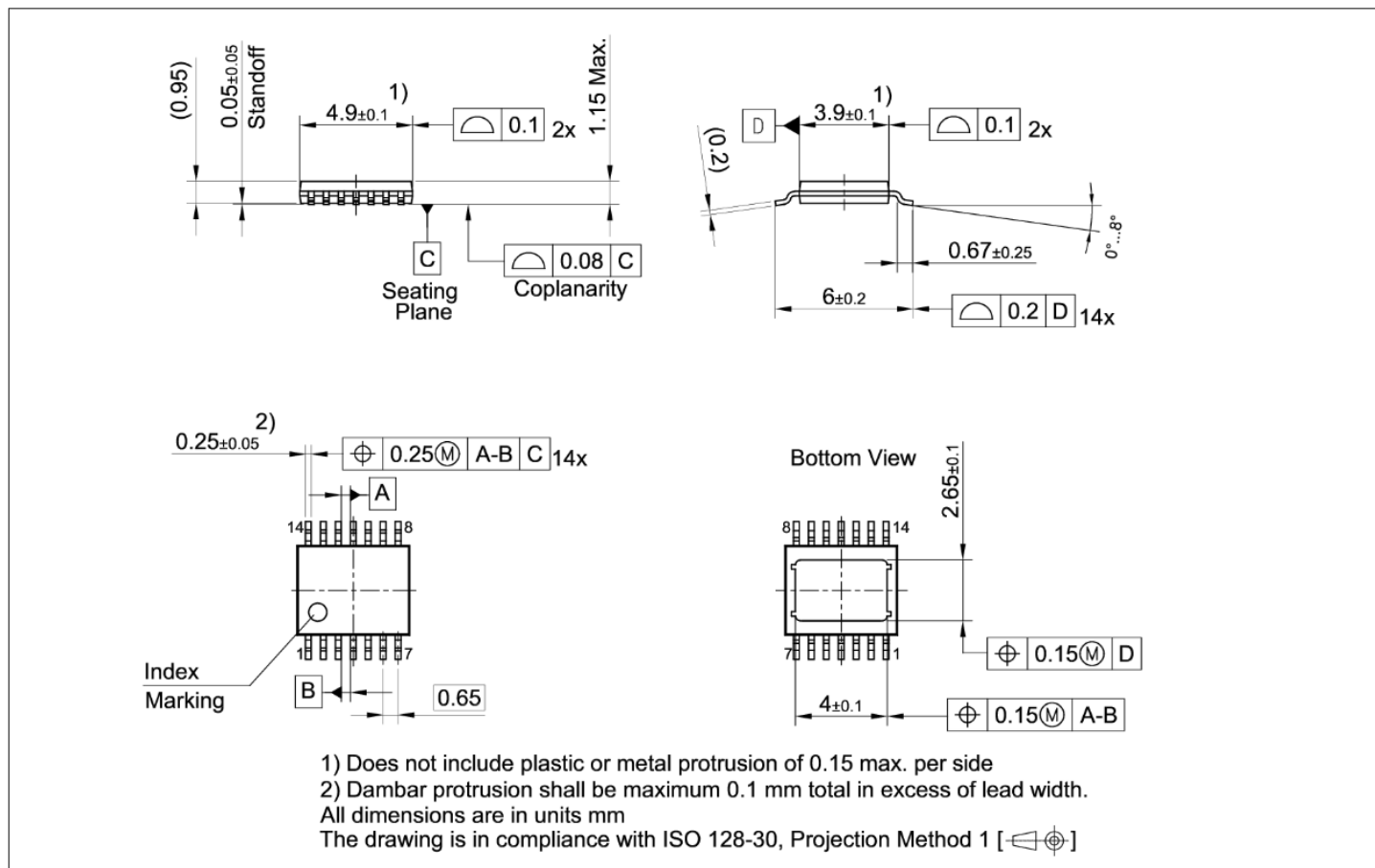


Figure 35 Package dimension



11 Datasheet revision history

Table 16 Revision history

Revision number	Date of release	Description of changes
1.00	2024-06-30	Datasheet

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