General Purpose NPN Epitaxial Planar Transistor

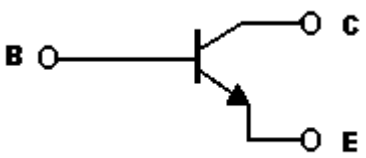
BTN5551K3

Features

- High breakdown voltage, $BV_{CEO} \geq 160V$
- Pb-free lead plating package

Symbol

BTN5551K3



B：Base
C：Collector
E：Emitter

Outline

TO-92L

E C B

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	180	V
Collector-Emitter Voltage	V_{CEO}	160	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current (DC)	I_C	600	mA
Collector Current (pulse)	I_{CP}	2 (Note)	A
Base Current	I_B	200	mA
Power Dissipation	P_D	900	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	139	°C/W
Operating Junction and Storage Temperature Range	Tj ; Tstg	-55~+150	°C

Note : Pulse test, pulse width≤300μs, duty cycle≤2%

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	180	-	-	V	I_C=100μA
BV_{CEO}	160	-	-	V	I_C=1mA
BV_{EBO}	6	-	-	V	I_E=10μA
I_{CBO}	-	-	50	nA	V_{CB}=120V
I_{EBO}	-	-	50	nA	V_{EB}=6V
*$V_{CE(sat)}1$	-	0.1	0.15	V	I_C=10mA, I_B=1mA
*$V_{CE(sat)}2$	-	-	0.2	V	I_C=50mA, I_B=5mA
*$V_{BE(sat)}1$	-	-	1	V	I_C=10mA, I_B=1mA
*$V_{BE(sat)}2$	-	-	1	V	I_C=50mA, I_B=5mA
*$h_{FE}1$	100	-	-	-	V_{CE}=5V, I_C=1mA
*$h_{FE}2$	100	-	-	-	V_{CE}=5V, I_C=10mA
*$h_{FE}3$	50	-	-	-	V_{CE}=5V, I_C=50mA
*$h_{FE}4$	120	-	270	-	V_{CE}=6V, I_C=2mA
f_T	100	-	-	MHz	V_{CE}=20V, I_C=10mA, f=100MHz
Cob	-	-	6	pF	V_{CB}=20V, I_E=0A,f=1MHz

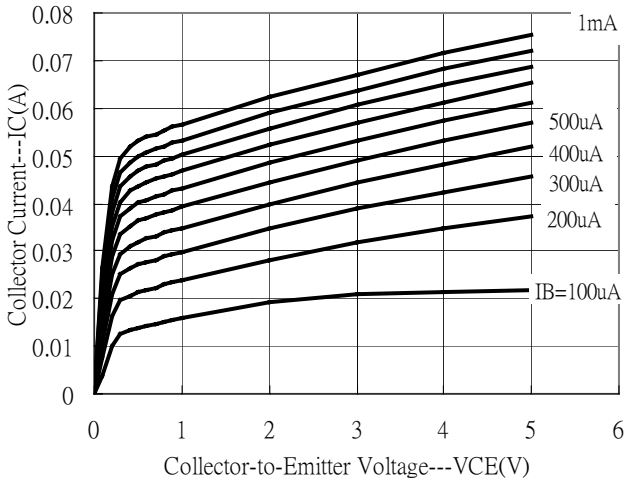
*Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

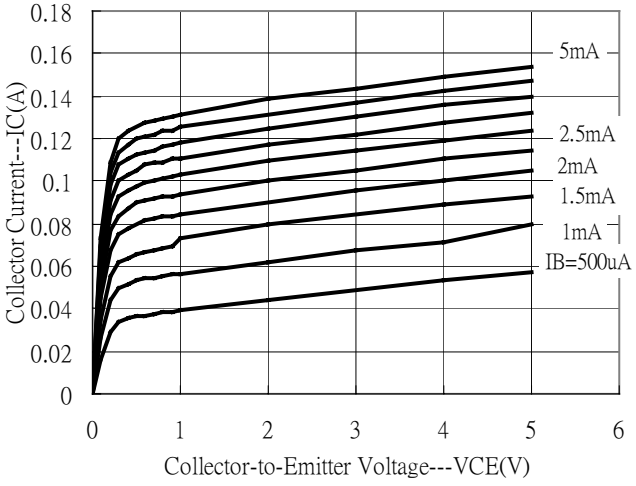
Device	Package	Shipping
BTN5551K3-0-BK-G	TO-92L (Pb-free lead plating and halogen-free package)	500 pcs / bag, 10 bags/box, 10 boxes/carton
BTN5551K3-0-TB-G	TO-92L (Pb-free lead plating and halogen-free package)	2000 pcs / Tape & Box

Typical Characteristics

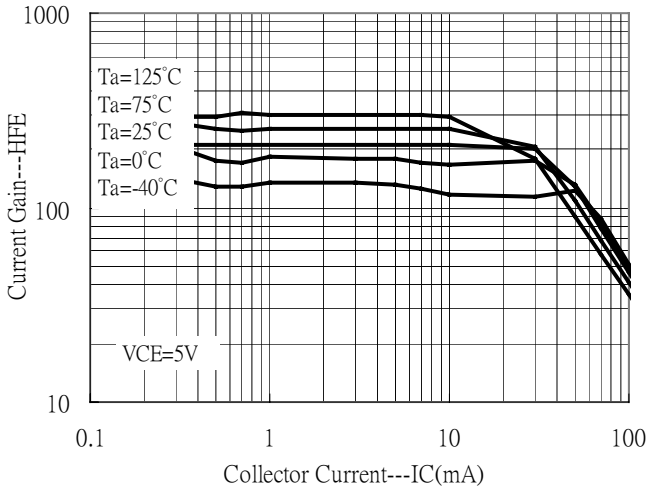
Emitter Grounded Output Characteristics



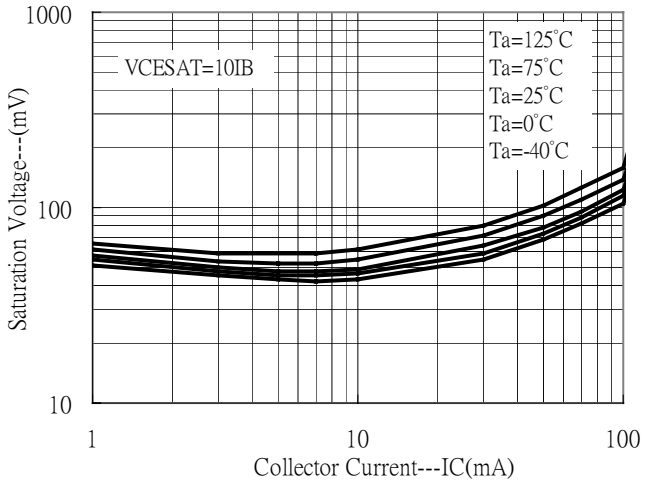
Emitter Grounded Output Characteristics



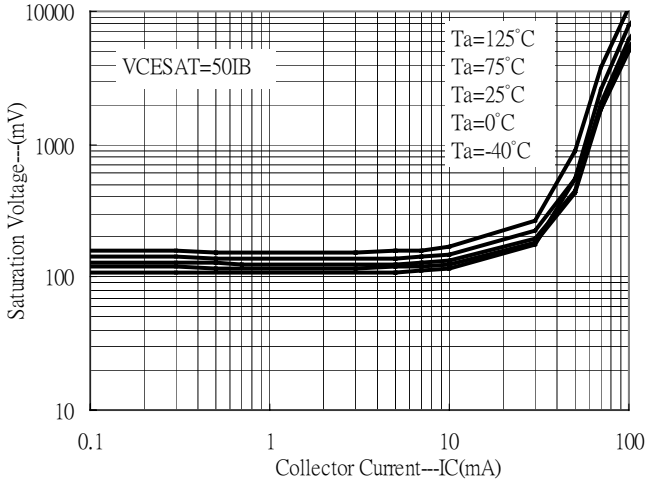
Current Gain vs Collector Current



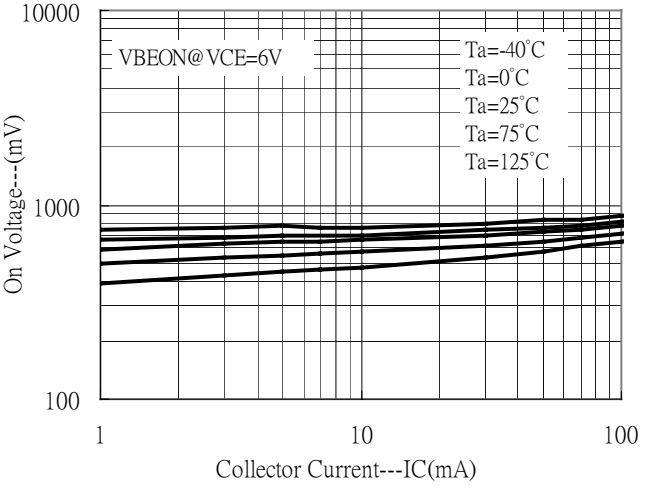
Saturation Voltage vs Collector Current



Saturation Voltage vs Collector Current

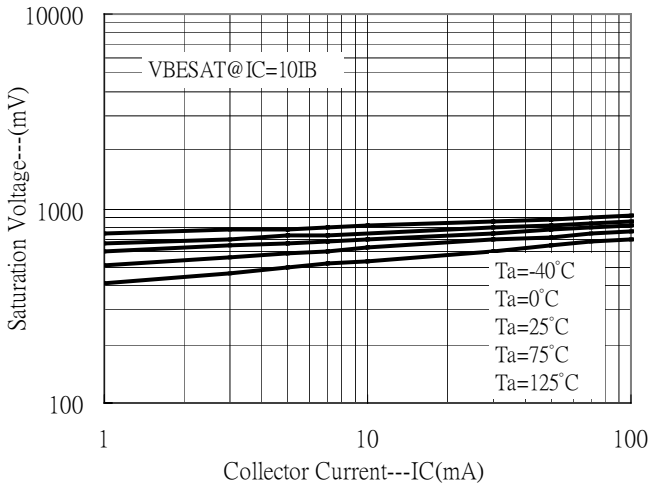


On Voltage vs Collector Current

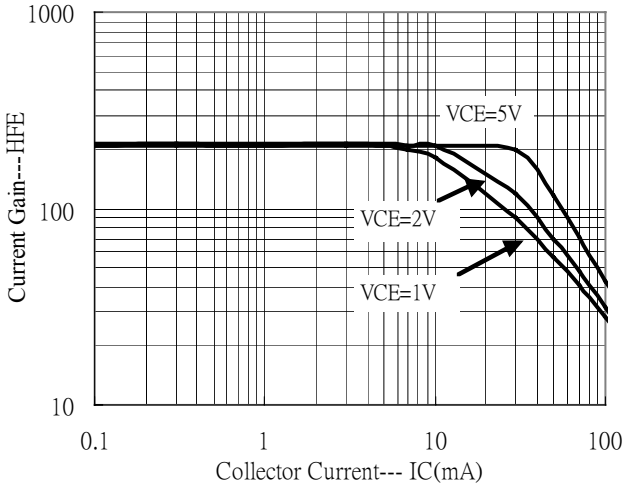


Typical Characteristics(Cont.)

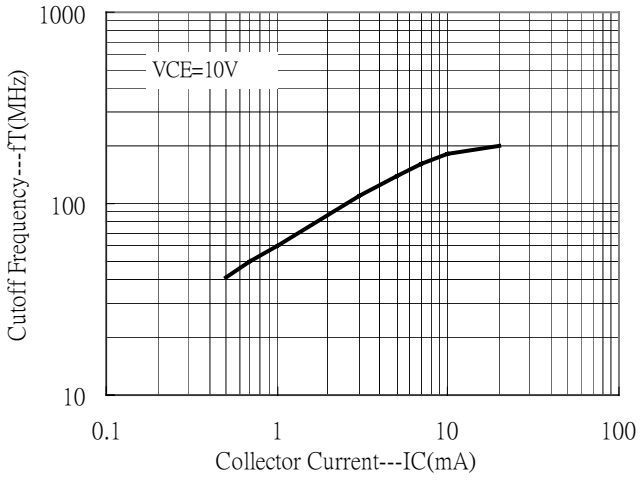
Saturation Voltage vs Collector Current



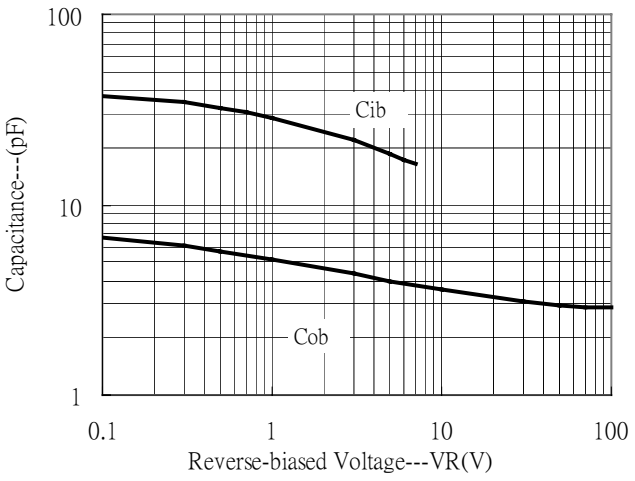
Current Gain vs Collector Current



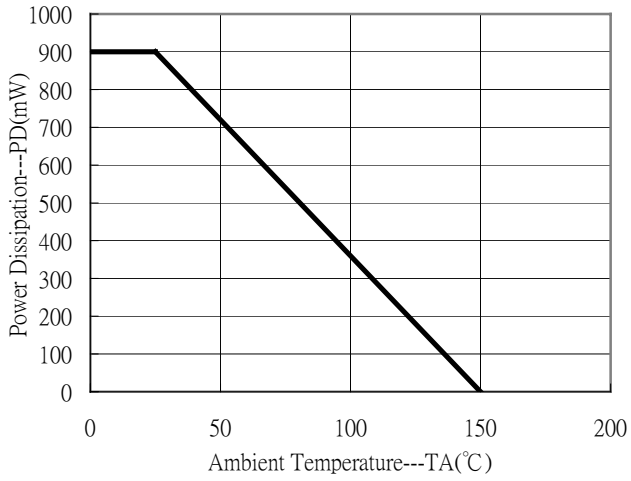
Cutoff Frequency vs Collector Current



Capacitance vs Reverse-biased Voltage



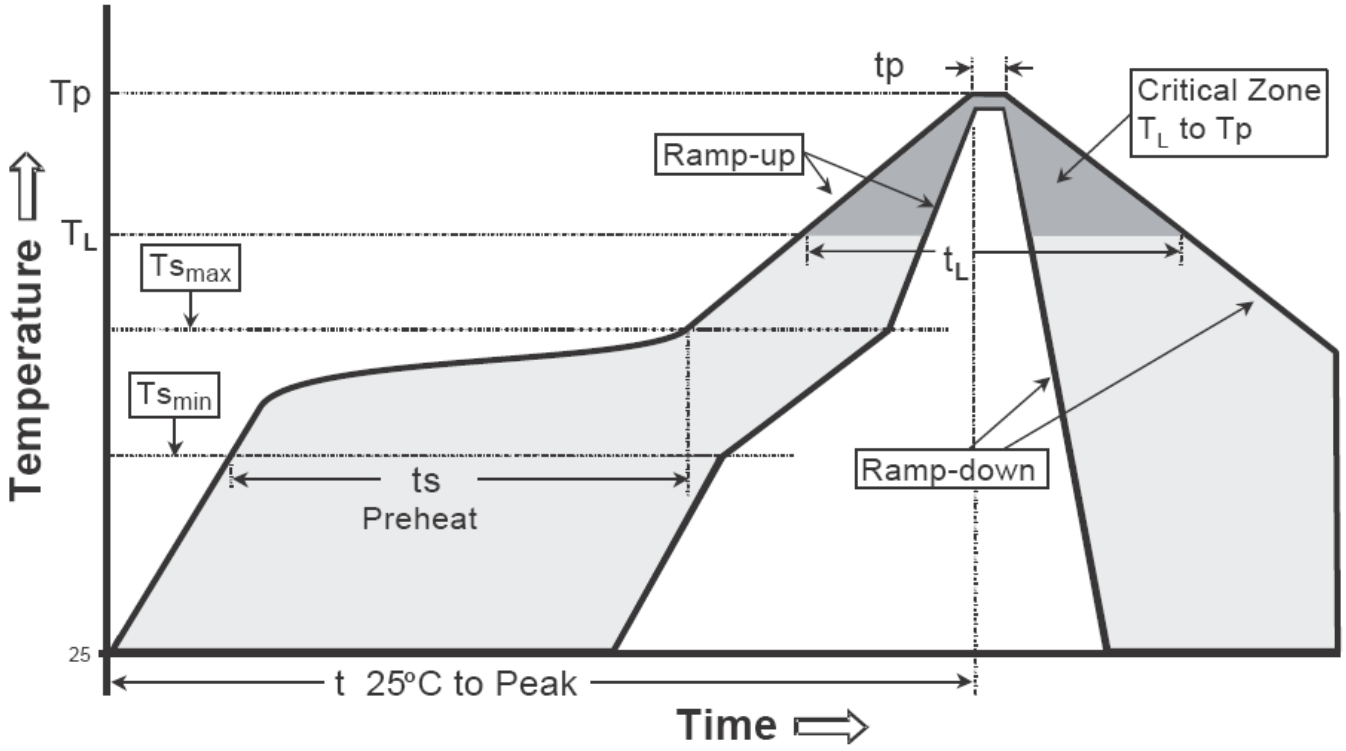
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

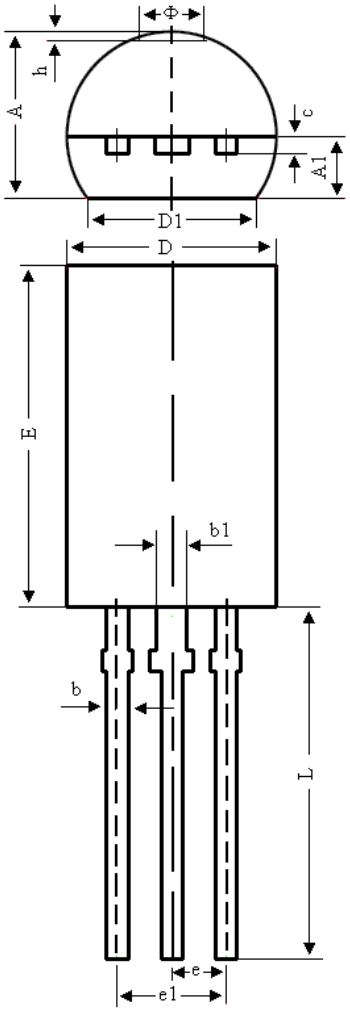
Recommended temperature profile for IR reflow

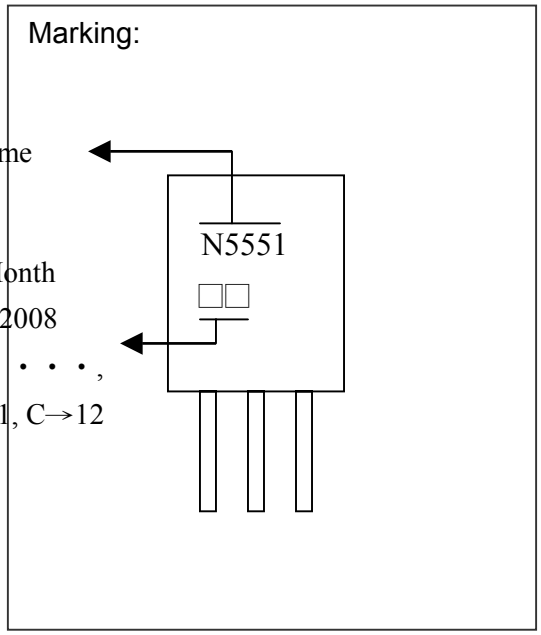


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-92L Dimension





Date Code: Year+Month
Year: 7→2007, 8→2008
Month: 1→1, 2→2, ・・・,
9→9, A→10, B→11, C→12

Style: Pin 1.Emitter 2.Collector 3.Base

3-Lead TO-92L Plastic Package
CYStek Package Code: K3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.146	0.161	3.700	4.100	E	0.307	0.323	7.800	8.200
A1	0.050	0.062	1.280	1.580	e	*0.05		*1.270	
b	0.014	0.022	0.350	0.550	e1	0.096	0.104	2.440	2.640
b1	0.024	0.031	0.600	0.800	L	0.543	0.559	13.800	14.200
c	0.014	0.018	0.350	0.450	φ	-	0.063	-	1.600
D	0.185	0.201	4.700	5.100	h	0.000	0.012	0.000	0.300
D1	0.157	-	4.000	-					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.