BTN8960 /62 /80 /82

High Current PN Half Bridge
NovalithIC™

Application Note

Rev. 0.3, 2014-09-11

Automotive Power

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1 Abstract

Note: The following information is only given to help with the implementation of the device and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide information and hints for a high current design, using PWM control with the NovalithIC™ half-bridge family BTN89xy for the automotive environment.

This family contains one P-channel high side MOSFET and one N-channel low side MOSFET with an integrated driver IC in one package. The NovalithIC™ is the interface between the microcontroler and the motor, equipped with diagnostic and protection functions.

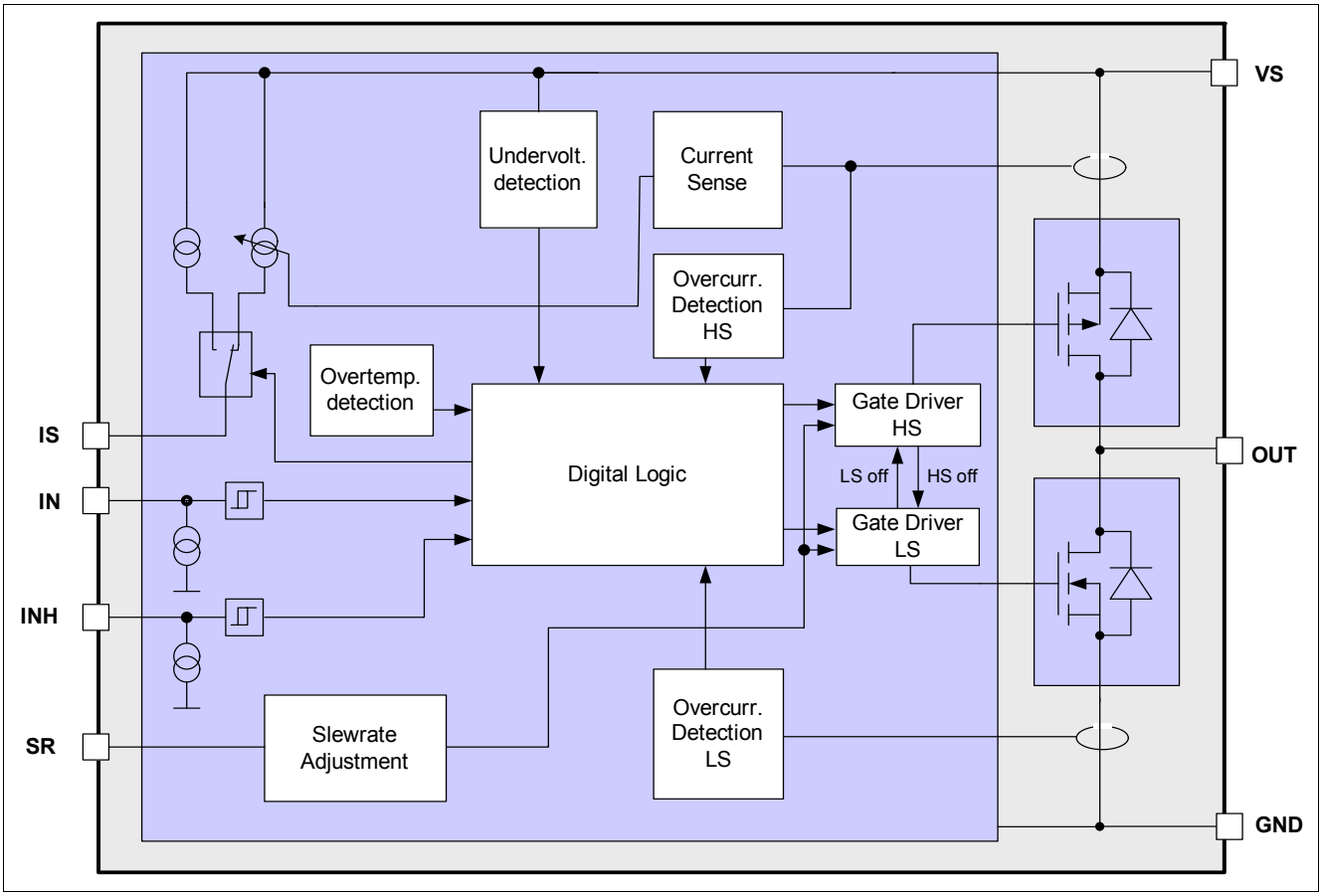

Figure 1 Block Diagram BTN89xy

2 Motor Configurations

Electrical motors are built with various architectures. Mechanically commutated motors with brushes, so called DC motors or electrically commutated motors, so called BLDC motors (Brush Less DC motors). The NovalithIC™ family can support all of them due to, the flexibility of the half-bridge concept.

Using NovalithIC™ controlling a DC-motor has the following advantages:

- Extremely low parasitic inductances between high side and low side MOSFET.
- Optimized switching performance of the MOSFET's to reduce power losses and EMC emission.
- Driving the motor with PWM for torque and speed control.
- Integrated freewheeling transistor.
- Integrated current measurement.
- Integrated diagnosis and protection.
- Microcontroller -compatible input pins.
- Small and PCB-area saving package.

2.1 Half-bridge configuration for mono-directional motor control

Figure 2 shows the design of a mono-directional motor control with NovalithIC™. In most cases, the motor is connected between "OUT" and "GND". This is because the chassis of a car is "GND", and therefore a short to "GND" is much more probable than a short to "Vs". For this reason it is statistically safer with a motor connected to "GND", because if a short accures in this case, the motor is not running.

Generally, it is also possible to use the NovalithIC™ to drive the motor between "OUT" and "Vs". The inverted "IN" signal must be respected.

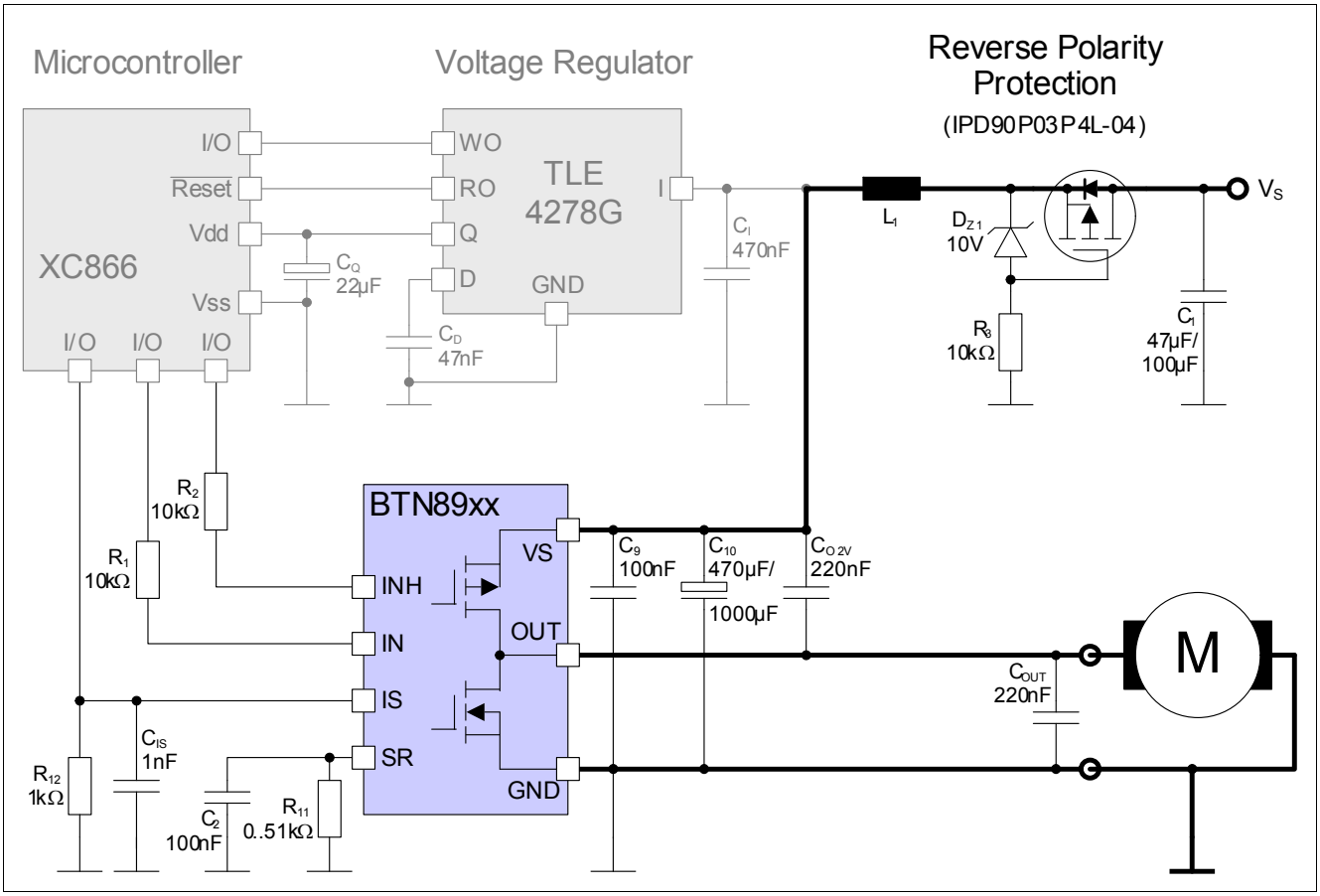

Figure 2 Application circuit for a monodirectional motor with BTN89xy

2.2 H-Bridge configuration for bidirectional motor control

With the NovalithIC™ family it is easy to build an H-bridge for bidirectional DC motor control by simply combining two devices in H-bridge configuration, as it is shown in **Figure 3** .

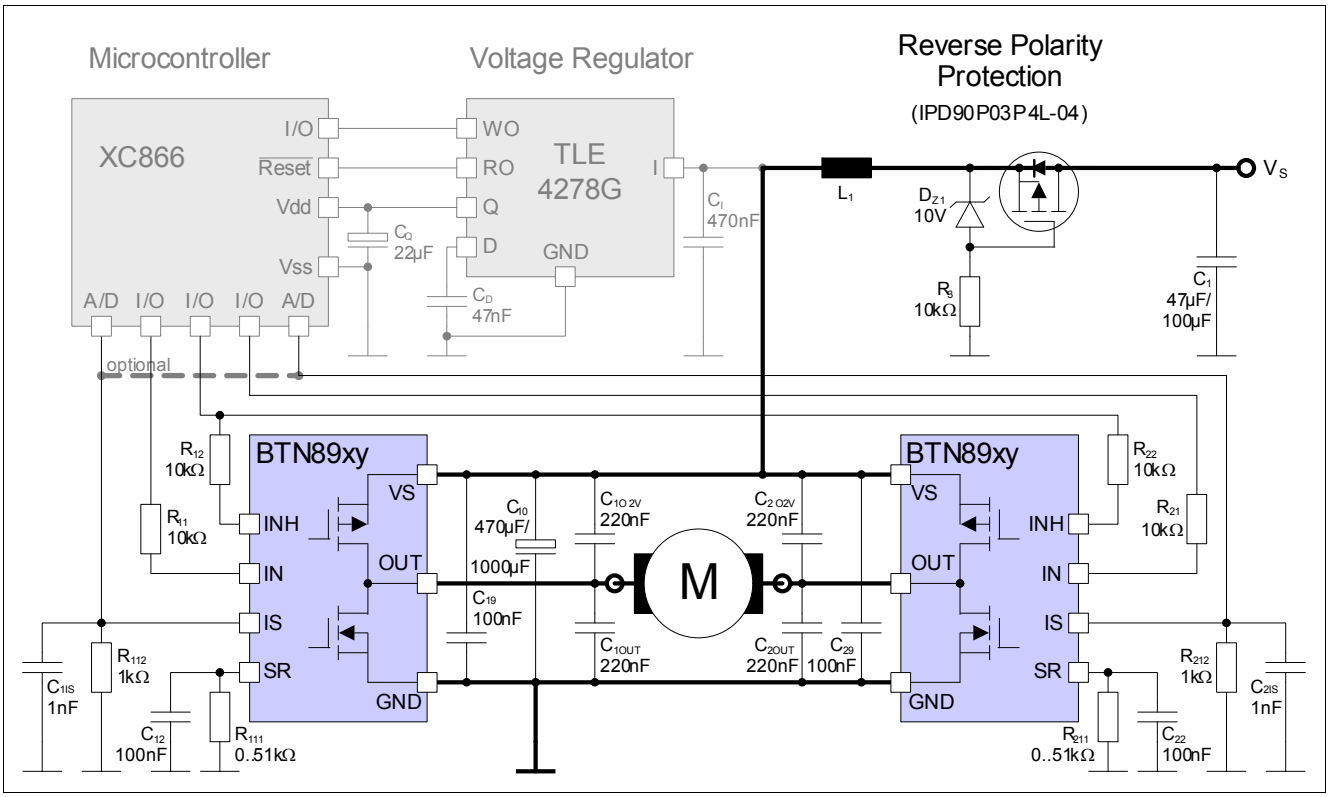

Figure 3 Application circuit for a bidirectional motor with BTN89xy H-bridge

3 Parasitic Inductance

In high-current applications, which the NovalithIC™ family is designed for, special care must be taken for parasitic inductors. The same is valid in case of very high frequencies, which are interesting with regard to EMC considerations.

Each kind of wire in the application is an inductor, e.g. PCB wires, bond wires, etc. The wire inductance can be estimated with

- 1mm PCB wire length approximately 1.2 nH
- 1 PCB via approximately 1 nH

The voltage drop of a wire can be calculated in the following way:

(1)

$$U_L = L \cdot \frac{dI}{dt}$$

As can be seen from this equation, care must be taken with the parasitic wire inductors with increasing current and decreasing switching time. The NovalithIC™ is designed to switch high currents very quickly. This means in applications with NovalithIC™, the parasitic inductors are relevant and special care must be taken.

3.1 Measuring signals at NovalithIC™

The parasitic inductance also has an influence on the measurement results. To measure the true signals at the NovalithIC™ it is mandatory to position the measurement probes directly at the device, as it is shown in **Figure 4**. The probe is connected directly to the Vs-pin of the NovalithIC™ and the reference signal directly to the GND-pin of the device.

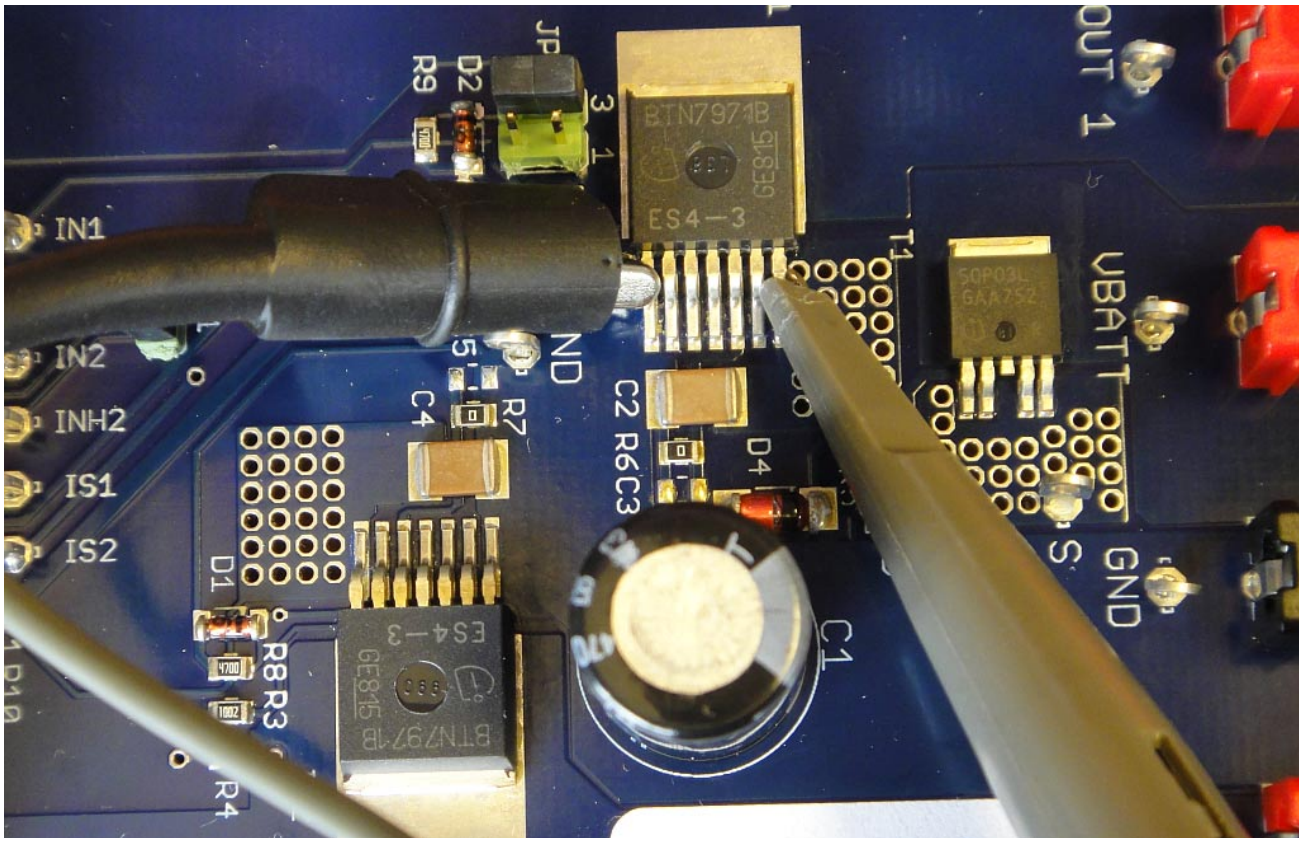

Figure 4 Measuring Vs with probe and reference directly connected to the NovalithIC™

Doing so enables to monitoring of the NovalithIC™ supply voltage when high currents are switched. For example when a short-circuit current is switched, this is the only possibility for measurement if the DC-link capacitor is sufficient to keep the supply voltage above the undervoltage detection threshold (also see **Chapter 4.2**).

4 Design guideline

For a safe and sufficient motor control design, discrete components are needed. Some of them must be dedicated to the motor application and some to the NovalithIC™.

4.1 Schematic and layout design rules

Figure 5 and **Figure 6** show an example of a schematic plus a corresponding layout for a half-bridge motor control with NovalithIC™.

The best performance in terms of parasitic inductance and EMC can be reached with a GND plane, which we strongly recommend be used.

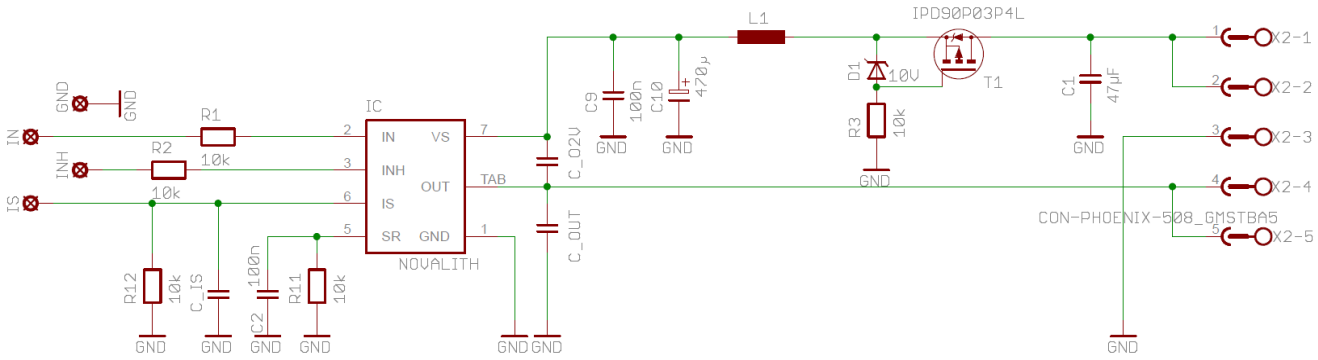

Figure 5 Example of a half-bridge schematic with NovalithIC™

Important design and layout rules:

The basis for the following items is the parasitic inductance of electrical wires, as described in **Chapter 3**.

- C10, so called DC-link capacitor: This electrolytic capacitor is required to keep the voltage ripple at the VS-pin of the NovalithIC™ low during switching operation (the measurement procedure for the supply voltage is described in **Chapter 3.1**). It is strongly recommended that the voltage ripple at the NovalithIC™ Vs-pin to GND-pin be kept below 1 V peak to peak. The value of C10 must be aligned accordingly. See **Equation (10)**. Most electrolytic capacitors are less effective at cold temperatures. It must be assured that C10 is also effective under the worst case conditions of the application.
  The layout is very important. As shown in **Figure 6**, the capacitor C10 must be positioned with very short wiring at the NovalithIC™. This must be done to keep the parasitic inductors of the PCB-wires as small as possible.
- C9: This ceramic capacitor supports C10 to keep the supply voltage ripple low and covers the fast transients between the Vs-pin and the GND-pin. The value of this ceramic capacitor must be chosen so that fast Vs-ripple at the NovalithIC™ does not exceed 1V peak to peak.
  The layout wiring for C9 must be shorter than for C10 to the NovalithIC™ to keep the parasitic PCB-wire inductance as small as possible. In addition the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- C_O2V: This ceramic capacitor is important for EMI in order to avoid entering electro magnetic disturbances into the NovalithIC™ as much as possible. Good results have been achieved with a value of 220nF.
  In terms of layout, it is important to place this capacitor between “OUT” and “Vs” without significant additional wiring from C_O2V to the Vs- and OUT-line.
- C_OUT: This ceramic capacitor helps improve the EMI and the ESD performance of the application. Good results have been achieved with a value of 220nF.
  To keep the RF and ESD out of the board, the capacitor is most effective when positioned directly on the board connector. In addition, the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.

- C1: This ceramic capacitor helps to improve the EMI and the ESD performance. In combination with L1 and C10 plus C9 a Pi-filter improves the electro magnetic emission on the Vs-line.
  Layout rules are the same as for C_OUT.

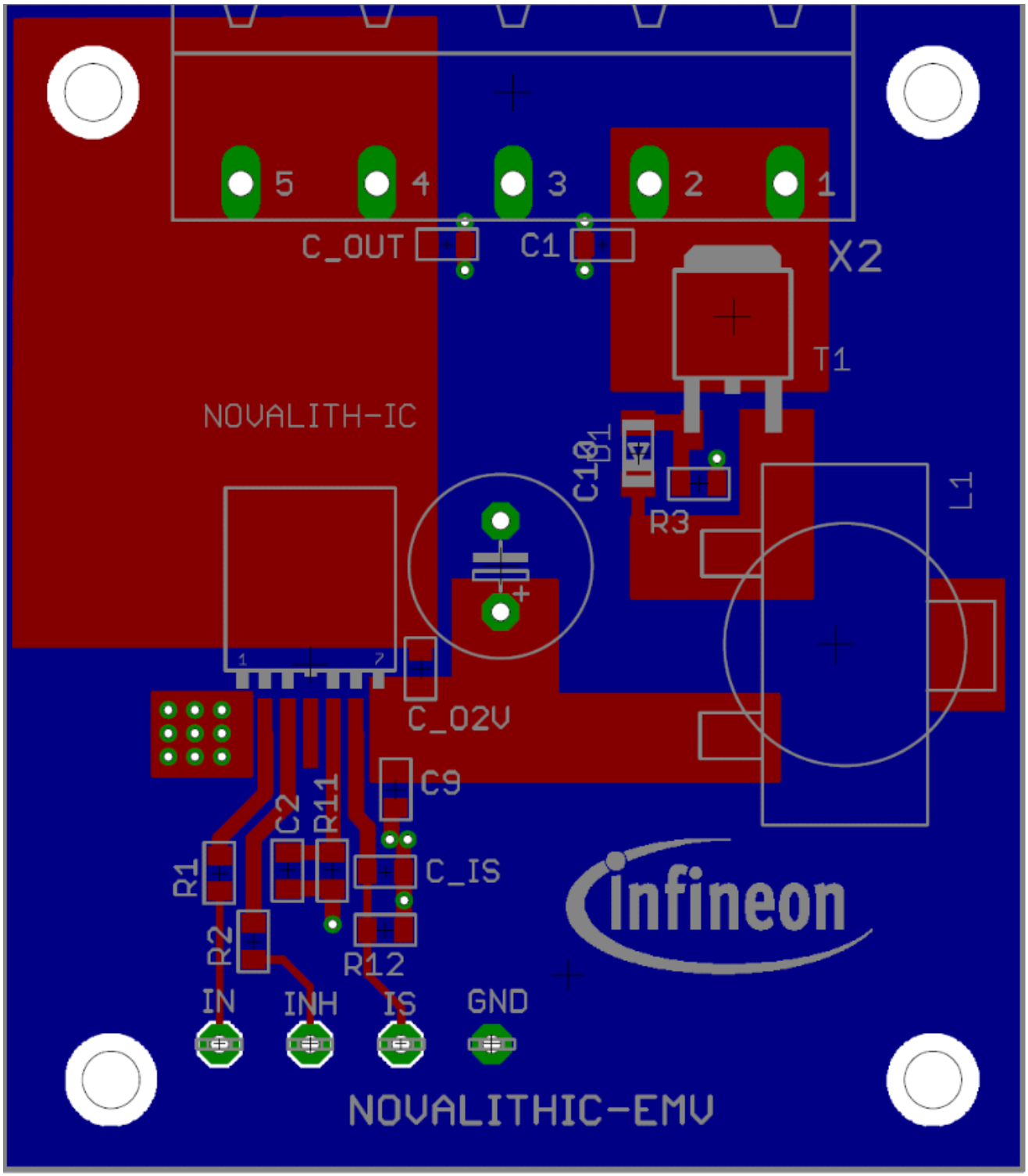

Figure 6 Example of an half-bridge layout with NovalithIC™ (not true to scale)

Other components:

- T1, D1 and R3: Reverse polarity protection. See **Chapter 4.4**.

- R11: Slew rate resistor according to data sheet.
- C2: Stabilization for slew rate resistor (R11).
- R12: Resistor to generate a current sensing voltage from the IS current.
- C_IS: Ceramic capacitor for EMI improvement. GND connection with at least two GND-vias. A good value is 1nF.
  In case the current should be measured during the PWM-phase this capacitor must be adapted to the ON-time inside the PWM-phase.
- R1 and R2: Device protection in case of µC pins shorted to Vs.

4.2 DC-link capacitor

For the stability of the DC-link voltage a sufficient capacitor is mandatory (in **Figure 2**, **Figure 3** and **Figure 5** it is C10). This is one of the most important component in a motor design with semiconductor switches.

The DC-link capacitor could be insufficient, because:

- The capacitor value is too small.
- The ESR of the capacitor is too high.
- When cold the capacitor value is too small.
- The distance between the DC-link capacitor and the NovalithIC™ is too large.
- The wiring between the DC-link capacitor and the NovalithIC™ is too long (see **Chapter 3**).

The value must be chosen carefully, taking the under-voltage toggling into account, which is described in **Chapter 4.2.2**.

4.2.1 Calculation of the DC-link capacitor and Pi-filter

As already mentioned in the design- and layout-rules of **Figure 5** the voltage ripple at the NovalithIC™ Vs-pin must not exceed 1V peak to peak. The necessary DC-link capacitor can be estimated in the following way:

Motor control with PWM means for the DC-link voltage to provide energy pulses during the “ON-phase” of the PWM cycle. The DC-link pulses are shown in **Figure 7**.

This energy must be provided by the DC-link capacitor. This can generally be described with

(2)

$$E = \frac{1}{2} \cdot C \cdot V^2 = P \cdot T$$

(3)

$$C = C_{DC-link}$$

The voltage at the DC-link capacitor consists of the DC-part and the delta voltage from the supply ripple.

(4)

$$V = V_{S,DC} + \Delta V_S$$

The total power in this system consists of the DC-power plus the power of the energy pulse (E_{pulse}), which provides the energy to the motor during the ON-phase of the half bridge.

(5)

$$P = P_{DC} + \Delta P$$

The maximum pulse length is determined by the PWM frequency, theoretically at a duty cycle of 100%:

(6)

$$T = T_{pulse} = T_{PWM} = \frac{1}{f_{PWM}}$$

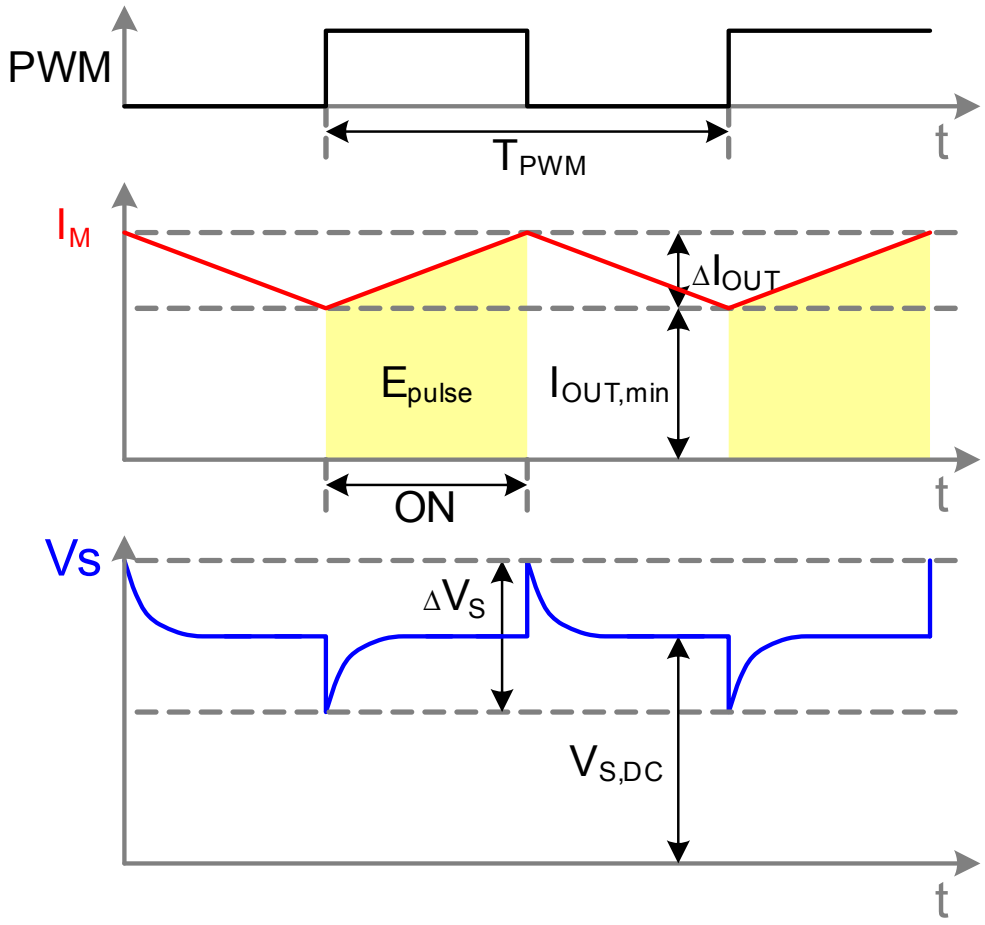

Figure 7 PWM control (PWM=IN-pin-signal, I_M=motor current and V_S=V_S-pin-voltage @ NovalithIC)

Insertion of **Equation (3)** to **Equation (6)** into **Equation (2)**

(7)

$$E = \frac{1}{2} \cdot C_{DC-link} \cdot (V_{S,DC} + \Delta V_S)^2 = (P_{DC} + \Delta P) \cdot T_{PWM}$$

(8)

$$\frac{1}{2} \cdot C_{DC-link} \cdot (V_{S,DC}^2 + 2 \cdot V_{S,DC} \cdot \Delta V_S + \Delta V_S^2) = P_{DC} \cdot T_{PWM} + \Delta P \cdot T_{PWM}$$

(9)

$$\frac{1}{2}\cdot C_{DC-link}\cdot V_{S,DC}^2 + C_{DC-link}\cdot V_{S,DC}\cdot \Delta V_S + \underbrace{\frac{1}{2}\cdot C_{DC-link}\cdot \Delta V_S^2}_{negligible} = P_{DC}\cdot T_{PWM} + \Delta P\cdot T_{PWM}$$

Finally the equation to calculate the DC-link capacitor is:

(10)

$$\boldsymbol{C_{DC-link} \geq \frac{\Delta P\cdot T_{PWM}}{V_{S,DC}\cdot \Delta V_S}}$$

(11)

$$\Delta P = V_S\cdot I_{nom} \approx V_S\cdot (I_{OUT,\min} + \frac{1}{2}\Delta I_{OUT})$$

The DC-link capacitor is primarily the energy buffer for the switching process of the PWM motor control. Secondly it is part of the Pi-filter. This means first the DC-link capacitor must be calculated according to **Equation (10)**. Based on this, it is recommended that the second capacitor of the Pi-filter C1 be estimated with:

(12)

$$\boldsymbol{C_1 = \frac{1}{10}\cdot C_{DC-link} = \frac{1}{10}\cdot C_{10}}$$

Generally the border frequency of the L_1-C_1-filter is determined with

(13)

$$f_g = \frac{1}{2\cdot \Pi\cdot \sqrt{L_1\cdot C_1}}$$

We recommend setting the border frequency f_g to half the value of the PWM -frequency f_{PWM}.

(14)

$$f_g = \frac{1}{2}\cdot f_{PWM} = \frac{1}{2\cdot \Pi\cdot \sqrt{L_1\cdot C_1}}$$

(15)

$$\boldsymbol{L_1 = \frac{1}{\Pi^2\cdot f_{PWM}^2\cdot C_1}}$$

Summary:

First calculate the DC-link capacitor with **Equation (10)**.

Second calculate the other capacitor of the Pi-filter with **Equation (12)**.

Then calculate the inductor of the Pi-filter with **Equation (15)**.

And last but not least, do not forget the important layout rules and how to measure the supply voltage correctly.

4.2.2 Under-voltage toggling

The power supply cable of most modules in a car are several meters long. The longer the supply cable is, the higher its parasitic inductance. In addition, most modules have a Pi-filter at the supply line with a inductor for EMC reasons. The sum of the supply line inductances have a significant influence on the Vs-voltage. When switching the motor ON during a normal motor start or PWM control, with a insufficient DC-link capacitor the supply voltage drops below the under-voltage threshold and the NovalithIC™ is switched to tristate. The supply voltage recovers above the under-voltage threshold and the NovalithIC™ switches on again, again dropping below the under-voltage threshold . . .

This effect can result in frequencies higher than 100kHz, as is shown in **Figure 8**. The device will be damaged by the power dissipation of the switching losses, which is faster than the reaction time of the over temperature shut down, because of the high switching frequency.

The under-voltage toggling will be worse if the OUT is shorted to GND.

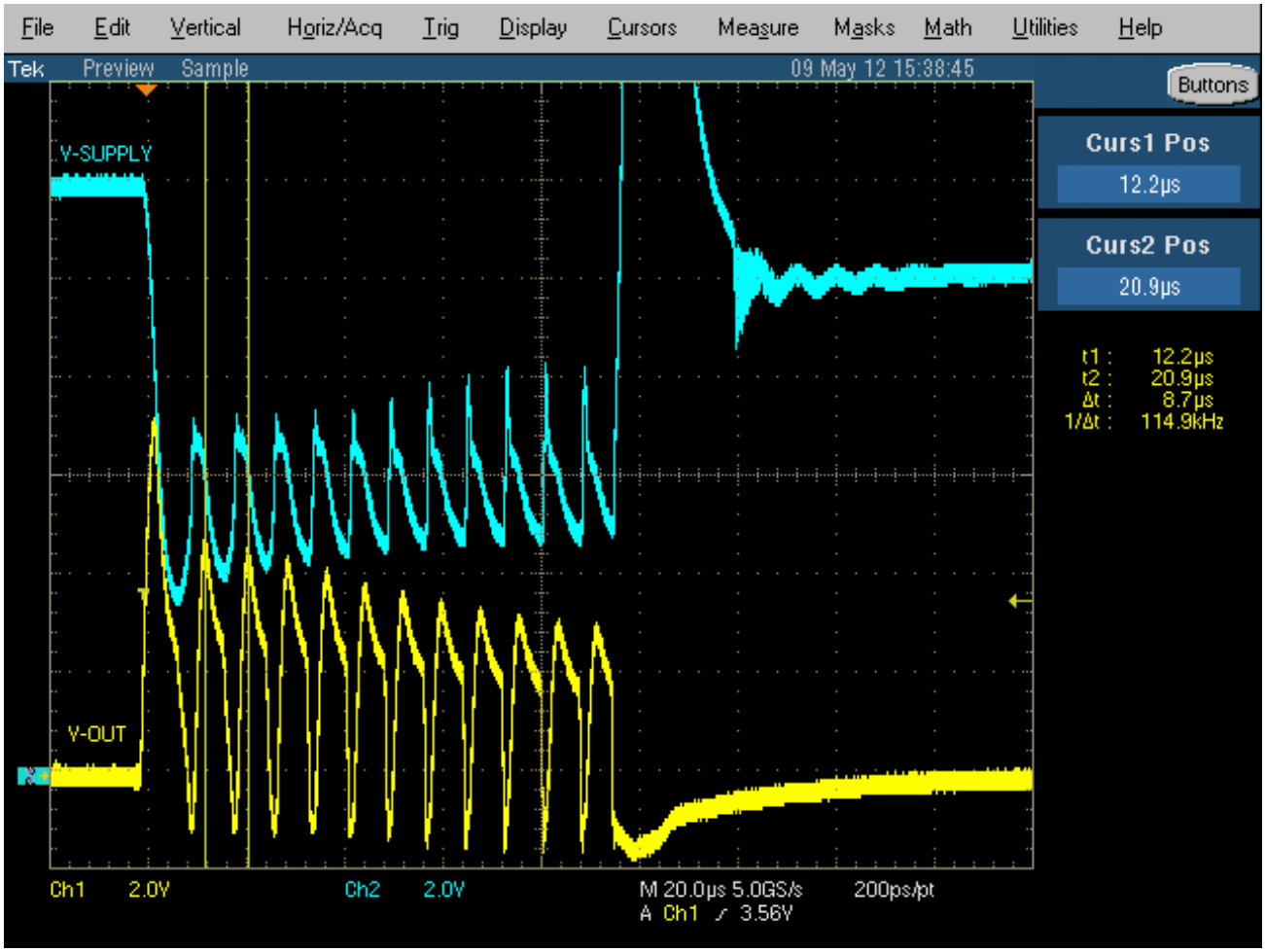

Figure 8 Under-voltage toggling started by short to GND and enabled by an insufficient DC-link capacitor.

With a sufficient DC-link capacitor the supply voltage drop is limited so as not to reach the under-voltage threshold, as is shown in **Figure 9**.

Both measurements in **Figure 8** and **Figure 9** are conducted with the Infineon “NovalithIC Demo Board V2.1” with BTN7933. The “ON-time” is limed to 100µs by the IN-signal, as shown in **Figure 9**. Only the DC-link capacitor is switched between the two measurements.

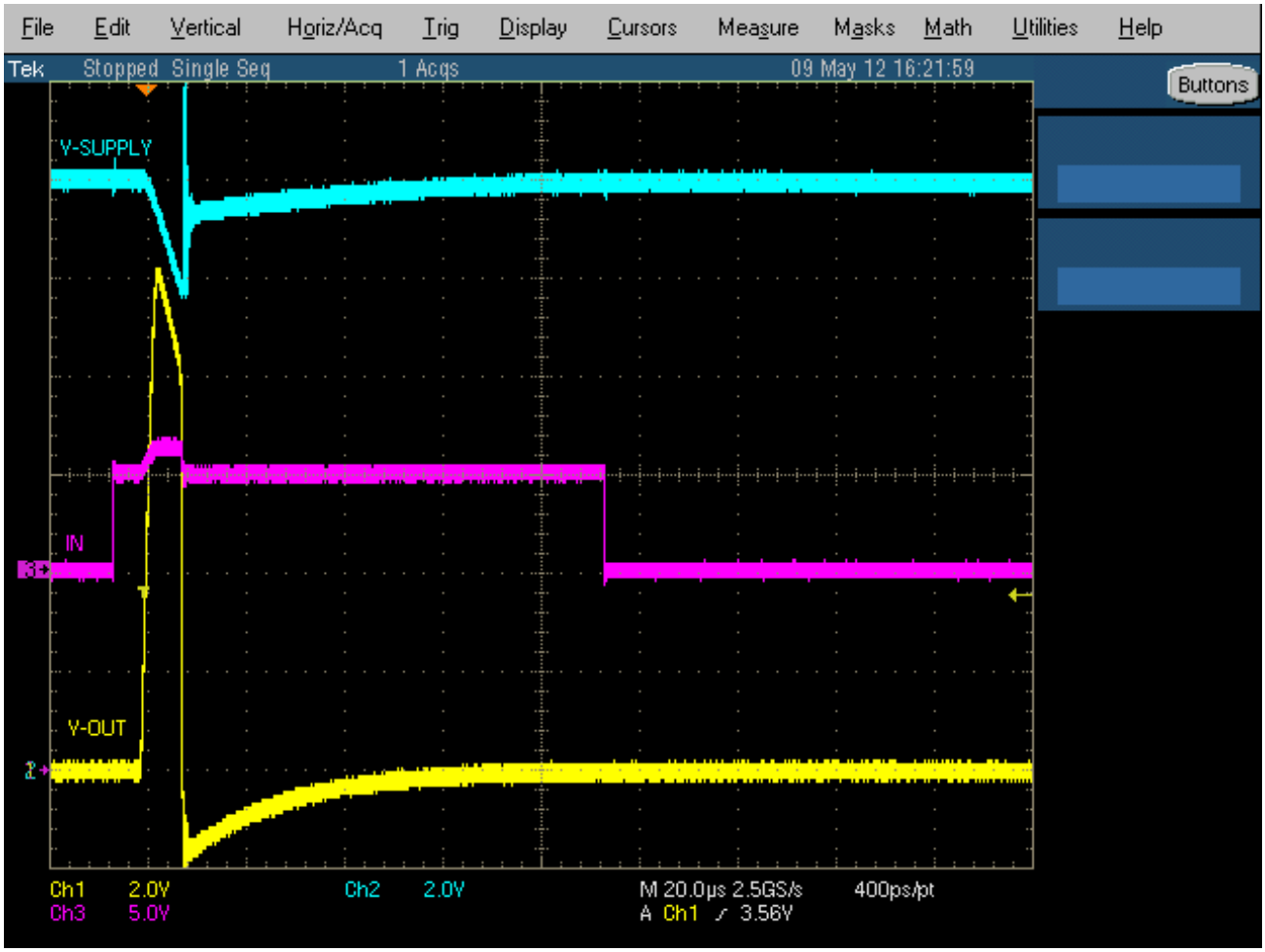

Figure 9 The sufficient DC-link capacitor avoided under-voltage -toggling in case of a short to GND.

4.3 Driving inductive loads over long wires

Inductive loads have a lowpass filter characteristic, like a motor. Because of this, the wire from the NovalithIC™ OUT to the motor injects electro magnetic disturbances into the OUT-pin. This antenna effect increases as the length of the motor wire increases.

The definition of a long motor wire strongly depends on the application and the environment. To provide a general idea, wire lengths of approximately 20cm and more are considered as “long wire”. The motor wire should therefore be as short as possible.

4.3.1 PWM operation

In case of a long motor wire and PWM operation the electro magnetic emission (EME) increases with the wire length and with the switching speed (inversion of $t_{r(HS)}$, $t_{r(LS)}$, $t_{f(HS)}$ and $t_{f(LS)}$). In this case it is advantageous to reduce the switching speed with the slew rate resistor at the SR-pin (see **Figure 5**, R_{11}). Reducing the switching speed has probably a impact on the PWM-frequency, which may needs to be adapted. In any case the power dissipation and the cooling concept needs to be reviewed. The slew rate resistor at the SR-pin should not exceed the max. slew rate resistor value of the data sheet $R_{SR} \leq 51k\Omega$.

4.3.2 Current sense

A long motor wire can pick up electro magnetic disturbances which could influence the current sense signal at the IS-pin. If a high accuracy of the current measurement is needed, it is recommended to use the IS-pin as status flag diagnosis and perform the current measurement with an external shunt plus current sense amplifier. An schematic example is shown in **Figure 10**.

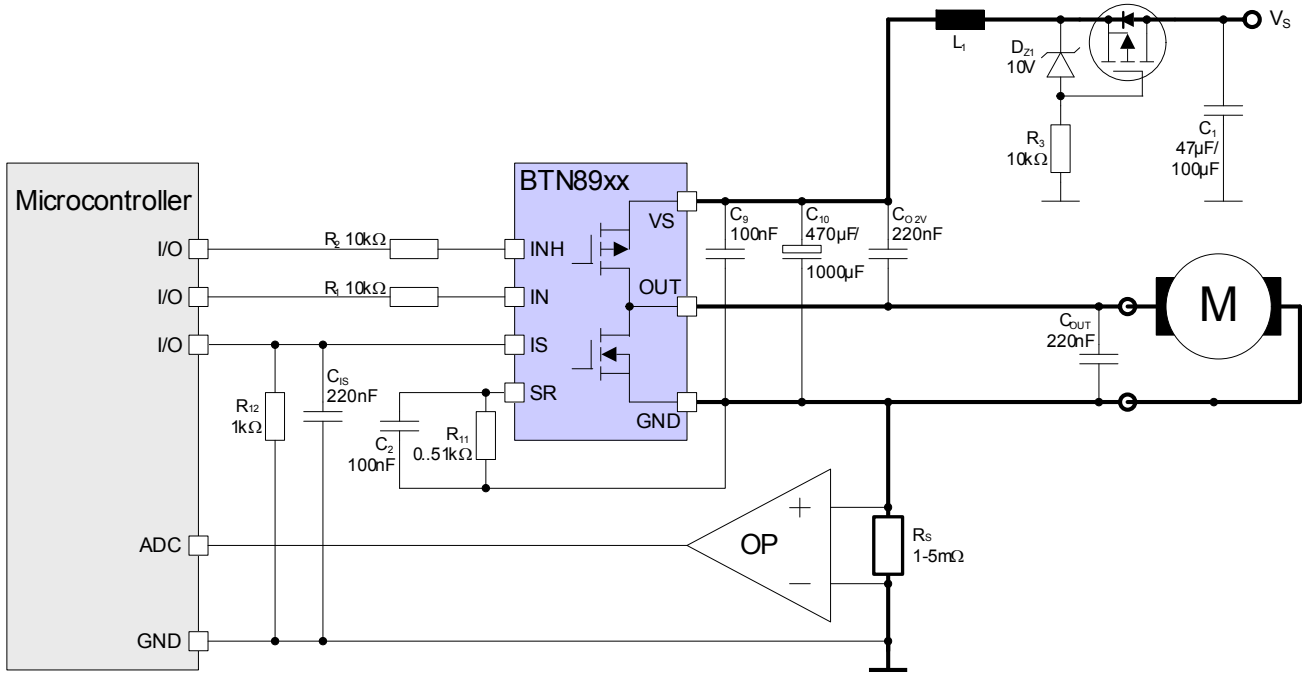

Figure 10 BTN89xx with external current measurement.

4.4 Reverse polarity protection

The semiconductor technology of NovalithIC™ used has a parasitic PN -diode from “GND” to the supply voltage pin “Vs”. If the supply voltage is inverted, a huge current will flow through this parasitic PN -diode and will damage the device. With reverse polarity protection, the reverse current is not possible and the semiconductor components of the design are protected.

In the schematic in **Figure 5**, reverse polarity protection is provided with a P-channel MOSFET (IPD90P03P4L-04), a zener-diode (D_1) and a resistor (R_3).

Normal operation Vs > GND:

- P-MOSFET OFF: The application is supplied by the body-diode of the reverse polarity protection transistor (IPD90P03P4L-04), e.g. in case of a power-up. The status “P-MOSFET ON” will quickly be reached.
- P-MOSFET ON: After the power-up in which the body diode was used as a supply path, the zener diode plus the resistor will generate a gate-source voltage in the range of 10V and the P-MOSFET is in ON-state. Only the $R_{DS,on}$ is in the power supply path.

Reverse polarity condition Vs < GND:

- The gate source voltage of the reverse polarity protection transistor is continuously “LOW” and the transistor is switched OFF. No current can flow in this state. The application will not be damaged.

4.5 Cooling

The NovalithIC™ half-bridge, driving high current generates power dissipation. These are R_{ON} losses and switching losses in case of PWM control, which heat up the device. For details, please see **Chapter 6**. The

package PG-TO263-7-1 provides a low thermal resistance which can be combined with a heat sink on the PCB to avoid exceeding the absolute maximum temperature values of the data sheet.

In **Figure 6** a cooling area (brown top layer, where the NovalithIC™-OUT is connected) has already been drawn. Depending on the power dissipation, other thermal sources on the PCB and the ambient temperature, the cooling needs to be carefully adapted to each application.

In addition the reverse polarity protection transistor T1 (**Figure 5** and **Figure 6**) generates $R_{DS,on}$ power losses and the cooling concept for this transistor must ensure that the device does not exceed the absolute maximum junction temperature.

5 Current Sense Improvement

The NovalithIC™ half-bridge-family has a current sense function with an IS-pin, providing the output current divided by a factor, so called dk_{ILIS}. The precision of the current measurement could be significantly improved by eliminating the IS-offset, dk_{ILIS}-production spread and respecting the temperature dependency of the dk_{ILIS}.

The table below provides an overview, of possible combinations of procedures to reduces current measurement errors.

Table 1 Current sense procedure and benefits

Procedures			Load current tolerance
Offset compensation			±28%
Offset compensation	Device dkILIS measurement		±10%
Offset compensation	Device dkILIS measurement	Temperature estimation	±6%
Offset compensation	Device dkILIS measurement	Temperature compensation	±3%

5.1 Characteristic of the dk_{ILIS}

The dk_{ILIS} has characteristic dependencies. The most important ones with respect to the supply voltage Vs and with respect to the temperature, are described in this chapter.

5.1.1 Supply voltage dependency of dk_{ILIS}

The dependency of the dk_{ILIS} of the supply voltage Vs is negligible, as **Figure 11** shows. This means the supply voltage can be ignored when calculating the load current.

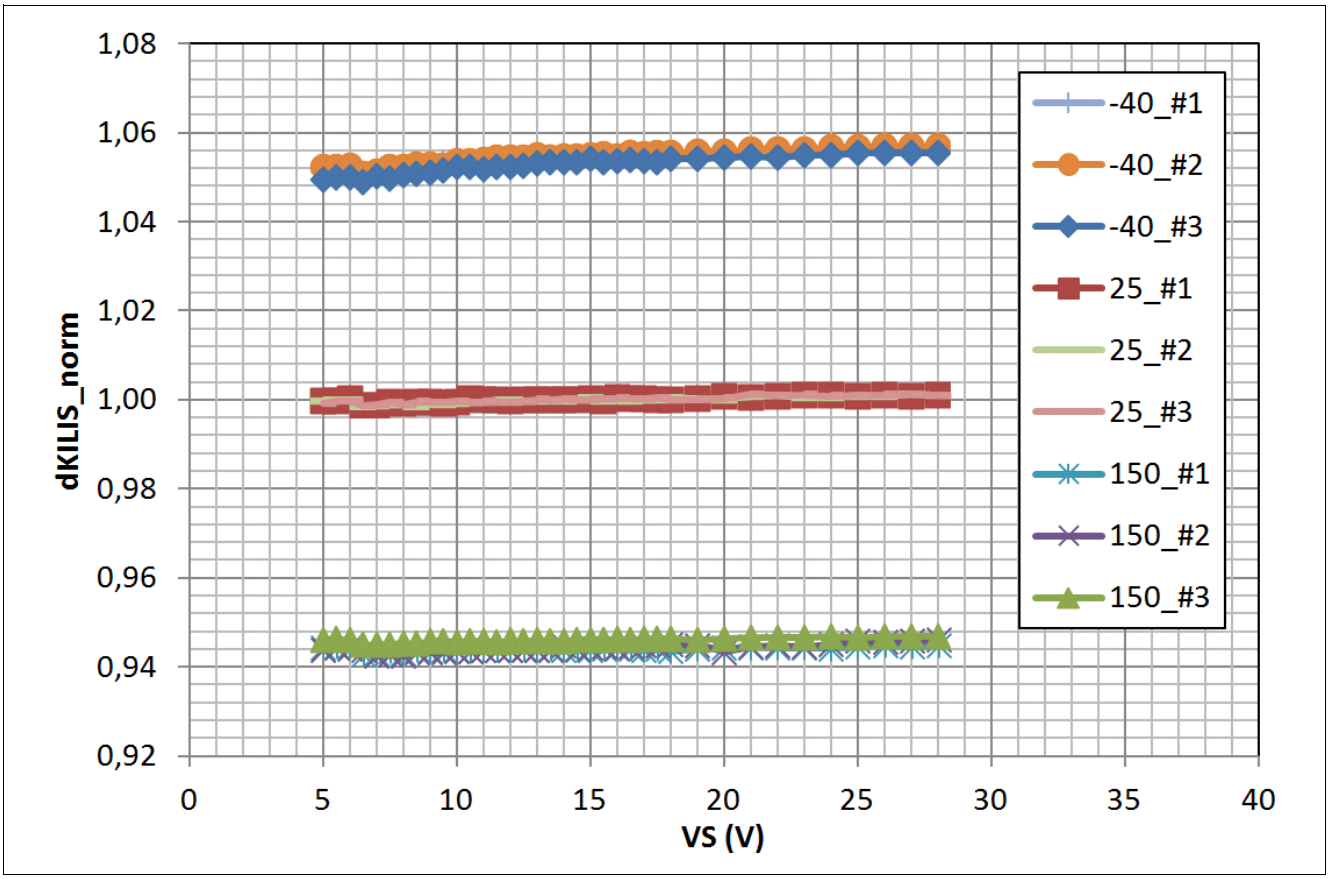

Figure 11 dk_{ILIS} vs. the supply voltage Vs.

5.1.2 TC 1000 life time tests

Life time tests of 1000 hours with a dedicated device stress set up and with many devices from different production lots showed the dk_{ILIS} is decreasing over life time up to -3%.

5.1.3 Temperature drift of the dk_{ILIS}

Figure 12 and **Figure 13** show the characteristics of the dk_{ILIS} vs. temperature and production spread with a scaling at 25°C.

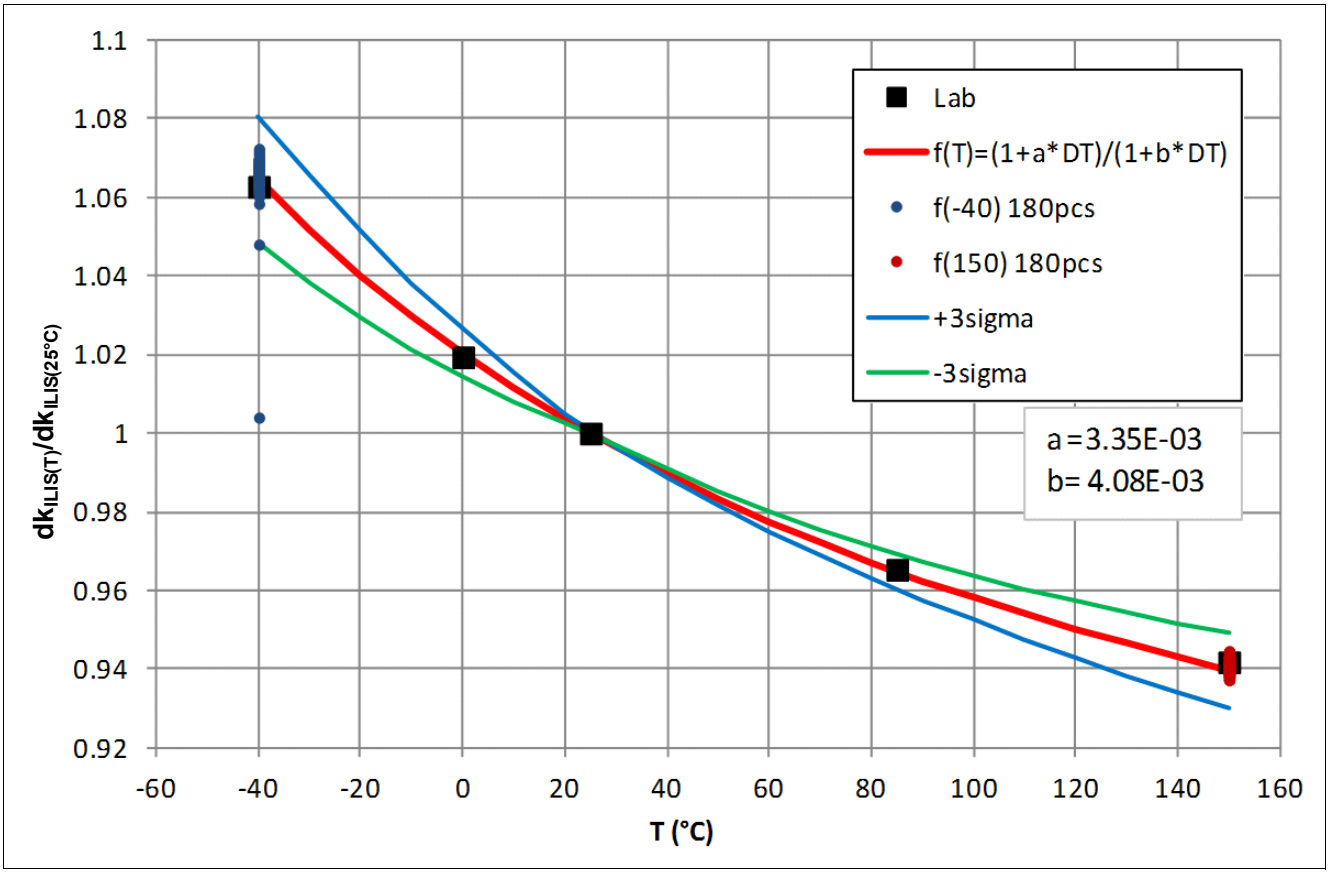

Figure 12 BTN8960 /62 dk_{ILIS} vs. temperature.
The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25°C.

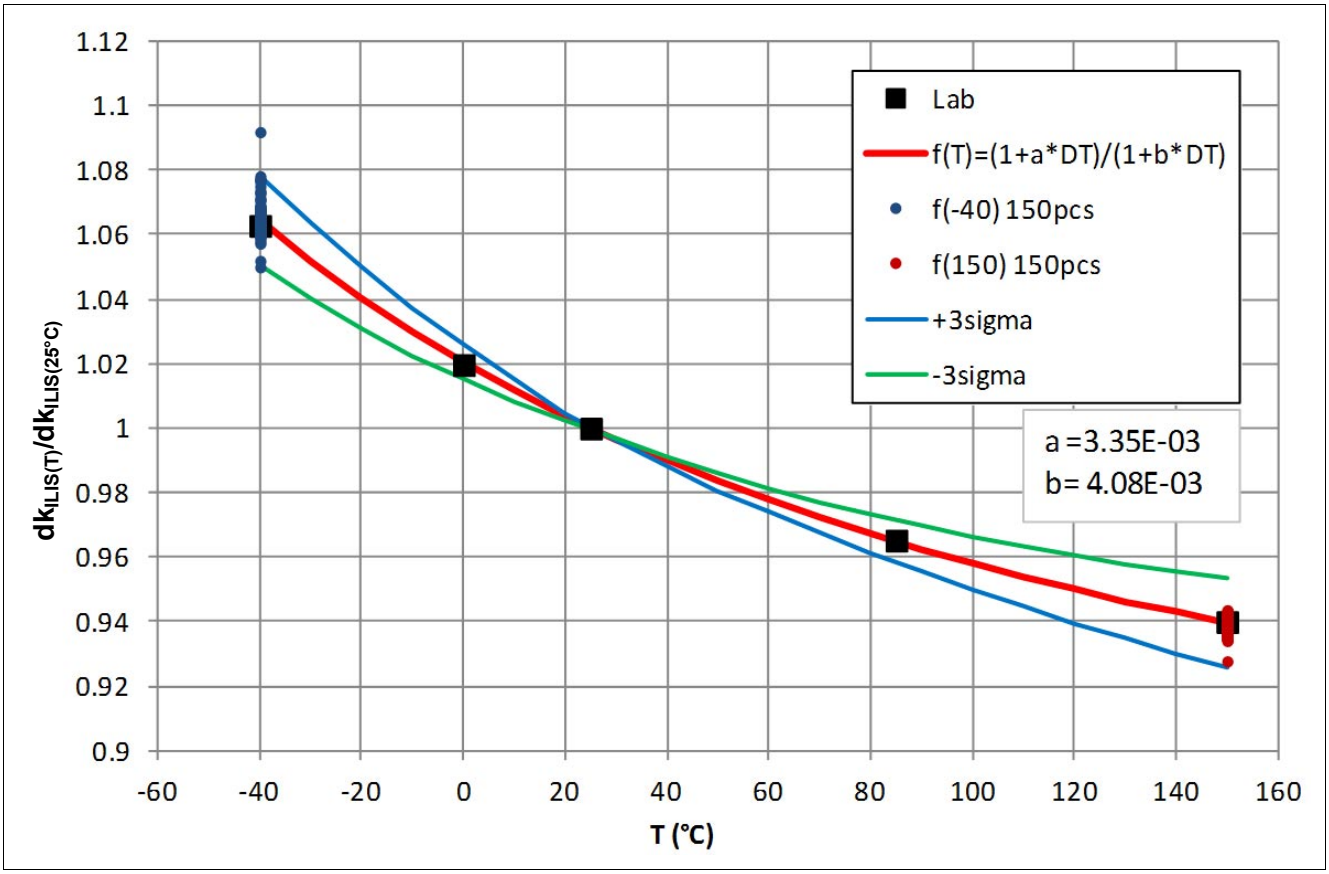

Figure 13 BTN8980 /82 dk_{ILIS} vs. temperature.
The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25°C.

5.2 Offset compensation

The BTN89xy series is featured with an artificial offset current at the IS-pin. This is shown in **Figure 14**.

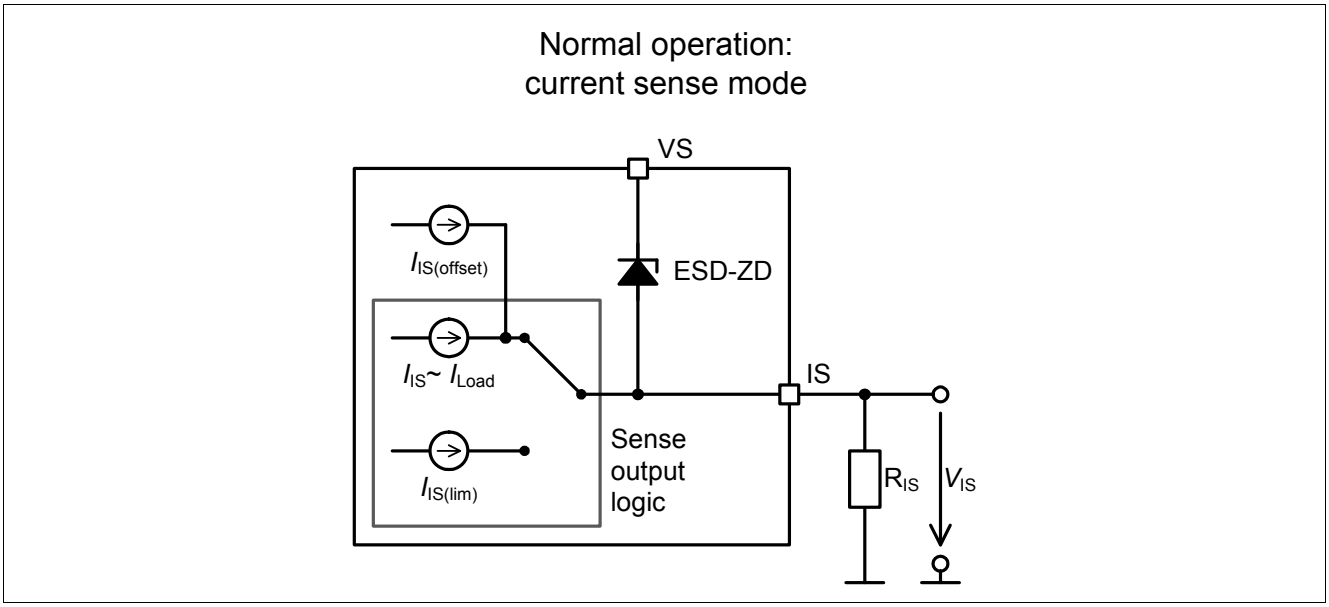

Figure 14 IS-pin internal structure

With this structure, it is possible to always have a measurable offset at IS without a load current. This makes it easy to measure the offset with the microcontroller, store the offset value and process this in the current measurement procedure.

The offset musst be compensated to allow a precise current measurement with the IS-pin.

The offset should be compensated before activating the load. When an application such as a fuel pump runs constantly with PWM, you can perform the offset compensation when INH=high and IN=low. In the PWM-phase, the best measurement results are achieved just before the rising edge of the IN-signal.

With this procedure, the specified dk_{ILIS} of ±28% could be reached, even for small load currents. This includes production spread, temperature dependency and aging. Most errors are caused by production spread, which could be compensated by measuring of the dk_{ILIS} of each device (device-specific dk_{ILIS}). Details of this approach are described in the relevant chapter.

5.3 Device specific dk_{ILIS}

With a measurement of the offset current and one IS-value at a certain load current at 25°C (e.g. 20A), it is possible to determine the individual $dk_{ILIS\text{-}device}$ and store it permanently to the microcontroller of the application. With this value, the graphs in **Figure 12** and in **Figure 13** are valid. The extreme values are shown by the blue line (+3sigma):

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40°C)
- $dk_{ILIS\text{-}min\text{-}H}$ = 0.93 (blue @ 150°C)

Taking into account the aging of the device (see **Chapter 5.1.2**) the minimum value of **Figure 12** and **Figure 13** (blue line) must be reduced by 3% (multiplying 0.97). This means the extreme values are as follows:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40°C)
- $dk_{ILIS\text{-}min\text{-}H\text{-}old} = dk_{ILIS\text{-}min\text{-}H} * 0.97 = 0.9$

This could be assumed as an error of ±10% including temperature drift and aging.

In this case the typical value should be assumed as follows:

- $dk_{ILIS\text{-}typ}$ = 0.99

The device calibration could be implemented in the module test sequence.

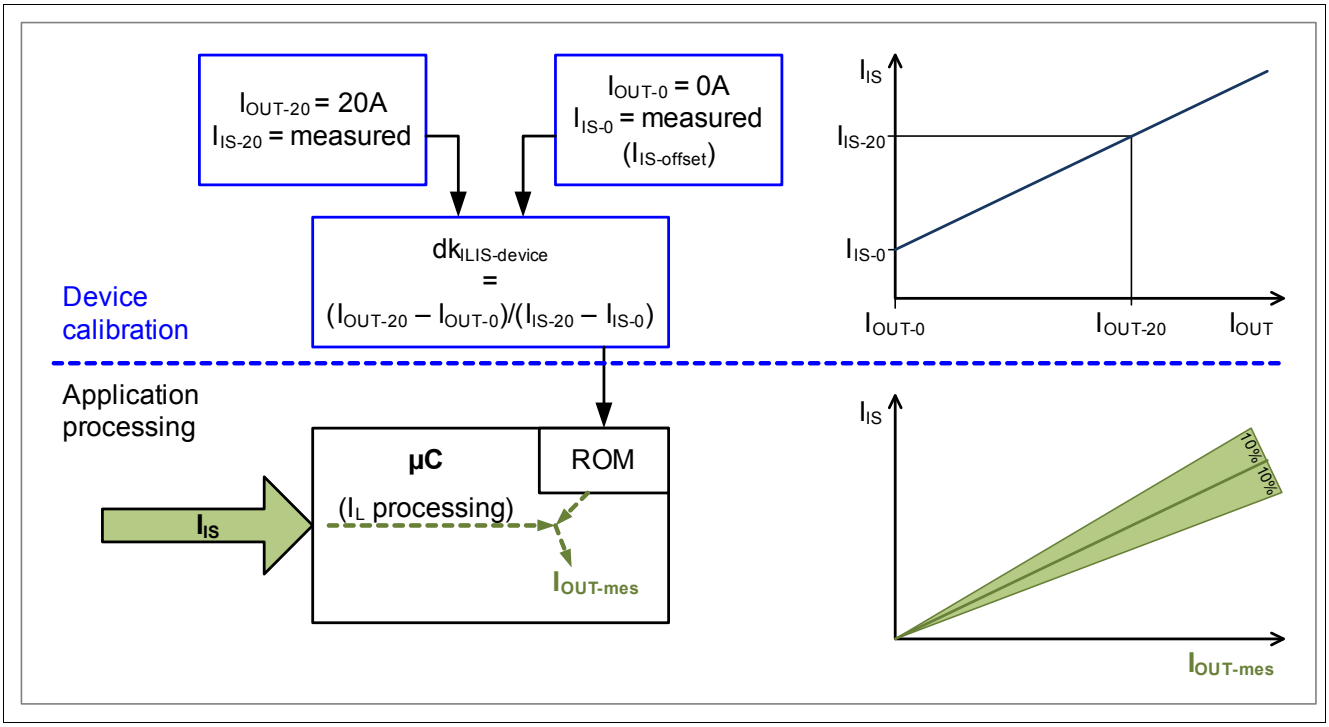

Figure 15 Generating the device fine $dk_{ILIS-device}$

5.4 Device fine dk_{ILIS} and temperature compensation

On the other hand the dk_{ILIS} is dependent on the temperature, which is shown in **Figure 12** and **Figure 13**. These figures show a characteristic temperature drift with a low content of production spread. This makes it possible to measure the temperature on the PCB and reduce the temperature dependency by means of a calculation in the microcontroller. This procedure is illustrated in **Figure 16**.

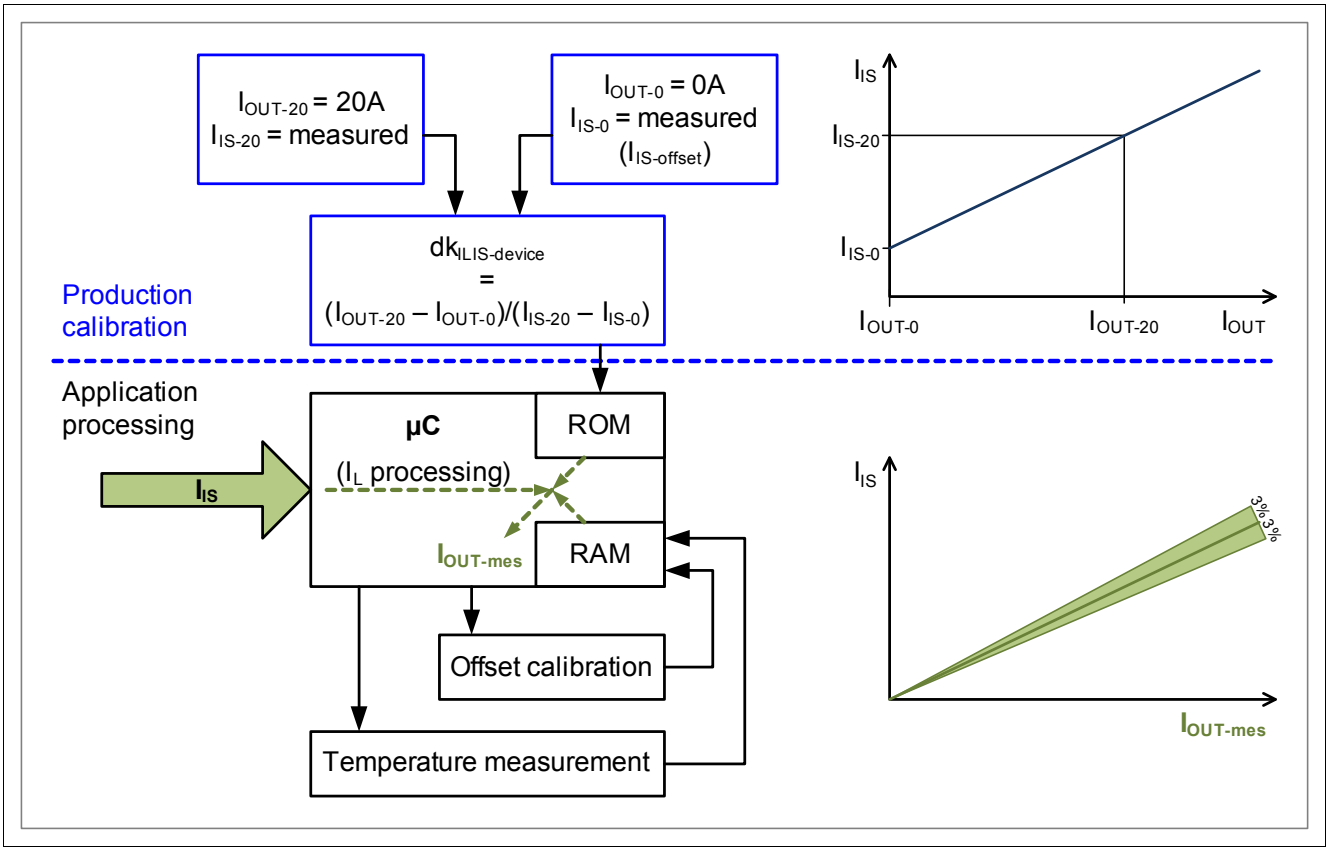

Figure 16 Load current "I_{OUT}" calculation with temperature compensation.

Taking the extreme values from **Figure 13**:

- $dk_{ILIS-max-C}$ = 1.08 (blue @ -40°C)
- $dk_{ILIS-min-C}$ = 1.05 (green @ -40°C)
- $dk_{ILIS-max-H}$ = 0.955 (green @ 150°C)
- $dk_{ILIS-min-H}$ = 0.925 (blue @ 150°C)

Multiplying the min. values with a factor of 0.97 (-3% aging) produces the following values:

- $dk_{ILIS-max-C}$ = 1.08 (blue @ -40°C)
- $dk_{ILIS-min-C-old}$ = 1.0185 (green @ -40°C)
- $dk_{ILIS-max-H}$ = 0.955 (green @ 150°C)
- $dk_{ILIS-min-H-old}$ = 0.9 (blue @ 150°C)

Calculating the typical value for:

- $dk_{ILIS-typ-C}$ = 1.05
- $dk_{ILIS-typ-H}$ = 0.928

These values could be compensated with a temperature measurement and the characteristic from **Figure 12** and **Figure 13** to provide the value of $dk_{ILIS-typ}$ = 1.

With this compensation the new min. and max. values are:

- $dk_{ILIS-max-C-T}$ = 1.03 (blue @ -40°C)
- $dk_{ILIS-min-C-old-T}$ = 0.9685 (green @ -40°C)
- $dk_{ILIS-max-H-T}$ = 1.027 (green @ 150°C)
- $dk_{ILIS-min-H-old-T}$ = 0.972 (blue @ 150°C)

After temperature compensation the min. and max. values are $dk_{ILIS\text{-}min\text{-}H\text{-}old\text{-}T}$ and $dk_{ILIS\text{-}max\text{-}C\text{-}T}$.

Ultimately a current measurement with a precision of ±3% could be achieved!

If higher tolerances are acceptable, the temperature measurement can be less precise.

5.4.1 An example of the I_{IS} failure with a rough temperature estimation

Assuming the dk_{ILIS} was calibrated during production at 25°C the I_{IS} measurement failure could be reduced to ±6%, only by estimating if the temperature is above or below 25°C. This estimation could be done e.g. by using the temperature characteristic of the $I_{IS\text{-}offset}$, which is included in the data sheet.

Temperature below 25°C:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40°C)
- $dk_{ILIS\text{-}min\text{-}25°C}$ = 1

Reducing the min. values with the -3% aging (multiplying with 0.97) the following values will be calculated:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40°C)
- $dk_{ILIS\text{-}min\text{-}25°C\text{-}old}$ = 0.97

For temperatures above 25°C the calculation method is essentially the same.

Ultimately, a current measurement with a precision of ±6% could be achieved without any external temperature measurement!

6 Power dissipation

The device dissipates some power. This power dissipation is generated in the top chip and in the individual MOSFETs. The high currents in the MOSFETs generate most of the power dissipation. The following consideration is based on several assumptions, so the result is ultimately an estimation which should help you understand the general trend.

The power dissipation in the MOSFETs consists mainly of conducted losses and switching losses. Losses in the body diode only occur during the cross current protection phase. They are therefore not taken into consideration.

6.1 Power dissipation of the control chip (top chip)

The control chip consumes a certain amount of current, and this causes power dissipation.

In DC-mode the following equation describes the power dissipation in the control chip:

(16)

$$P_{CC-DC} = (I_{Vs(ON)} + I_{IS}) \cdot V_S$$

In PWM-mode, an additional current is needed to charge/discharge the MOSFET gates. This leads to the following PWM power dissipation:

(17)

$$P_{CC-PWM} = Q_{tot} \cdot V_S \cdot f_{PWM}$$

The gate charges for the BTN89xx are specified in the table below:

Table 2 Q_{tot} of BTN896x and BTN898x

Product	Total gate charge
BTN8960 /62	450 nC
BTN8980 /82	550 nC

Power dissipation in the control chip can be calculated as follows:

(18)

$$P_{CC} = P_{CC-DC} + P_{CC-PWM} = (I_{Vs(ON)} + I_{IS}) \cdot V_S + Q_{tot} \cdot V_S \cdot f_{PWM}$$

6.2 Conduction power dissipation

In the ON-state, a MOSFET has a specific R_{ON} which is listed in the data sheet. R_{ON} is different for the high side (HS) and the low side (LS) MOSFETs. This means that R_{ON} must be selected according to the driving situation. A current flowing through this transistor generates the following conducted losses:

(19)

$$P_{CL} = I^2 \cdot R_{ON}$$

In case the NovalithIC™ is driven in a static condition, **Equation (19)** can be used to estimate the static conducted losses for the high side or low side MOSFET.

6.3 Power dissipation due to switching

With PWM control, switching losses need to be taken into account because they generate most of the power dissipation for high PWM frequencies. The NovalithIC™ devices are designed to drive motors or other inductive loads. This chapter deals with switching losses that are generated while driving an inductive load.

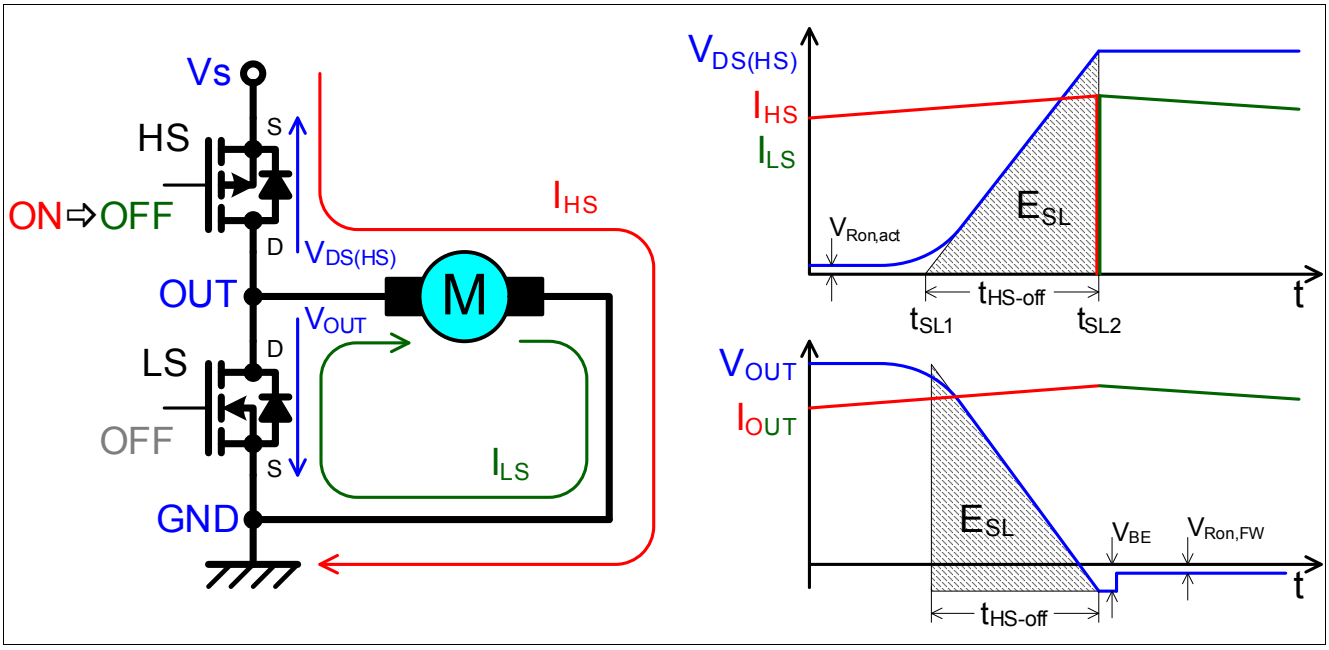

Figure 17 High Side switching scenario of BTN89xy

The current in an inductor cannot be changed abruptly (rule of Lenz). As shown in **Figure 17** the current in the high side (HS) MOSFET is driven by the motor inductance as long as the OUT voltage drops one V_{BE} below GND and the current is flowing through the body diode of the low side (LS) MOSFET. This means that the current I_{HS} is flowing in the high side (HS) MOSFET, even though this is in linear mode during $t_{HS\text{-}off}$.

The NovalithIC™ has a cross-current protection mechanism which ensures that an output MOSFET is turned on only when the other one is off. This causes a free wheeling current through the MOSFET body diode (V_{BE} in **Figure 17**) before the resistive path is switched on. The power dissipation caused by the body diode is negligible and thus not taken into account in this estimation.

The rise- and fall- time in the data sheet is the period during which the output voltage decreases from 80% to 20%. In order to determine the switching losses, we need to determine the time required to decrease the output voltage from 100% to 0%. The $t_{HS\text{-}off}$ can be estimated from the data sheet parameters with the **Equation (20)** accordingly.

(20)

$$t_{HS-off} = \frac{t_{f(HS)}}{0.5}$$

Factor 0.5 is related to ΔV_{OUT} from 0% to 100%

For the other switching times ($t_{HS\text{-}on}$, $t_{LS\text{-}off}$ and $t_{LS\text{-}on}$) **Equation (20)** can be used to perform the same calculation using the corresponding data sheet parameters ($t_{r(HS)}$, $t_{f(LS)}$ and $t_{r(LS)}$).

Other assumptions, with a minor effect on the result, include the following:

- The load current during the switching process is constant.
- V_{OUT} and $V_{DS(HS)}$ have a linear behaviour.
- The switching times are assumed as equal and in the following always referred to as $t_{HS\text{-}off}$.

The switching energy E_{SL} is shown in **Figure 17** and can be estimated using **Equation (21)** below:

(21)

$$E_{SL} = \int_{t_{SL1}}^{t_{SL2}} V_S \cdot I_{OUT} \cdot dt = \frac{V_S \cdot I_{OUT}}{2} \cdot t_{HS-off}$$

From the switching energy E_{SL} the average power loss P_{SL} can be determined with two switching times per PWM period. This is shown in **Equation (22)**:

(22)

$$\overline{P_{SL}} = \frac{V_S \cdot I_{OUT}}{2} \cdot 2 \cdot t_{HS-off} \cdot f_{PWM} = V_S \cdot I_{OUT} \cdot t_{HS-off} \cdot f_{PWM}$$

6.4 Entire power dissipation of the MOSFETs

The average power dissipation in PWM-mode consists of the switching losses plus the conducted losses, as shown in **Figure 18**. We must take into account that the losses occur in the high side (HS) and low side (LS) MOSFET. In the example of **Figure 17**, where the motor is connected to GND, the switching losses occur in the high side (HS) MOSFET. The conducted losses occur in the high side (HS) MOSFET during the ON-phase and in the low side (LS) MOSFET in the free wheeling phase, as shown in **Figure 18**.

In PWM-mode, the PWM-period-time is:

(23)

$$T_{PWM} = \frac{1}{f_{PWM}}$$

The duty cycle (DC) of the PWM-mode is the relation between the ON-time and the PWM-period-time in percent.

(24)

$$DC = \frac{T_{ON}}{T_{PWM}}$$

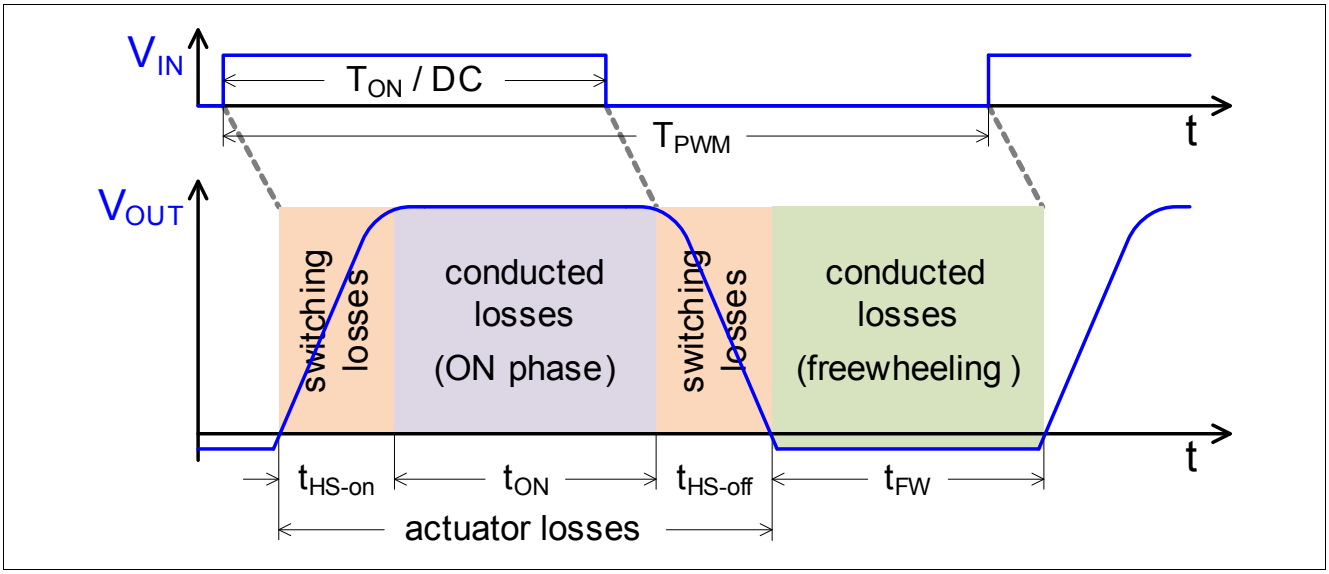

Figure 18 Entire power dissipation of BTN89xy with the motor connected to GND

In **Chapter 6.4.2** and **Chapter 6.4.3** the power dissipation is estimated separately for the high side (HS) and low side (LS) MOSFET.

6.4.1 PWM control and the duty cycle constraints

If t_{FW} is close to or below zero, no freewheeling occurs. V_{OUT} does not go below GND. This means that only switching losses are generated. Thus, a duty cycle generating $t_{FW} \leq 0$ is insufficient to control the motor current and therefore not taken into account in the following calculations. In this case, the high side (HS) MOSFET should be permanently on.

The same is valid for $t_{ON} \leq 0$. In this case, the low side (LS) MOSFET should be permanently on.

Extremely low or high duty cycle values required by real applications can be achieved by increasing the switching speed and/or by increasing T_{PWM}.

6.4.2 Entire power dissipation in the actuator MOSFET

In the motor-to-GND scenario the actuator MOSFET is the high side (HS) MOSFET, as in **Figure 17** and in motor-to-Vs scenario, the actuator MOSFET is the low side (LS) MOSFET. The entire power dissipation consists of two times the switching losses plus the cunducted losses in the ON-phase, as shown in **Figure 18**. The time of the ON-phase in PWM-mode is provided by the following formulae:

(25)

$$t_{ON} = T_{ON} - t_{HS-on}$$

As mentioned in "**Other assumptions**" on **Page 25** switching times are assumed as equal and named as $t_{HS\text{-}off}$:

(26)

$$t_{ON} = T_{ON} - t_{HS-off}$$

Equation for estimate the entire conducted energy in the actuator MOSFET:

(27)

$$E_{act} = 2 \cdot E_{SL} + E_{ON} = V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON,act} \cdot t_{ON}$$

From **Equation (27)** the average power dissipation in the actuator MOSFET can be determined by multiplying **Equation (27)** by f_{PWM}:

(28)

$$\overline{P_{act}} = E_{act} \cdot f_{PWM} = (V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON,act} \cdot t_{ON}) \cdot f_{PWM}$$

Equation (28) is an estimation of the average power dissipation in the actuator MOSFET. In **Figure 17**, this is the high side (HS) MOSFET.

6.4.3 Entire power dissipation in the freewheeling MOSFET

In the motor-to-GND scenario , the freewheeling MOSFET is the low side (LS) MOSFET, as in **Figure 17**, and in the motor-to-Vs scenario the freewheeling MOSFET is the high side (HS) MOSFET. The entire power dissipation consists of the conducted losses in the freewheeling phase, as shown in **Figure 18**. The duration of the freewheeling phase in PWM-mode is provided by the equation below:

(29)

$$t_{FW} = T_{PWM} - T_{ON} - t_{HS-off}$$

Important note: For the proper use of **Equation (29)** refer to **Chapter 6.4.1**.

Equation to determine the entire freewheeling energy in the freewheeling MOSFET:

(30)

$$E_{FW} = I_{OUT}^2 \cdot R_{ON,FW} \cdot t_{FW} = I_{OUT}^2 \cdot R_{ON,FW} \cdot (T_{PWM} - T_{ON} - t_{HS-off})$$

From **Equation (30)** the average power dissipation in the freewheeling MOSFET can be determined by multiplying **Equation (30)** by f_{PWM}:

(31)

$$\overline{P_{FW}} = E_{FW} \cdot f_{PWM} = I_{OUT}^2 \cdot R_{ON,FW} \cdot (T_{PWM} - T_{ON} - t_{HS-off}) \cdot f_{PWM}$$

Equation (31) is an estimation of the average power dissipation in the freewheeling MOSFET. In **Figure 17**, this is the low side (LS) MOSFET.

6.5 Entire power dissipation in the NovalithIC™

To determine the entire power dissipation in the NovalithIC™, combine **Equation (28)**, **Equation (31)** and **Equation (18)**.

(32)

$$\overline{P_{Nova}} = \overline{P_{act}} + \overline{P_{FW}} + P_{CC}$$

Equation (32) is the average of the different power losses in one PWM period, as shown in **Figure 18**, plus the power losses in the control chip.

6.6 Simplifications

Because the losses in the control chip are typically negligible in comparison with the losses in the MOSFETs, they are neglected in this simplification.

Taking into account that the high side (HS) and the low side (LS) MOSFET are in a similar R_{ON} range, the equation for determining the entire power dissipation in the NovalithIC™ can be significantly reduced by using the same R_{ON} for both the high side (HS) and the low side (LS) MOSFET. The more conservative approach is to use the higher R_{ON} of both.
The idea behind this is to have the same R_{ON} for the conducted losses of the ON- and the freewheeling phase, according to **Figure 18**. Due to this simplification the energy in one PWM- period is two times the switching losses E_{SL} and R_{ON} losses during the remaining time:

(33)

$$E_{Nova} = 2 \cdot E_{SL} + P_{CL} \cdot (T_{PWM} - 2 \cdot t_{HS-off})$$

(34)

$$E_{Nova} = 2 \cdot \frac{V_S \cdot I_{OUT}}{2} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON} \cdot (T_{PWM} - 2 \cdot t_{HS-off})$$

From the simplyfied NovalithIC™ energy to the simplyfied NovalithIC™ power dissipation by multiplying **Equation (34)** by f_{PWM}:

(35)

$$\overline{P_{Nova,S}} = (V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON} \cdot (T_{PWM} - 2 \cdot t_{HS-off})) \cdot f_{PWM}$$

7 Revision History

Previous revision: 0.1, 2012-07-09

Revision	Date	Changes
0.2	2013-01-16	**Page 4** - **Chapter 2**: Added benefits. **Page 4** - **Figure 2**; **Page 5** - **Figure 3**; **Page 9** - **Other components:**Changed resistor name from R_1 to R_3 and C_{IS}-value to 1nF and C_{IS}-text. **Page 11**: Updated **Figure 7**. **Page 4** - **Figure 2**, **Page 5** - **Figure 3**: Update value of C1. **Page 9** - **Figure 6**: Update footnote of figure. **Page 17**: New **Chapter 5**.
0.3	2014-08-29	**Page 14** - **Chapter 4.3**: Added. **Page 15** - **Chapter 4.5**: Text update. **Page 24** - **Chapter 6**: Added. **Chapter 2**: Updated application circuits (C1 and DC-link)

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