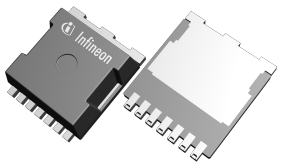
BTN9960LV

Datasheet

MOTIX™ single half-bridge with integrated driver IC

Features

- AEC-Q100/Q006 qualified (Grade 1)
- Supply voltage range 8 V - 18 V (max up to 40 V)
- Path resistance of typ. 9.7 mΩ @ 25°C (max. 18.1 mΩ @ 150°C)
- Low quiescent current of max. 3.3 µA @ 85°C
- Protection features: overcurrent, undervoltage, overtemperature
- Overcurrent detection level of 35 A min
- Eight selectable switching slew rates for optimized EME
- Status flag diagnosis with feedback of current sense, temperature and slew rate



AEC Qualified RoHS

Potential applications

- Automotive 12 V brushed DC Motor
- Fuel, washer pump

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The BTN9960LV is an integrated high current half-bridge for motor drive applications. It is part of the MOTIX™ single half-bridge product family containing one p-channel high-side MOSFET and one n-channel low-side MOSFET with an integrated driver IC in one package. Due to the p-channel high-side switch the need for a charge pump is eliminated thus minimizing EME. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit.

The BTN9960LV provides a cost optimized solution for protected high current PWM motor drives with very low board space consumption.

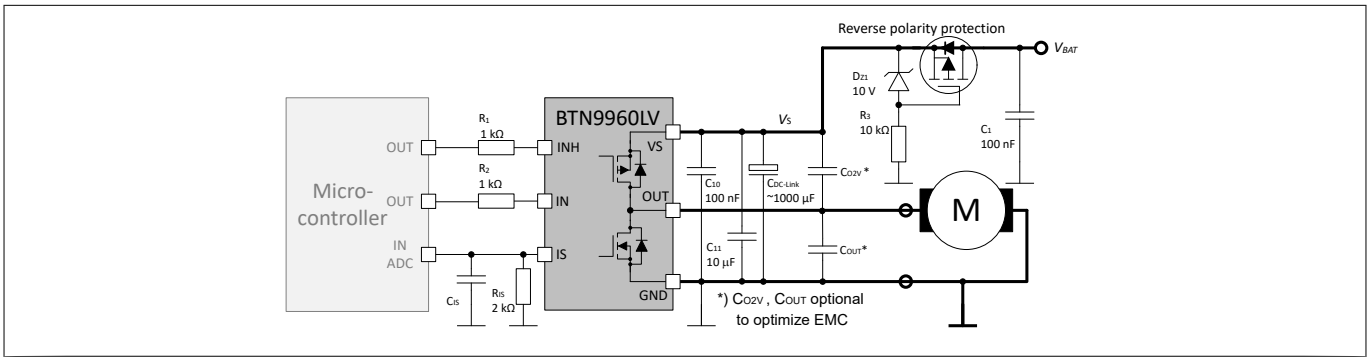


Figure 1 Typical application

Type	Package	Marking
BTN9960LV	PG-HSOF-7-1 (sTOLL)	BTN9960

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1 Block diagram

The BTN9960LV contains three separate chips in one package: one p-channel high-side MOSFET and one n-channel low-side MOSFET together with a driver IC, forming an integrated high current half-bridge. All three chips are mounted on a common lead frame, using the chip-on-chip and chip-by-chip technology. The power switches utilize vertical MOS technologies to ensure optimum ON-state resistance. Due to the p-channel high-side switch the need for a charge pump is eliminated thus minimizing EME. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, overcurrent, undervoltage and short circuit. The BTN9960LV can be combined with other BTN9960LVs to form an H-bridge or a 3-phase drive configuration.

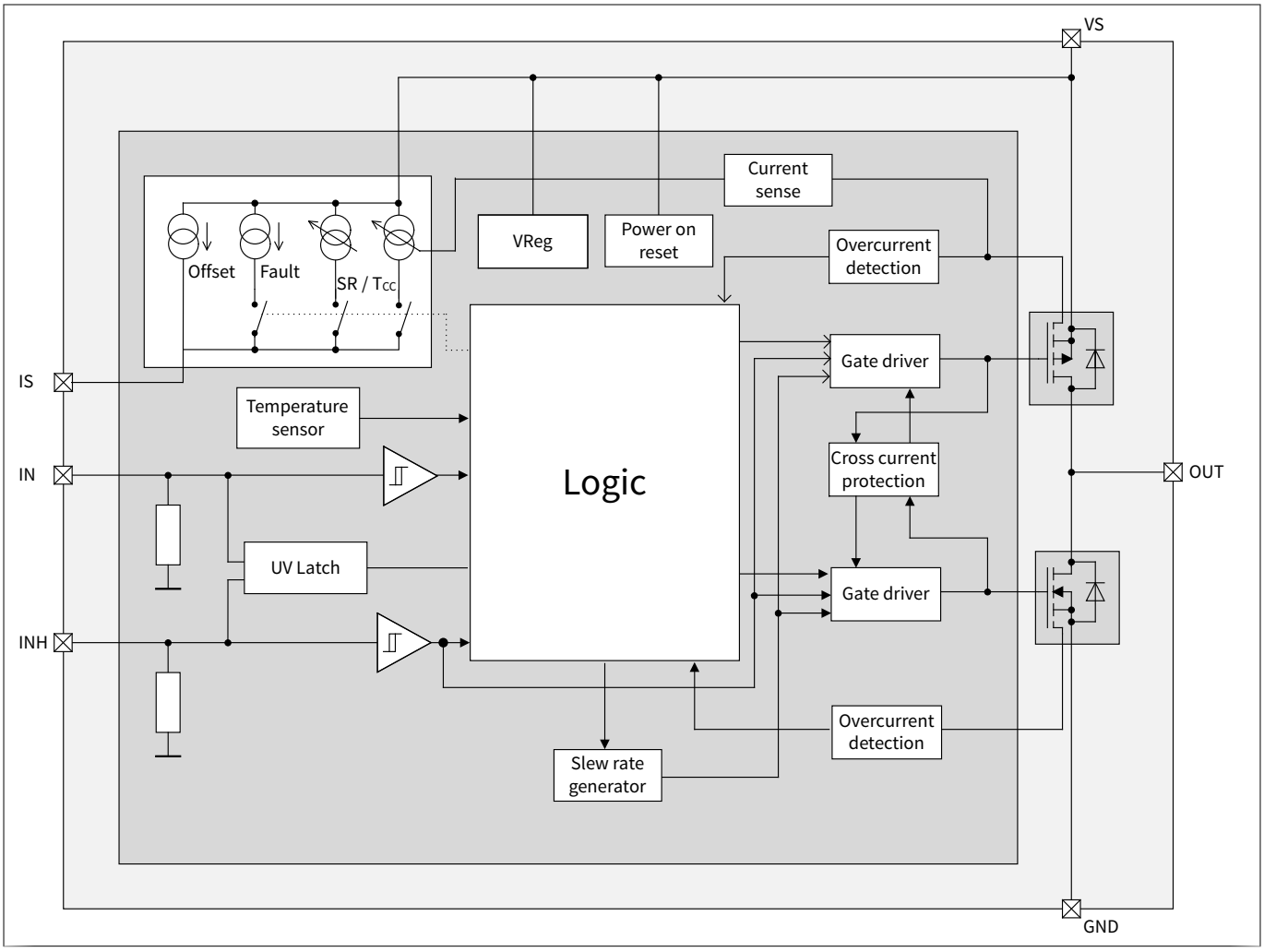

Figure 2 Block diagram

Following figure shows the terms used in this datasheet.

1 Block diagram

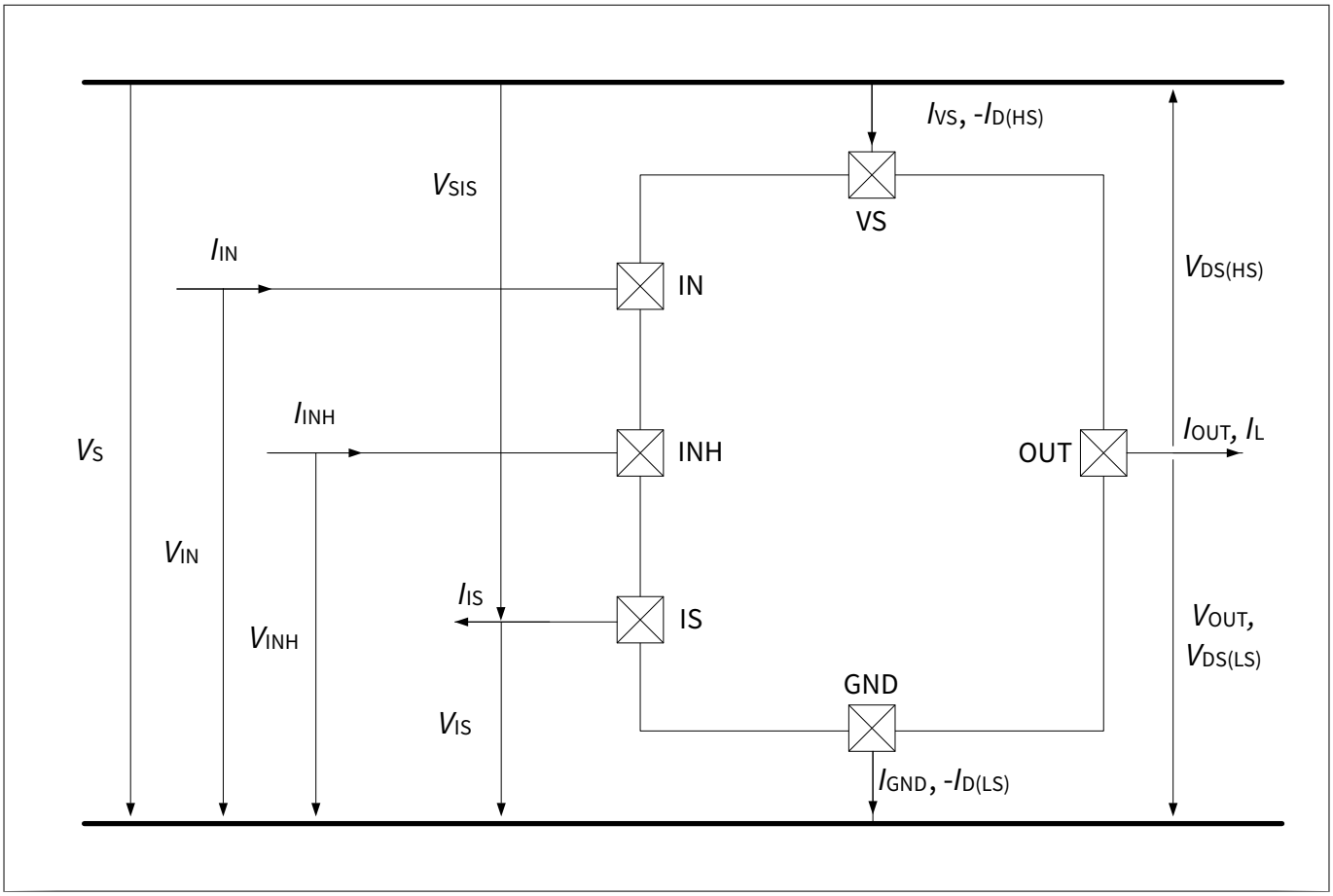

Figure 3 Terms

2 Pin configuration

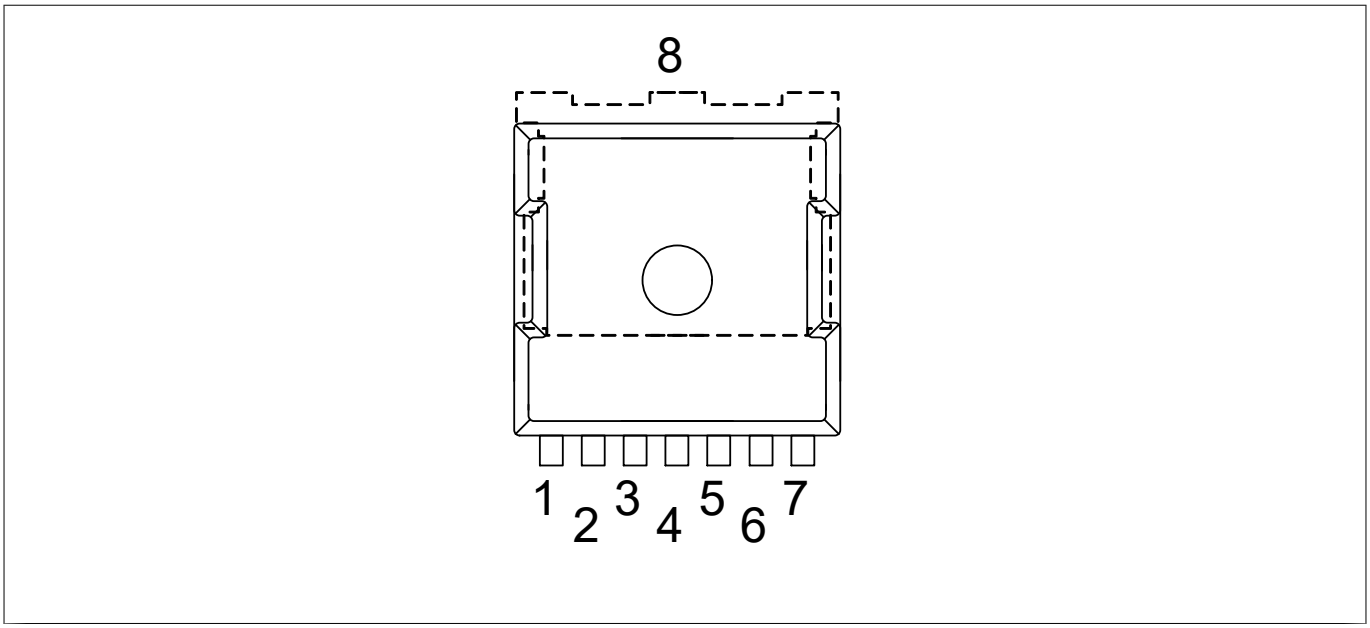

Figure 4 Pin assignment BTN9960LV (top view)

Table 1 Pin definitions and functions

Pin	Symbol	I/O	Function
1,2	**GND**	**–**	**Ground** (1)
3	IN	I	Input Defines whether high- or low-side switch is activated. An internal pull down resistor is connected to this pin.
4	INH	I	Inhibit When set to low device goes in tristate. An internal pull down resistor is connected to this pin.
5	IS	O	Current sense, temperature sense, slew rate level and diagnostics
6,7	**VS**	**–**	**Supply** (1)
8 (EP)	**OUT**	**O**	**Power output of the bridge**

1) All terminal pins must be connected together on the PCB. All terminal pins are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow

Bold type: pin needs power wiring

3 General product characteristics

The device is intended to be used in an automotive environment. The circumstances, how the device environment must look like, are described in this chapter.

3.1 Absolute maximum ratings

Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) [1)]

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltages						
Supply voltage	V_S	-0.3	–	40	V	–
Drain-source voltage high-side	$V_{DS(HS)}$	-40	–	–	V	$T_j \geq 25°C$
Drain-source voltage high-side	$V_{DS(HS)}$	-38	–	–	V	$T_j < 25°C$
Drain-source voltage low-side	$V_{DS(LS)}$	–	–	40	V	$T_j \geq 25°C$
Drain-source voltage low-side	$V_{DS(LS)}$	–	–	38	V	$T_j < 25°C$
Logic input voltage	V_{IN} V_{INH}	-0.3	–	5.5	V	–
Voltage between VS and IS pin	V_{SIS}	-0.3	–	40	V	–
Voltage at IS pin	V_{IS}	-0.3	–	40	V	–
Currents						
HS drain current	$\lvert I_{D(HS)} \rvert$	–	–	I_{OCH0}	A	Switch active [2)]
LS drain current	$\lvert I_{D(LS)} \rvert$	–	–	I_{OCL0}	A	Switch active [2)]
Temperatures						
Junction temperature	T_j	-40	–	150	°C	–
Storage temperature	T_{stg}	-55	–	150	°C	–
ESD susceptibility						
ESD robustness all pins (HBM)	$\lvert V_{ESD(HBM,local)} \rvert$	–	–	2	kV	HBM [3)]
ESD robustness OUT vs GND vs VS (HBM)	$\lvert V_{ESD(HBM,global)} \rvert$	–	–	6	kV	HBM [3)]
ESD robustness all pins (CDM)	$\lvert V_{ESD(CDM)} \rvert$	–	–	500	TC	CDM [4)]
ESD robustness corner pins (CDM) (pins VS, GND, OUT)	$\lvert V_{ESD(CDM,corner)} \rvert$	–	–	750	TC	CDM [4)]

1) Not subject to production test, specified by design.
2) Maximum applicable single pulse current depends on t_{pulse}. See figure maximum single pulse current.
3) Human body model “HBM” robustness: class 2 according to AEC-Q100-002.

4) Charged device model “CDM” robustness: class C2a according to AEC-Q100-011 Rev D. “TC” corresponds to “test condition” according to AEC-Q100-011.

Latchup Robustness: class II according to AEC-Q100-04

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

The parameters of the functional range are listed in the following table:

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage range for normal operation	$V_{S(nor)}$	8	–	18	V	1)
Extended supply voltage range for operation	$V_{S(ext)}$	4.5	–	40	V	Falling $V_{S(ext)}$ Parameter deviation possible 1)
Junction temperature	T_j	-40	–	150	°C	1)

1) Not subject to production test, specified by design.

3.3 Thermal resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to https://www.jedec.org/

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction-case, high-side switch Rthjc (HS) = ΔTj(HS)/Pv(HS)	$R_{thJC(HS)}$	–	0.5	0.7	K/W	1)
Thermal resistance junction-case, low-side switch Rthjc(LS) = ΔTj(LS)/Pv(LS)	$R_{thJC(LS)}$	–	0.8	1.1	K/W	1)
Thermal resistance junction-ambient	R_{thJA}	–	19	–	K/W	1) 2)

1) Not subject to production test, specified by design.
2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The device (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3 General product characteristics

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

4 Block description and characteristics

4.1 Supply characteristics

Table 5 Supply characteristics

V_S = 8 V to 18 V, T_j = -40°C to 150°C, I_L = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
General						
Supply current	$I_{VS(on)}$	–	2.3	4.5	mA	V_{INH} = 5 V V_{IN} = 0 V or 5 V normal operation DC-mode (no fault condition) according to Table 12
Supply current in SR selection mode	$I_{VS(on\_SR)}$	–	2.0	3.2	mA	V_{INH} = 0 V V_{IN} = 5 V SR selection mode $I_{VS(on\_SR)} = I_{VS} - I_{IS}$ (no fault condition)
Quiescent current Tj = 150°C	$I_{VS(off)\_150C}$	–	–	75	µA	$V_{INH} = V_{IN}$ = 0 V T_j = 150°C
Quiescent current at Tj ≤ 85°C	$I_{VS(off)\_85C}$	–	–	5	µA	$V_{INH} = V_{IN}$ = 0 V $T_j \leq$ 85°C [1]
Quiescent current Tj ≤ 85°C and VS = 13.5 V	$I_{VS(off)\_85C\_13.5V}$	–	–	3.3	µA	$V_{INH} = V_{IN}$ = 0 V VS = 13.5 V $T_j \leq$ 85°C [1]

1) Not subject to production test, specified by design.

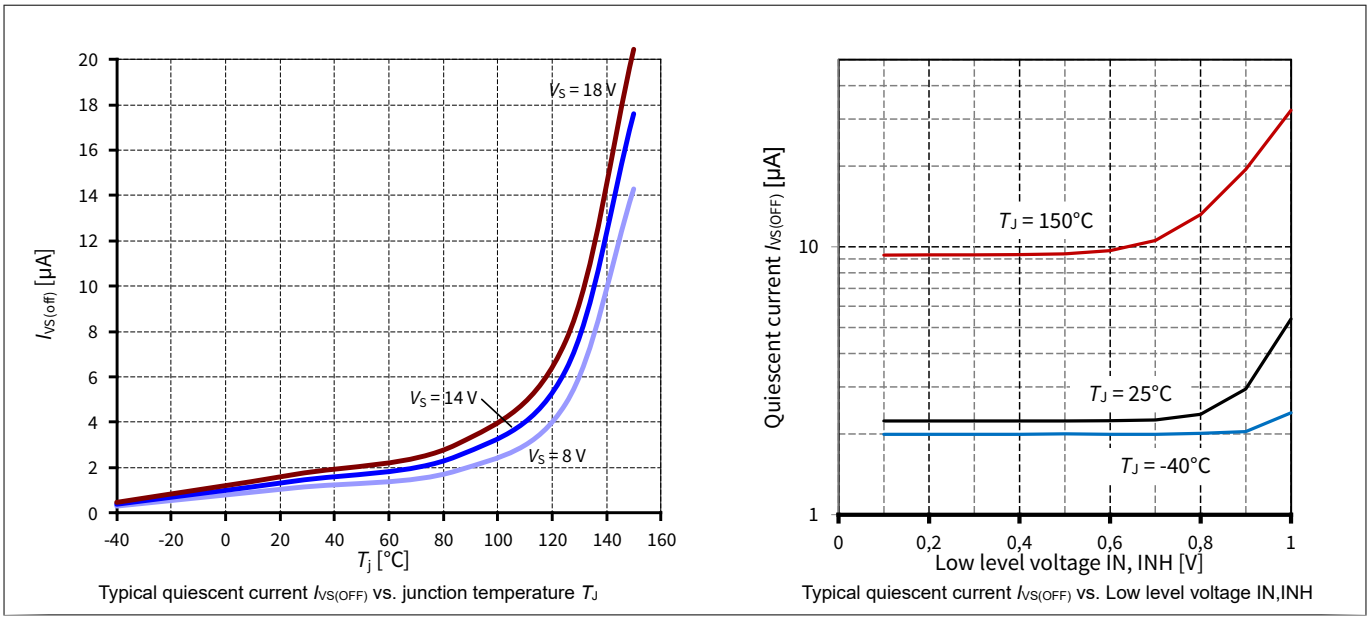

Figure 5 Typical quiescent current $I_{VS(OFF)}$ characteristics

4.2 Power stages

The power stages of the BTN9960LV consist of a p-channel vertical DMOS transistor for the high-side switch and a n-channel vertical DMOS transistor for the low-side switch. All protection and diagnostic functions are located in a separate driver IC. Both switches allow active freewheeling and thus minimizing power dissipation during PWM control.

The ON-state resistance R_{ON} is dependent on the supply voltage V_S as well as on the junction temperature T_j. The typical ON-state resistance characteristics are shown in Figure 6.

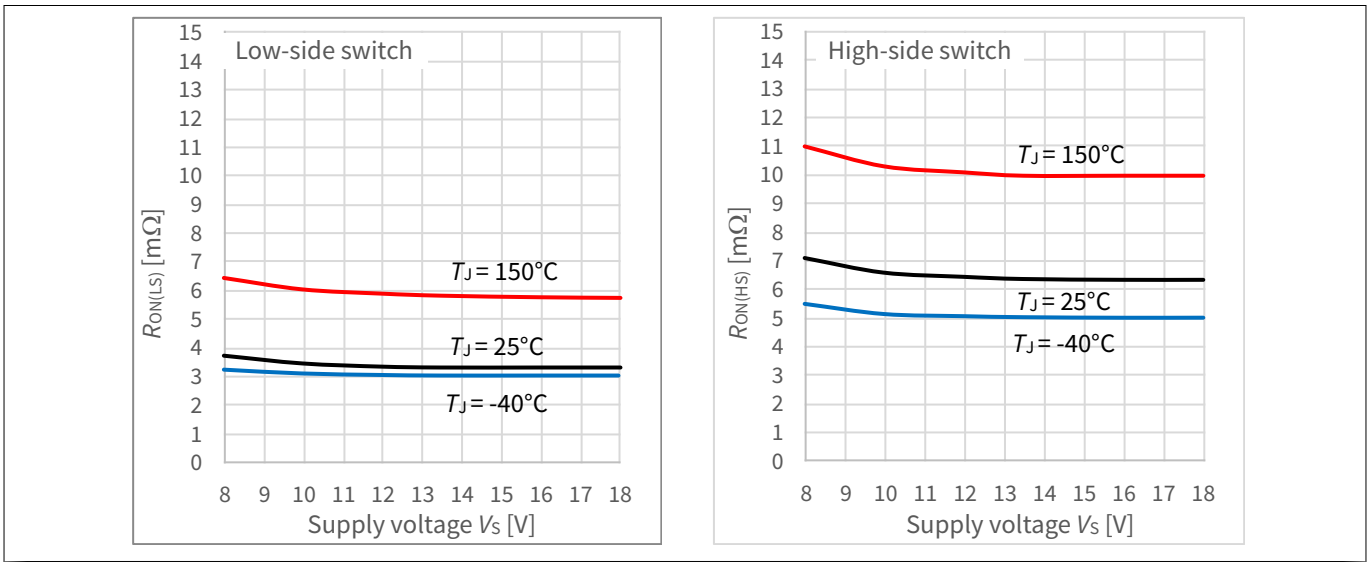

Figure 6 Typical ON-state resistance vs. supply voltage V_S

4.2.1 Electrical characteristics – power stages – static

Table 6 Electrical characteristics – power stages – static

V_S = 8 V to 18 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-side switch – static characteristics						
ON-state high-side resistance	$R_{ON(HS)}$	–	6.3	–	mΩ	I_{OUT} = 15 A; V_S = 13.5 V T_j = 25°C [1]
ON-state high-side resistance	$R_{ON(HS)}$	–	9.0	11.8	mΩ	I_{OUT} = 15 A; V_S = 13.5 V T_j = 150°C
ON-state high-side resistance	$R_{ON(HS)}$	–	9.5	–	mΩ	I_{OUT} = 15 A; V_S = 6 V T_j = 25°C [1]
ON-state high-side resistance	$R_{ON(HS)}$	–	13.5	16.7	mΩ	I_{OUT} = 15 A; V_S = 6 V T_j = 150°C
Leakage current high-side	$I_{L(LKHS)}$	–	–	1	µA	V_{INH} = V_{IN} = 0 V; V_{OUT} = 0 V $T_j \leq$ 85°C [1]
Leakage current high-side	$I_{L(LKHS)}$	–	–	60	µA	V_{INH} = V_{IN} = 0 V; V_{OUT} = 0 V T_j = 150°C
Reverse diode forward-voltage high-side	$V_{DS(HS)}$	–	0.9	–	V	I_{OUT} = -15 A T_j = -40°C [1] [2]
Reverse diode forward-voltage high-side	$V_{DS(HS)}$	–	0.85	–	V	I_{OUT} = -15 A T_j = 25°C [1] [2]
Reverse diode forward-voltage high-side	$V_{DS(HS)}$	–	0.7	0.9	V	I_{OUT} = -15 A T_j = 150°C [2]
Low-side switch – static characteristics						
ON-state low-side resistance	$R_{ON(LS)}$	–	3.4	–	mΩ	I_{OUT} = -15 A; V_S = 13.5 V T_j = 25°C [1]
ON-state low-side resistance	$R_{ON(LS)}$	–	5.7	6.3	mΩ	I_{OUT} = -15 A; V_S = 13.5 V T_j = 150°C
ON-state low-side resistance	$R_{ON(LS)}$	–	5.1	–	mΩ	I_{OUT} = -15 A; V_S = 6 V T_j = 25°C [1]
ON-state low-side resistance	$R_{ON(LS)}$	–	8.6	10.2	mΩ	I_{OUT} = -15 A; V_S = 6 V T_j = 150°C
Leakage current low-side	$I_{L(LKLS)}$	–	–	1	µA	V_{INH} = V_{IN} = 0 V; V_{OUT} = V_S $T_j \leq$ 85°C [1]
Leakage current low-side	$I_{L(LKLS)}$	–	–	30	µA	V_{INH} = V_{IN} = 0 V; V_{OUT} = V_S T_j = 150°C

(table continues...)

Table 6 (continued) Electrical characteristics – power stages – static

V_S = 8 V to 18 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Reverse diode forward-voltage low-side	$-V_{DS(LS)}$	–	0.9	–	V	I_{OUT} = 15 A T_j = -40°C 1) 2)
Reverse diode forward-voltage low-side	$-V_{DS(LS)}$	–	0.8	–	V	I_{OUT} = 15 A T_j = 25°C 1) 2)
Reverse diode forward-voltage low-side	$-V_{DS(LS)}$	–	0.6	0.8	V	I_{OUT} = 15 A T_j = 150°C 2)

1) Not subject to production test, specified by design.
2) Due to active freewheeling, diode is conducting only for a few µs, depending on the selected slew rate SRx.

4.2.2 Switching times

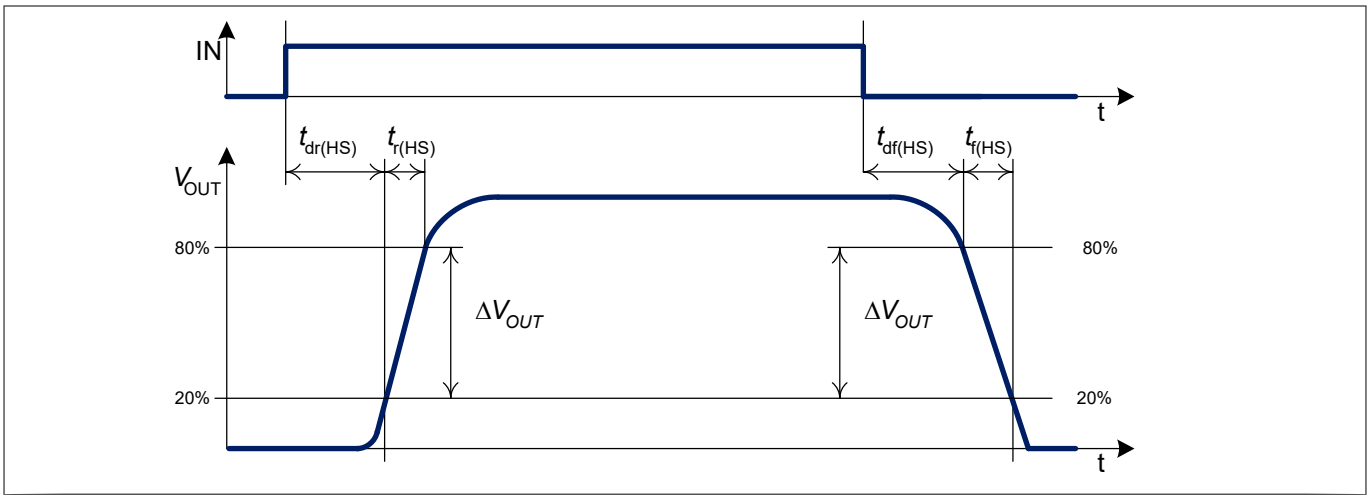

Figure 7 Definition of switching times high-side (R_{load} to GND)

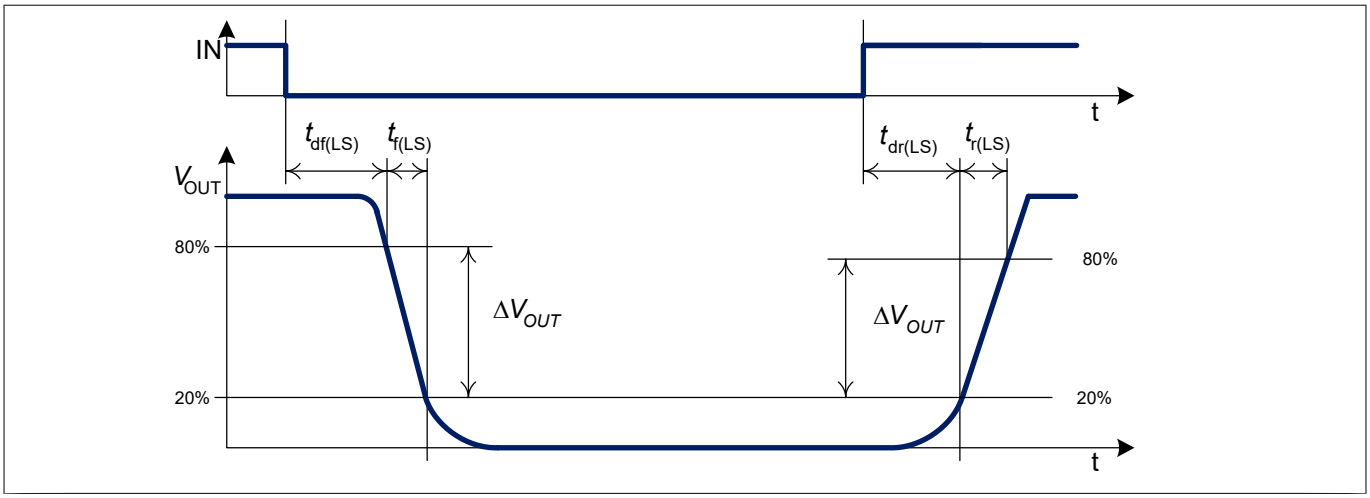

Figure 8 Definition of switching times low-side (R_{load} to V_S)

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse. It can be calculated using the following formulas for $\Delta t_{xS} = t_{IN} - t_{OUT}$:

- $\Delta t_{HS} = (t_{dr(HS)} + 0.5\ t_{r(HS)}) - (t_{df(HS)} + 0.5\ t_{f(HS)})$
- $\Delta t_{LS} = (t_{df(LS)} + 0.5\ t_{f(LS)}) - (t_{dr(LS)} + 0.5\ t_{r(LS)})$

One of 8 different slew rates (SR) can be selected as described in Chapter 4.4.2.

After waking up from stand-by mode, the slew rate level SR0 is selected.

4.2.2.1 Electrical characteristics – power stages – dynamic

Table 7 Electrical characteristics – power stages – dynamic

Paragraph condition: V_S = 13.5 V, T_j = -40°C to 150°C, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse, I_{OUT} > 90 mA freewheeling, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-side switch – dynamic characteristics						
Rise-time of HS for SR0	$t_{r(HS),SR0}$	0.05	0.25	0.55	µs	SR-level = SR0
Rise-time of HS for SR1	$t_{r(HS),SR1}$	–	0.36	–	µs	SR-level = SR1
Rise-time of HS for SR2	$t_{r(HS),SR2}$	–	0.5	–	µs	SR-level = SR2
Rise-time of HS for SR3	$t_{r(HS),SR3}$	–	0.83	–	µs	SR-level = SR3
Rise-time of HS for SR4	$t_{r(HS),SR4}$	–	1.0	–	µs	SR-level = SR4
Rise-time of HS for SR5	$t_{r(HS),SR5}$	0.22	1.25	5.00	µs	SR-level = SR5
Rise-time of HS for SR6	$t_{r(HS),SR6}$	–	2.5	–	µs	SR-level = SR6
Rise-time of HS for SR7	$t_{r(HS),SR7}$	–	5.0	–	µs	SR-level = SR7
Switch-ON delay time HS for SR0	$t_{dr(HS),SR0}$	2.4	3.6	4.4	µs	SR-level = SR0
Switch-ON delay time HS for SR1	$t_{dr(HS),SR1}$	–	4.1	–	µs	SR-level = SR1

(table continues...)

Table 7 (continued) Electrical characteristics – power stages – dynamic

Paragraph condition: V_S = 13.5 V, T_j = -40°C to 150°C, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse, I_{OUT} > 90 mA freewheeling, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Switch-ON delay time HS for SR2	$t_{dr(HS),SR2}$	–	4.6	–	µs	SR-level = SR2
Switch-ON delay time HS for SR3	$t_{dr(HS),SR3}$	–	5.9	–	µs	SR-level = SR3
Switch-ON delay time HS for SR4	$t_{dr(HS),SR4}$	–	6.8	–	µs	SR-level = SR4
Switch-ON delay time HS for SR5	$t_{dr(HS),SR5}$	4.6	8	11.2	µs	SR-level = SR5
Switch-ON delay time HS for SR6	$t_{dr(HS),SR6}$	–	13.2	–	µs	SR-level = SR6
Switch-ON delay time HS for SR7	$t_{dr(HS),SR7}$	–	23.3	–	µs	SR-level = SR7
Fall-time of HS for SR0	$t_{f(HS),SR0}$	0.05	0.25	0.55	µs	SR-level = SR0
Fall-time of HS for SR1	$t_{f(HS),SR1}$	–	0.36	–	µs	SR-level = SR1
Fall-time of HS for SR2	$t_{f(HS),SR2}$	–	0.5	–	µs	SR-level = SR2
Fall-time of HS for SR3	$t_{f(HS),SR3}$	–	0.83	–	µs	SR-level = SR3
Fall-time of HS for SR4	$t_{f(HS),SR4}$	–	1.0	–	µs	SR-level = SR4
Fall-time of HS for SR5	$t_{f(HS),SR5}$	0.22	1.25	5.00	µs	SR-level = SR5
Fall-time of HS for SR6	$t_{f(HS),SR6}$	–	2.5	–	µs	SR-level = SR6
Fall-time of HS for SR7	$t_{f(HS),SR7}$	–	5.0	–	µs	SR-level = SR7
Switch-OFF delay time HS for SR0	$t_{df(HS),SR0}$	1.8	2.5	4.2	µs	SR-level = SR0
Switch-OFF delay time HS for SR1	$t_{df(HS),SR1}$	–	2.8	–	µs	SR-level = SR1
Switch-OFF delay time HS for SR2	$t_{df(HS),SR2}$	–	3.1	–	µs	SR-level = SR2
Switch-OFF delay time HS for SR3	$t_{df(HS),SR3}$	–	3.9	–	µs	SR-level = SR3
Switch-OFF delay time HS for SR4	$t_{df(HS),SR4}$	–	4.4	–	µs	SR-level = SR4
Switch-OFF delay time HS for SR5	$t_{df(HS),SR5}$	3.4	5.0	9.0	µs	SR-level = SR5
Switch-OFF delay time HS for SR6	$t_{df(HS),SR6}$	–	8.1	–	µs	SR-level = SR6

(table continues...)

Table 7 (continued) Electrical characteristics – power stages – dynamic

Paragraph condition: V_S = 13.5 V, T_j = -40°C to 150°C, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse, I_{OUT} > 90 mA freewheeling, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Switch-OFF delay time HS for SR7	$t_{df(HS),SR7}$	–	14.0	–	µs	SR-level = SR7
Low-side switch – dynamic characteristics						
Rise-time of LS for SR0	$t_{r(LS),SR0}$	0.05	0.25	0.55	µs	SR-level = SR0
Rise-time of LS for SR1	$t_{r(LS),SR1}$	–	0.36	–	µs	SR-level = SR1
Rise-time of LS for SR2	$t_{r(LS),SR2}$	–	0.5	–	µs	SR-level = SR2
Rise-time of LS for SR3	$t_{r(LS),SR3}$	–	0.83	–	µs	SR-level = SR3
Rise-time of LS for SR4	$t_{r(LS),SR4}$	–	1.0	–	µs	SR-level = SR4
Rise-time of LS for SR5	$t_{r(LS),SR5}$	0.22	1.25	5.00	µs	SR-level = SR5
Rise-time of LS for SR6	$t_{r(LS),SR6}$	–	2.5	–	µs	SR-level = SR6
Rise-time of LS for SR7	$t_{r(LS),SR7}$	–	5.0	–	µs	SR-level = SR7
Switch-ON delay time LS for SR0	$t_{df(LS),SR0}$	2.6	3.6	5.4	µs	SR-level = SR0
Switch-ON delay time LS for SR1	$t_{df(LS),SR1}$	–	4.1	–	µs	SR-level = SR1
Switch-ON delay time LS for SR2	$t_{df(LS),SR2}$	–	4.6	–	µs	SR-level = SR2
Switch-ON delay time LS for SR3	$t_{df(LS),SR3}$	–	5.9	–	µs	SR-level = SR3
Switch-ON delay time LS for SR4	$t_{df(LS),SR4}$	–	6.8	–	µs	SR-level = SR4
Switch-ON delay time LS for SR5	$t_{df(LS),SR5}$	6.4	8.0	12.7	µs	SR-level = SR5
Switch-ON delay time LS for SR6	$t_{df(LS),SR6}$	–	13.2	–	µs	SR-level = SR6
Switch-ON delay time LS for SR7	$t_{df(LS),SR7}$	–	23.3	–	µs	SR-level = SR7
Fall-time of LS for SR0	$t_{f(LS),SR0}$	0.05	0.25	0.55	µs	SR-level = SR0
Fall-time of LS for SR1	$t_{f(LS),SR1}$	–	0.36	–	µs	SR-level = SR1
Fall-time of LS for SR2	$t_{f(LS),SR2}$	–	0.5	–	µs	SR-level = SR2
Fall-time of LS for SR3	$t_{f(LS),SR3}$	–	0.83	–	µs	SR-level = SR3
Fall-time of LS for SR4	$t_{f(LS),SR4}$	–	1.0	–	µs	SR-level = SR4
Fall-time of LS for SR5	$t_{f(LS),SR5}$	0.22	1.25	5.00	µs	SR-level = SR5

(table continues...)

Table 7 (continued) Electrical characteristics – power stages – dynamic

Paragraph condition: V_S = 13.5 V, T_j = -40°C to 150°C, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse, I_{OUT} > 90 mA freewheeling, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall-time of LS for SR6	$t_{f(LS),SR6}$	–	2.5	–	µs	SR-level = SR6
Fall-time of LS for SR7	$t_{f(LS),SR7}$	–	5.0	–	µs	SR-level = SR7
Switch-OFF delay time LS for SR0	$t_{df(LS),SR0}$	1.5	2.5	3.3	µs	SR-level = SR0
Switch-OFF delay time LS for SR1	$t_{dr(LS),SR1}$	–	2.8	–	µs	SR-level = SR1
Switch-OFF delay time LS for SR2	$t_{dr(LS),SR2}$	–	3.1	–	µs	SR-level = SR2
Switch-OFF delay time LS for SR3	$t_{dr(LS),SR3}$	–	3.9	–	µs	SR-level = SR3
Switch-OFF delay time LS for SR4	$t_{dr(LS),SR4}$	–	4.4	–	µs	SR-level = SR4
Switch-OFF delay time LS for SR5	$t_{dr(LS),SR5}$	2.8	5.0	6.4	µs	SR-level = SR5
Switch-OFF delay time LS for SR6	$t_{dr(LS),SR6}$	–	8.1	–	µs	SR-level = SR6
Switch-OFF delay time LS for SR7	$t_{dr(LS),SR7}$	–	14.0	–	µs	SR-level = SR7

4.3 Protection functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range.

Protection functions are not designed to be used for continuous or repetitive operation, with the exception of the overcurrent protection (Chapter 4.3.3) and undervoltage shutdown (Chapter 4.3.1).

Undervoltage, overtemperature and overcurrent events are indicated by a fault current $I_{IS(fault)}$ at the IS pin as described in Chapter 4.4.3.

The protection functions of the BTN9960LV are prioritized in the following way:

Table 8 Protection functions priorities

Priority	Function	Reference
0 (highest)	Undervoltage shutdown	Chapter 4.3.1
1	Overtemperature protection	Chapter 4.3.2
2	Overcurrent protection	Chapter 4.3.3
3	Stand-by mode	The device only goes into stand-by mode if no fault is present

4.3.1 Undervoltage shutdown with restart

To avoid uncontrolled motion of the driven motor at low voltages the device switches off (output is tri-state), if the supply voltage drops below the switch-OFF voltage $V_{UV(OFF)}$.

If a slew rate level SR0 to SR4 is selected, the device will switch off with the selected slew rate in case of an undervoltage detection. For slew rate level SR5 to SR7, the device will switch off with slew rate level SR4 instead.

As soon as the supply voltage VS rises above the switch-ON voltage $V_{UV(ON)}$, with a hysteresis of $V_{UV(HY)}$, the output channel of the device follows the IN pin again.

The restart is delayed with a time t_{UVD} which protects the device in case the undervoltage condition is caused by a short circuit event (according to AEC-Q100-012).

After power-up, the device is starting without waiting for the delay time t_{UVD}.

The slew rate level and the undervoltage event are stored in analog latches, which are supplied by the INH or/and IN pin. Thus at least one of the two pins always shall be set high during this undervoltage event, until the presence of the $I_{IS(fault)}$ current, to keep the previously set slew rate level after the undervoltage shutdown.

In the case of both INH and IN being 0 during an undervoltage event, a power on reset is performed.

In case of an undervoltage event, the fault current $I_{IS(fault)}$ is provided at the IS pin, once the supply voltage rises above $V_{UV(ON)}$ again.

The fault signal at the IS pin is reset after t_{UVD} after the supply voltage rises above $V_{UV(ON)}$. This behavior is shown in Figure 9.

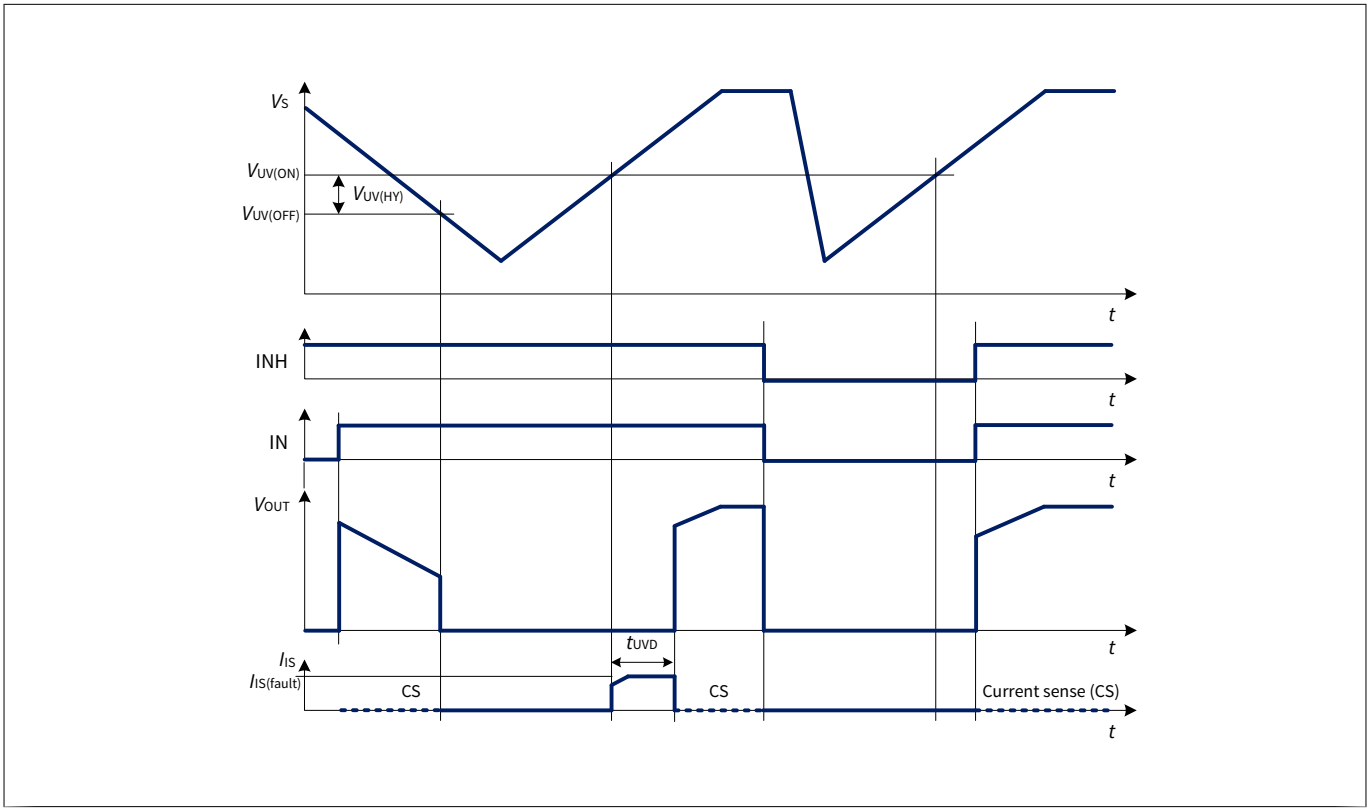

Figure 9 Timing diagram for undervoltage behavior for load to GND

4.3.2 Overtemperature protection

The device is protected against overtemperature by an integrated temperature sensor. Overtemperature leads to a shutdown of the output stage (both the high-side and low-side switch).

This state is latched until the device is reset by a low signal with a minimum length of t_{reset} at the INH and IN pin, provided that its temperature has decreased at least the thermal hysteresis ΔT in the meantime.

If a slew rate level SR0 to SR4 is selected, the device will switch off with the selected slew rate in case of overtemperature. For slew rate level SR5 to SR7, the device will switch off with slew rate level SR4 instead.

4.3.3 Overcurrent protection

The current in the bridge is measured in both switches.

As soon as the current in forward direction in one switch (high-side or low-side) is reaching the limit I_{OCx}, the device goes either into current limitation mode or switches off with latch, depending on the selected SR-level. The corresponding dependencies are described in Table 9.

Table 9 Slew rate dependent overcurrent strategies

SR-level	Mode	Note
SR0	Current limitation (retry)	For details see Chapter 4.3.3.1
SR1		
SR2		
SR3		
SR4		
SR5	Switch-OFF with latch	Requiring reset of the fault latch For details see Chapter 4.3.3.2
SR6		
SR7		

4.3.3.1 Current limitation

If this mode is selected according to Table 9 and the current in forward direction in one switch (high-side or low-side) has reached the limit I_{OCx}, the affected switch is deactivated and the other switch is activated for t_{CLS}. During that time all changes at the IN pin are ignored.

However, during current limitation, the INH pin can still be used to switch both MOSFETs off.

After t_{CLS} the switches follow the IN pin again.

The fault signal at the IS pin is reset after 1.5 * t_{CLS}. This behavior is shown in Figure 10.

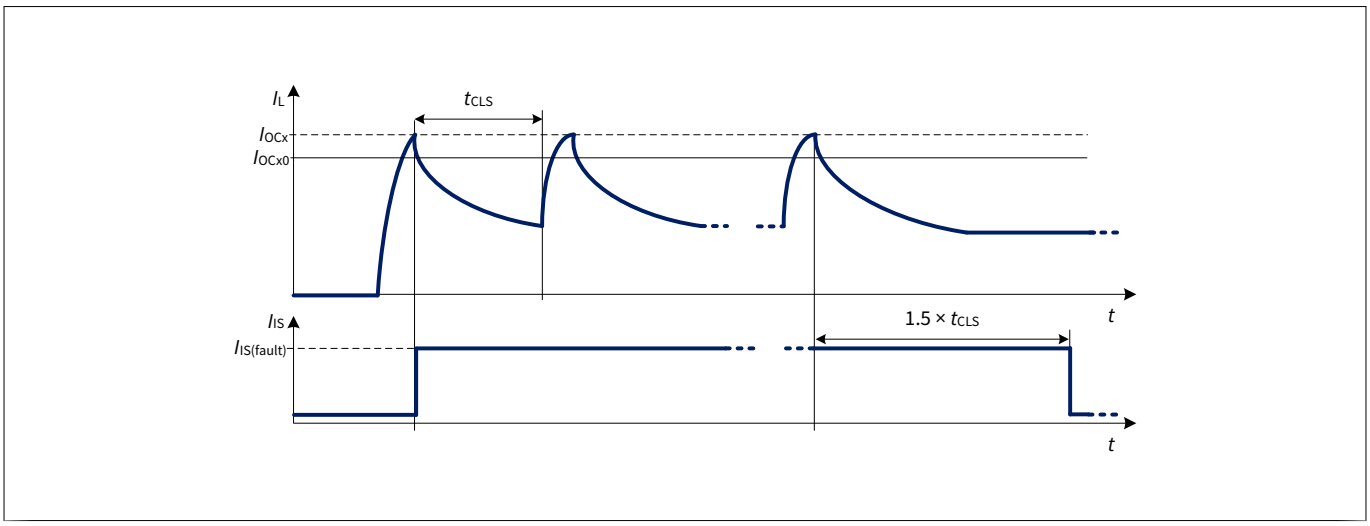

Figure 10 Timing diagram current limitation (inductive load)

For this mode, the MOSFETs are switched off each with the same slew rates (SR-level) as in normal operation.

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. This method of limiting the current has the advantage of greatly reduced power dissipation in the BTN9960LV compared to driving the MOSFET in linear mode.

Therefore it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

4.3.3.2 Switch-OFF with latch

If this mode is selected according to Table 9 and as soon as the current in forward direction in one switch (high-side or low-side) has reached the limit I_{OCx}, both output stages are shut down. This state is latched until the device is reset by a low signal with a minimum length of t_{reset} at the INH and IN pin. This behavior is illustrated in Figure 11.

In order to minimize power dissipation, the MOSFETs are switched off each with the same slew rate level SR4.

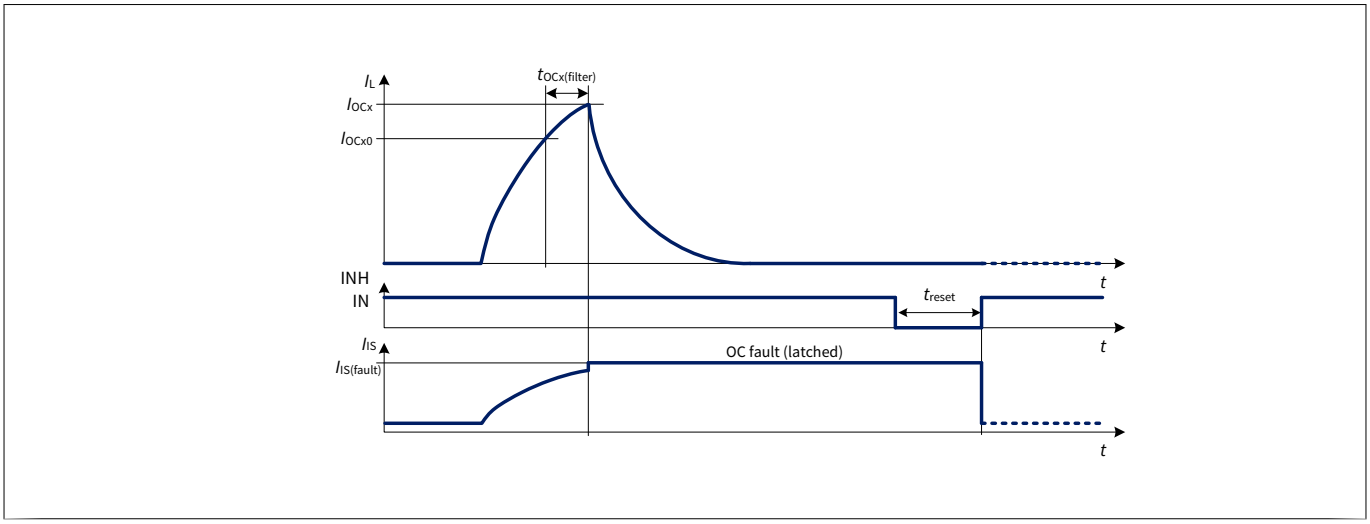

Figure 11 Timing diagram switch-OFF with latch (inductive load)

4.3.4 Short circuit protection

The device provides embedded protection functions against

- Output short circuit to ground
- Output short circuit to supply voltage
- Short circuit of load

The short circuit protection is realized by the previously described undervoltage and overcurrent protection in combination with the overtemperature shutdown of the device.

4.3.5 Electrical characteristics – protection functions

Table 10 Electrical characteristics – protection functions

V_S = 8 V to 18 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage shutdown						
Switch-ON voltage	$V_{UV(ON)}$	–	–	5.5	V	V_S increasing

(table continues...)

Table 10 (continued) Electrical characteristics – protection functions

V_S = 8 V to 18 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Switch-OFF voltage	$V_{UV(OFF)}$	3.8	–	4.5	V	V_S decreasing
ON/OFF hysteresis	$V_{UV(HY)}$	–	0.8	–	V	1)
Overcurrent shutdown						
Overcurrent detection level high-side	I_{OCH0}	35	47	60	A	V_S = 13.5 V
Overcurrent detection level low-side	I_{OCL0}	35	47	60	A	V_S = 13.5 V
Thermal shutdown						
Thermal shutdown junction temperature	T_{jSD}	155	175	200	°C	1)
Thermal switch-ON junction temperature	T_{jSO}	150	–	190	°C	1)
Thermal hysteresis	ΔT	–	7	–	K	1)
Protection and reset timing						
Shut-OFF time for HS and LS	t_{CLS}	–	115	210	µs	–
Undervoltage recovery delay time	t_{UVD}	–	115	210	µs	–
Reset pulse at INH and IN pin (INH & IN low)	t_{reset}	9	–	–	µs	–

1) Not subject to production test, specified by design.

4.4 Control and diagnostics

The control inputs IN and INH consist of TTL/CMOS compatible Schmitt triggers with hysteresis which control the integrated gate drivers for the MOSFETs. Setting the INH or/and IN pin to high enables the device. When the INH pin is high, one of the two power switches is switched on depending on the status of the IN pin. To deactivate both switches, the INH pin has to be set to low. No external driver is needed. The BTN9960LV can be interfaced directly to a microcontroller, as long as the maximum ratings in Chapter 3.1 are not exceeded.

4.4.1 Dead time generation

In bridge applications it has to be assured that the high-side and low-side MOSFET are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver IC, generating a so called dead time between switching off one MOSFET and switching on the other.

The dead time generated in the driver IC is dependent on the selected slew rate.

4.4.2 Adjustable slew rate

In order to optimize electromagnetic emission, one of 8 different switching speeds for the MOSFETs can be selected. This selectability allows the user to optimize the balance between emission and power dissipation within his own application. The slew rate adjustment function is only accessible, if no fault is present.

In case the device was in stand-by mode previously, the function is available after the device wake-up time t_{wakeup}. Therefore the first pulse at pin IN needs to exceed the wake-up time t_{wakeup}.

When INH = low and IN = high without a fault being present, the device is in SR selection mode with both high-side and low-side MOSFETs being switched off.

When the SR selection mode initially is entered, a temperature information is provided as described in Chapter 4.4.3.2 at the IS pin independently from the selected SR-level.

Only when IN goes low (falling edge) for a duration of t_{SR}, the next mode is selected when IN rises again. During this transition pulse, the INH pin has to be low permanently.

In the next mode, the slew rate won't be changed, but a current sense signal $I_{IS(SRx)}$ depending on the currently selected SR-level SRx (as further described in Chapter 4.4.3.2) is provided at the IS pin. This allows to validate if the desired SR-level has been selected.

For any further transition pulse, the next SR-level will be selected. The newly selected SR-level then will be indicated at the IS pin with the corresponding $I_{IS(SRx)}$.

After reaching SR-level SR7, the next selectable SR-level is SR0 again. This procedure is illustrated in Figure 12.

The SR selection mode is left if a fault occurs or by setting INH to high. The procedure is shown in the state diagram in Figure 15.

The states at pin IN and INH may not transition synchronous in the same direction, therefore a time delay of t_{lag} need to be applied.

After stand-by and power-up, the default value for the slew rate is level SR0.

After an undervoltage event the selected slew rate level is persistent, under the conditions described in Chapter 4.3.1 with more details.

In case an undervoltage event occurs during the slew rate selection mode, the slew rate configuration can not be guaranteed. Therefore slew rate programming need to be repeated once the undervoltage event has disappeared.

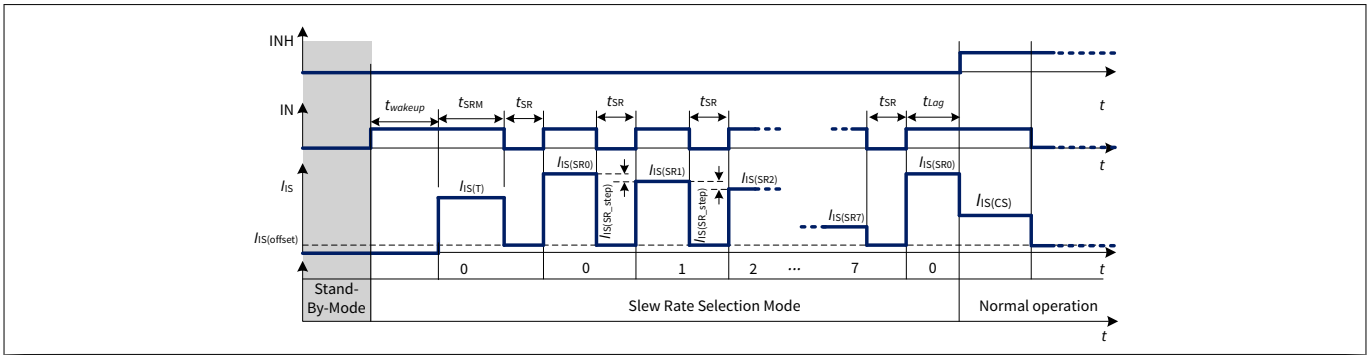

Figure 12 Slew rate level selection

Note: t_{wakeup} is only needed if the device was in stand-by-mode before.

4.4.3 Status flag diagnosis with current and temperature sense capability

The sense pin IS is used as a combined current sense, temperature sense, slew rate level feedback and fault flag output. Further details, in which state which signal is provided by the IS pin is described in Table 11. The IS pin has three different modes of operation:

4.4.3.1 Current sense

In normal operation (current sense mode), with the IN and INH pin being high (for further details see Table 11), a current source is connected to the IS pin, which delivers a current proportional to the forward load current flowing through the active high-side switch.

The sense current can be calculated out of the load current by the following equation:

$I_{IS} = I_L / dk_{ILIS} + I_{IS(offset)}$

The other way around, the load current can be calculated out of the sense current by following equation:

$I_L = dk_{ILIS} \cdot (I_{IS} - I_{IS(offset)})$

The differential current sense ratio dk_{ilis} is defined by:

$dk_{ILIS} = (I_{L2} - I_{L1}) / (I_{IS}(I_{L2}) - I_{IS}(I_{L1}))$

If the high-side drain current is zero ($I_{SD(HS)}$ = 0 A) the offset current $I_{IS} = I_{IS(offset)}$ still will be driven. The external resistor R_{IS} determines the voltage per IS output current. The voltage can be calculated by $V_{IS} = R_{IS} \cdot I_{IS}$.

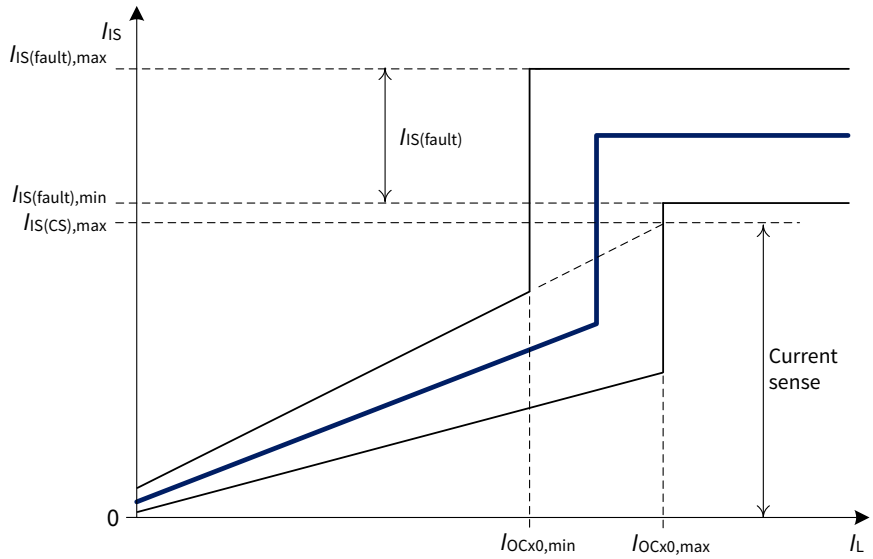

Figure 13 Sense current vs. load current

4.4.3.2 Temperature sense and slew rate feedback

In slew rate selection mode, with the IN pin being high and the INH being low after the first transition (further details see Chapter 4.4.2) the IS pin provides a constant current $I_{IS(SRx)}$, allowing to distinguish between the different SR-levels.

The sense current I_{IS} can be calculated as follows for the slew rate level SRx:

$I_{IS(SRx)} = I_{IS(SR0)} - x \cdot I_{IS(SR\_step)}$

To correctly determine all eight slew rate levels, $I_{IS(SR0)}$ and each individual device's $I_{IS(SR\_step)}$ have to be calibrated.

When initially entering the SR selection mode, a current source is connected to the IS pin, which delivers a current proportional to the junction temperature of the control chip T_{CC}, which is illustrated in Figure 14. The sense current $I_{IS(T)}$ can be calculated out of the junction temperature in Kelvin T[K] by the following equation:

$I_{IS(T)} = k_{TIS} \cdot T_{CC}$

Based on the temperature coefficient k_{TIS}, the temperature T_{CC} then calculates as follows:

$T_{CC} = I_{IS(T)} / k_{TIS}$

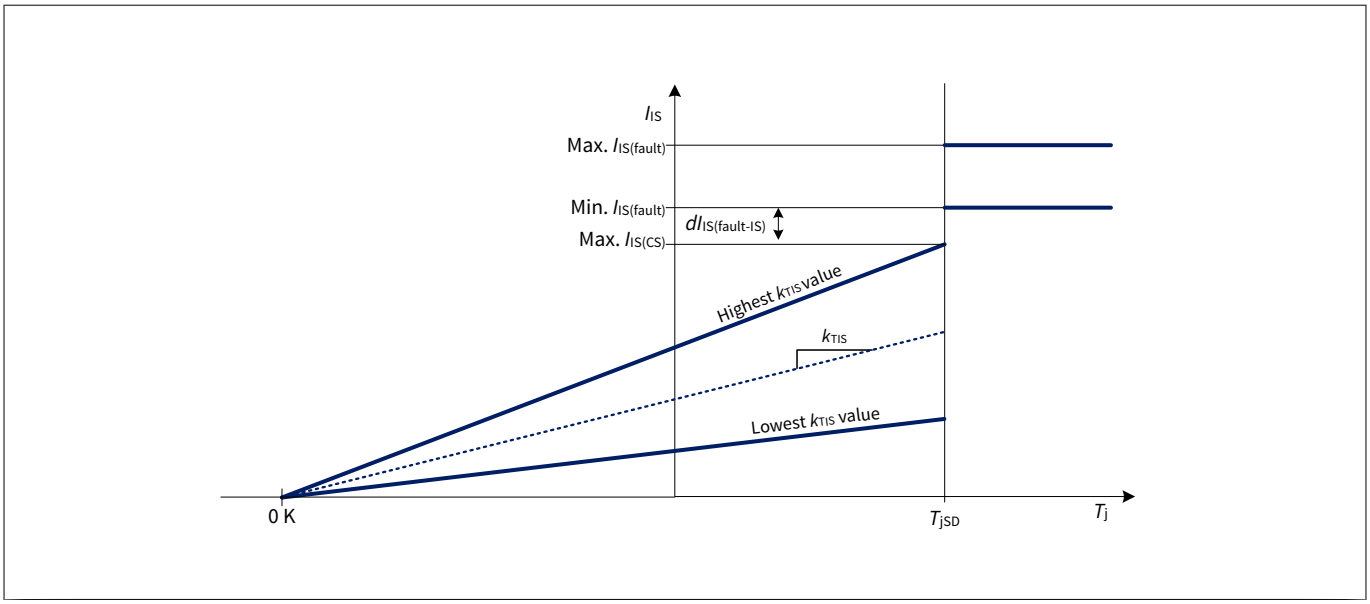

Figure 14 Sense current vs. junction temperature in the initial state of the SR selection mode

4.4.3.3 Fault feedback

In case of a fault condition, according to the truth table (Table 11), the status output is connected to a current source which is independent of the load current and provides $I_{IS(fault)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage.

4.4.4 Truth table

Table 11 Truth table

Device state	Inputs		Outputs			Mode
	INH	IN	HSS	LSS	IS	
Normal operation	0	0	OFF	OFF	$I_{IS(offset)}$	See note [2] Device enters stand-by mode after t > t_{stdby}
					tri state –	Device in stand-by mode
	1	0	OFF	ON	$I_{IS(offset)}$	LSS active
	1	1	ON	OFF	CS [3]	HSS active
Slew rate selection	0	1	OFF	OFF	$I_{IS(SRx,T)}$ $I_{IS(offset)}$	Slew rate selection mode During INH = IN = low pulse
Overtemperature (OT) at HSS or LSS	1	X	OFF	OFF	$I_{IS(fault)}$	Shutdown with latch, fault detected [4]
	X	1	OFF	OFF	$I_{IS(fault)}$	
Current limitation (CL) mode at HSS or LSS	1	1	OFF	ON	$I_{IS(fault)}$	Switched mode, fault detected [5]
	1	0	ON	OFF	$I_{IS(fault)}$	
Overcurrent (OC) switch-OFF with latch at HSS or LSS	1	X	OFF	OFF	$I_{IS(fault)}$	OC shutdown with latch, fault detected [4]
	X	1	OFF	OFF	$I_{IS(fault)}$	

(table continues...)

Table 11 (continued) Truth table

Undervoltage (UV), $V_S < V_{UV(OFF)}$	1	X	OFF	OFF	* [1]	Undervoltage shutdown, fault detected [6]
	X	1	OFF	OFF		

1) Sense current present ≤ $I_{IS(offset)}$.
2) The device only goes into stand-by mode if no fault is present.
3) Current sense - high-side (CS): $I_{IS} = I_L / dk_{ILIS} + I_{IS(offset)}$, for details see Chapter 4.4.3.1.
4) Requires the reset of the fault latch with INH = IN = low for t_{reset} to get back to normal operation.
5) Will return to normal operation after t_{CLS}; Fault signal $I_{IS(fault)}$ is reset after 1.5*t_{CLS} (see Chapter 4.3.3.1).
6) When $V_S > V_{UV(ON)}$ (rising), the device will return to normal operation after t_{UVD}; Fault signal $I_{IS(fault)}$ is reset after t_{UVD} (see Chapter 4.3.1).

Table 12 Switches – states table

Inputs	Switches
0 = logic LOW	OFF = switched off
1 = logic HIGH	ON = switched on
X = 0 or 1	

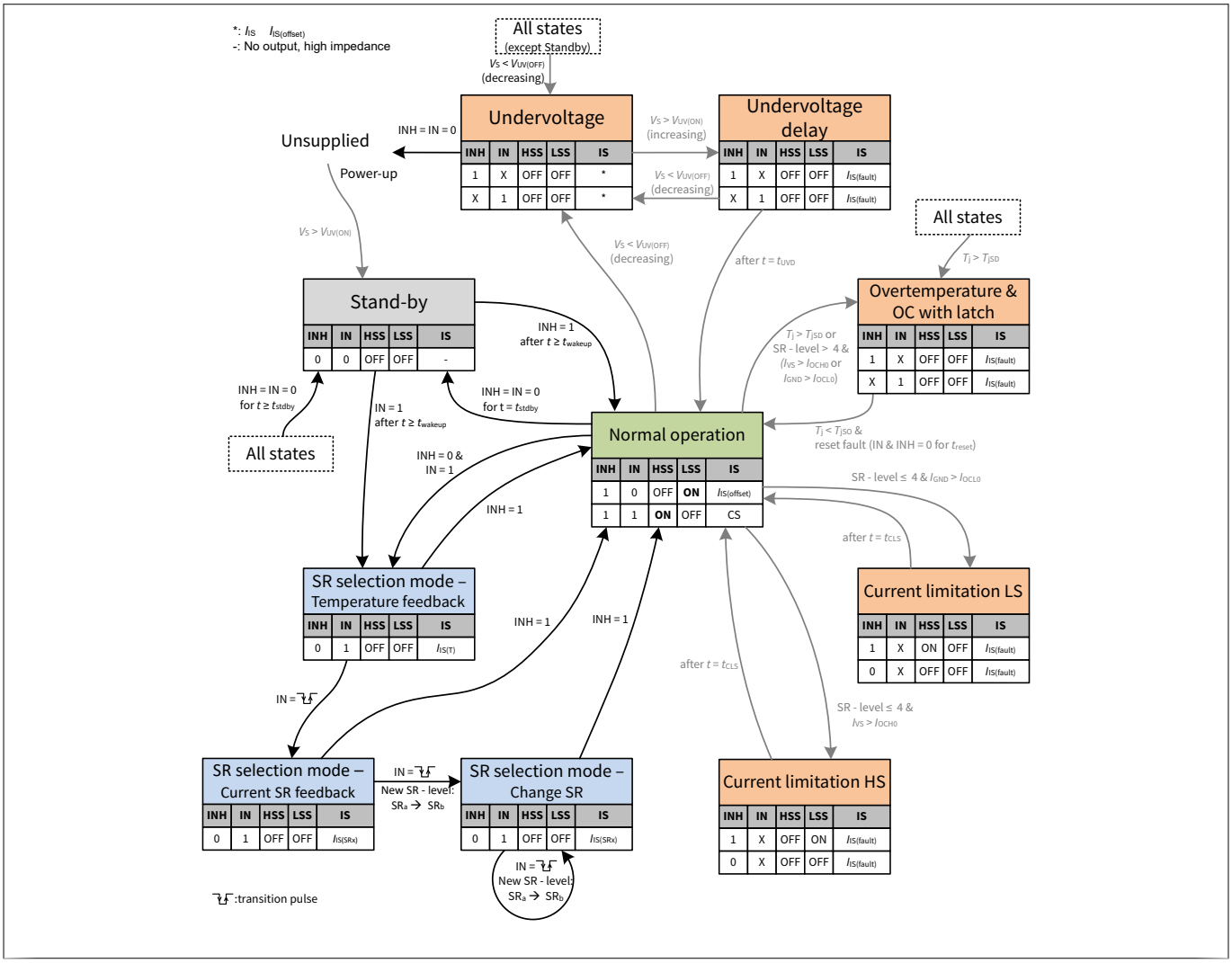

Figure 15 Simplified state diagram

4.4.5 Electrical characteristics – control and diagnostics

Table 13 Electrical characteristics – control and diagnostics

V_S = 8 V to 18 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Control inputs (IN and INH)						
High level voltage INH, IN	$V_{INH(H)}$ $V_{IN(H)}$	–	1.6	2.1	V	–
Low level voltage INH, IN	$V_{INH(L)}$ $V_{IN(L)}$	1.0	1.3	–	V	–
Low level voltage INH, IN for VS < 8 V	$V_{INH(L)\_UV(OFF)}$ $V_{IN(L)\_UV(OFF)}$	0.4	–	–	V	V_S = 4.5 V, falling V_S
Input voltage hysteresis	$V_{INH(HYS)}$ $V_{IN(HYS)}$	–	300	–	mV	1)
Input current high level	$I_{INH(H)}$ $I_{IN(H)}$	25	50	80	µA	V_{IN} = V_{INH} = 5.5 V
Input current low level	$I_{INH(L)}$ $I_{IN(L)}$	3	6	10	µA	V_{IN} = V_{INH} = 1.0 V
Slew rate selection						
Slew rate level selection pulse time	t_{SR}	0.5	–	80	µs	See Figure 12
Slew rate selection mode settling time	t_{SRM}	1	–	–	µs	See Figure 12
Wake-up time	t_{wakeup}	–	–	5	µs	After stand-by 1)
Lag time between IN/INH state change	t_{lag}	0.5	–	–	µs	1)
Time to enter stand-by mode	t_{stdby}	100	–	300	µs	After both INH and IN transitioned from high to low
Sense current for SR-level SR0	$I_{IS(SR0)}$	1.8	2.15	2.5	mA	SR-level = SR0
Current sense step between two SR-levels	$I_{IS(SR\_step)}$	150	190	230	µA	–
Current sense						
Differential current sense ratio in static on-condition dkILIS = dIL/dIIS BTN9960	dk_{ILIS}	21.7	28.9	36.1	10^3	1 A ≤ I_L < I_{OCH0} V_S = 13.5 V R_{IS} = 2 kΩ
Sense current in fault condition	$I_{IS(fault)}$	2.51	2.75	3.25	mA	V_S = 13.5 V

(table continues...)

Table 13 (continued) Electrical characteristics – control and diagnostics

V_S = 8 V to 18 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum analog sense current in normal operational condition	$I_{IS(CS)}$	–	–	2.5	mA	V_S = 13.5 V; in CS mode [1]
Isense leakage current	I_{ISL}	–	–	1	µA	$V_{INH} = V_{IN}$ = 0 V R_{IS} = 2 kΩ
Isense offset current	$I_{IS(offset)}$	30	300	600	µA	V_{INH} = 5 V V_{IN} = 0 V or $I_{SD(HS)}$ = 0 A R_{IS} = 2 kΩ
Temperature sense at 25°C	$I_{IS(T)\_25°C}$	–	1.2	–	mA	$I_{IS(T)}$ T_j = 25°C R_{IS} = 2 kΩ
Temperature coefficient for temperature sense	k_{TIS}	3.16	3.72	4.28	µA/K	[1]

1) Not subject to production test, specified by design.

5 Application information

Note: The following information is given as a hint for the implementation of the device only and cannot be regarded as a description or warranty of a certain functionality, condition or quality of the device.

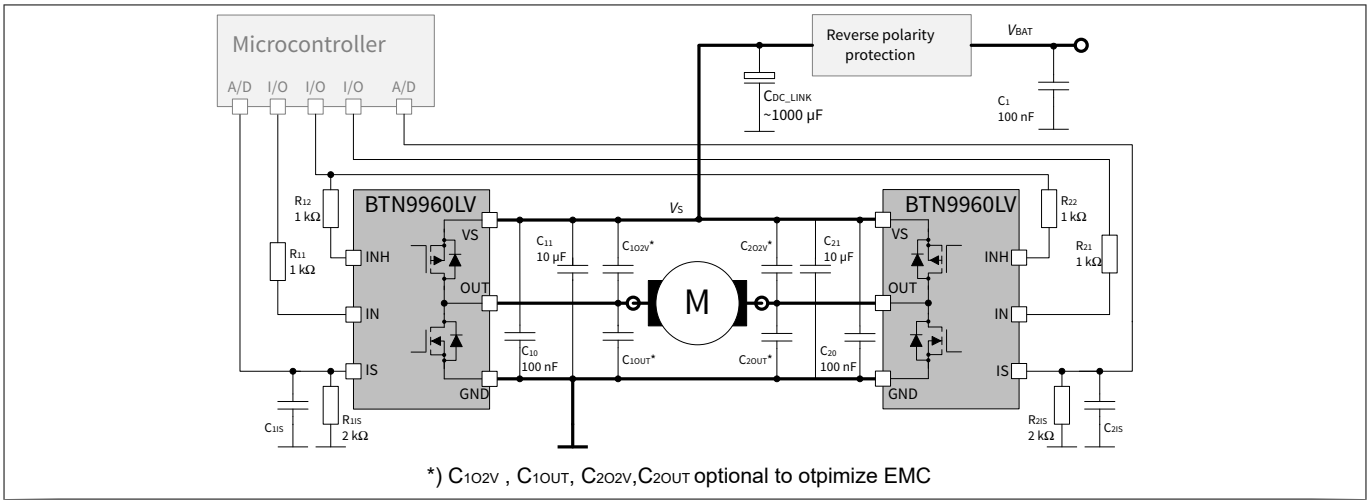

Figure 16 Application circuit: H-bridge with two BTN9960LV

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

To stabilize the supply voltage V_S in PWM operation or in over current limitation a sufficient dimensioned low ESR electrolytic capacitor CDC-Link is needed. It prevents destructive voltage peaks and drops. The supply voltage ripple at the device between VS pin and GND must be kept below 1 V peak-to-peak and the capacitors need to be sized accordingly. Therefore the ceramic capacitors C10/C11 respectively C20/C21 must be placed close to the device pins VS and GND. The traces should be kept as short as possible to minimize stray inductance. The value of the capacitors must be verified in the real application to ensure low ripple and transients at the VS pin. The digital inputs IN and INH need to be protected against over-currents (e.g. caused by induced voltage spikes) by a series resistor of typical 1 kΩ.

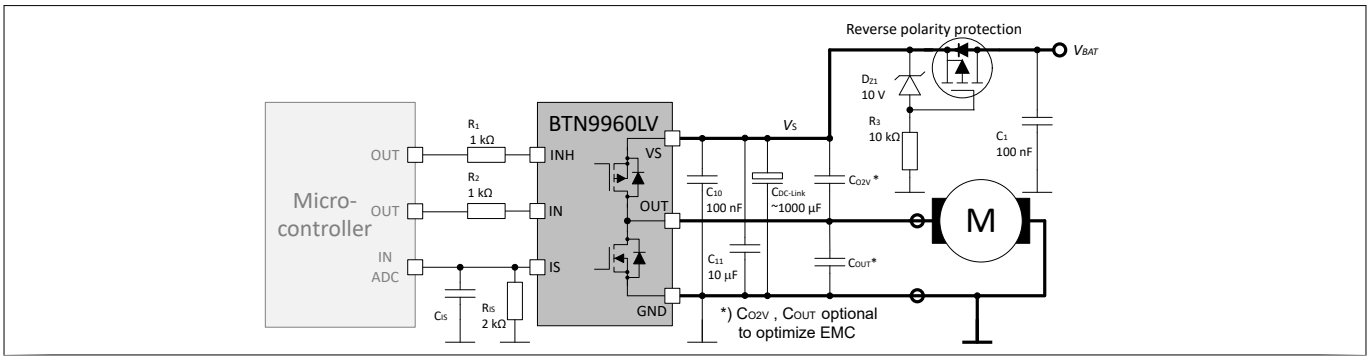

Figure 17 Application circuit: single half-bridge with load (motor) connected to GND

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

The applicable PWM frequency for which the output signal at OUT pin tracks the control signal at IN pin depends on:

- Desired duty cycle range of the output OUT (e.g. 20% to 80%)
- Selected slew rate for the output OUT

5 Application information

- Switch-ON and switch-OFF delay times of HS / LS switches ($t_{dr(HS)}$, $t_{df(LS)}$, $t_{df(HS)}$, $t_{dr(LS)}$), depending on slew rate
- Rise-time and fall-time of HS / LS switch ($t_{r(HS)}$, $t_{f(LS)}$, $t_{f(HS)}$, $t_{r(LS)}$), depending on slew rate

6 Package

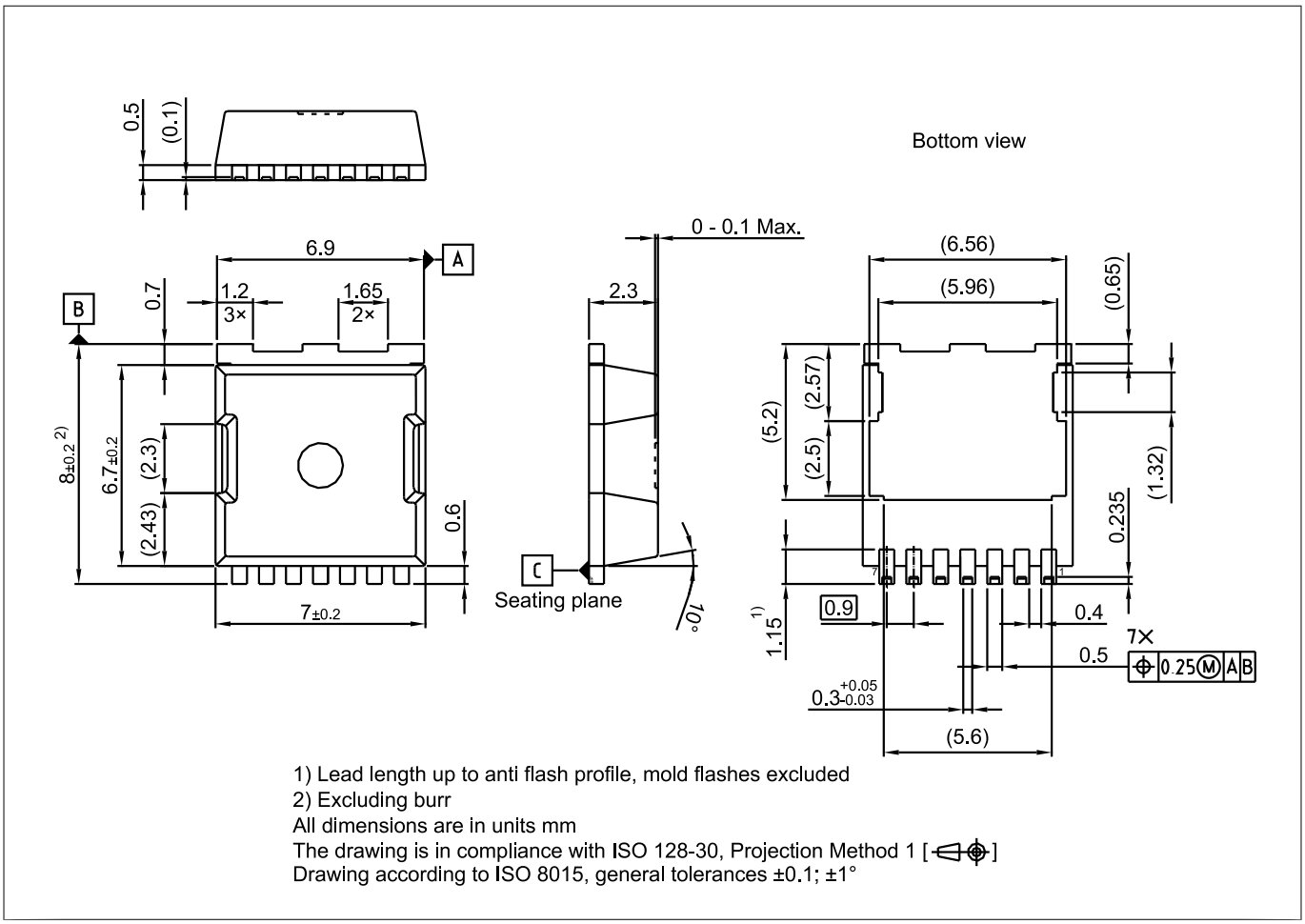

Figure 18 PG-HSOF-7 (sTOLL)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further package information, please visit our website:

https://www.infineon.com/packages

7 Revision history

Document version	Date of release	Description of changes
1.0	2023-03-01	Initial release

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