# BTS4130QGA

## Smart High-Side Power Switch

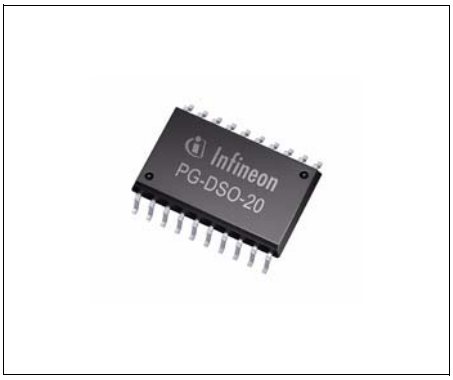
Automotive Power

Never stop thinking

**Smart High-Side Power Switch** **BTS4130QGA**

**Four Channel Device**

# 1 Overview




**PG-DSO-20-32**

### Basic Features

- Withstand low Cranking Voltage
- Fit for 12V Application
- Four Channel device
- Very low Stand-by Current
- CMOS Compatible Inputs
- Electrostatic Discharge Protection (ESD)
- Optimized Electromagnetic Compatibility
- Logic ground independent from load ground
- Very low Leakage Current from OUT to the load in OFF State
- Green Product (RoHS compliant)
- AEC Qualified

### Description

The BTS4130QGA is a quad channel Smart High-Side Power Switch. It is embedded in a PG-DSO-20-32 package, providing protective functions and diagnostics. The power transistor is built by a N-channel power MOSFET with charge pump. The device is monolithically integrated in Smart technology. It is specially designed to drive relays as well as resistive loads in the harsh automotive environment.

**Table 1 Electrical Parameters (short form)**

| Parameter | Symbol | Value |
|---|---|---|
| Operating voltage range | $V_{SOP}$ | 5.5V .... 20V |
| Undervoltage switch OFF at $T_j$ = -40°C | $V_{s\ (USO)}$ | 3.2V |
| Maximum load per channel | $P_{BULB}$ | 2 * R5W, relays or LED |
| Over voltage protection | $V_{S\ (AZ)}$ | 43V |
| Max ON State resistance at $T_j$ = 150°C per channel | $R_{DS(ON)}$ | 260mΩ |
| Nominal load current (one channel active) | $I_{L\ (nom)}$ | 1.8A |
| Minimum current limitation | $I_{L\_SCR}$ | 5A |
| Standby current for the whole device with load | $I_{S(off)}$ | 16µA |
| Maximum reverse battery voltage | $-V_{s(REV)}$ | 32V |

| Type | Package | Marking |
|---|---|---|
| BTS4130QGA | PG-DSO-20-32 | BTS4130QGA |

### Diagnostic Feature

- Open load detection in OFF state
- Feedback of the thermal shutdown in ON state
- Diagnostic feedback with open drain output

### Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of $V_S$ protection
- Electrostatic discharge protection (ESD)

### Application

- All types of resistiv, inductive and capacitive loads

# 2 Block Diagram

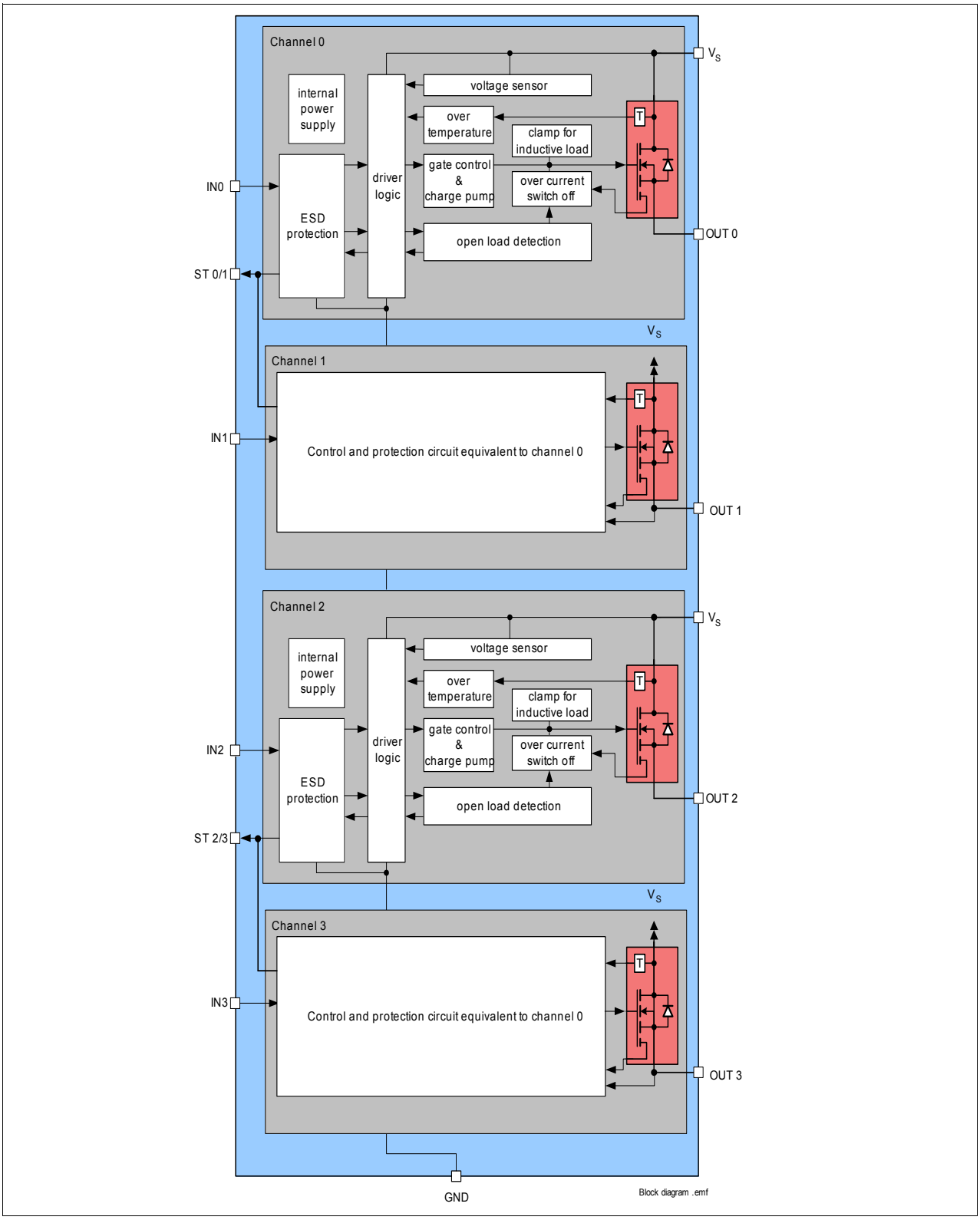



**Figure 1 Block diagram for the BTS4130QGA**

# 3 Pin Configuration

## 3.1 Pin Assignment

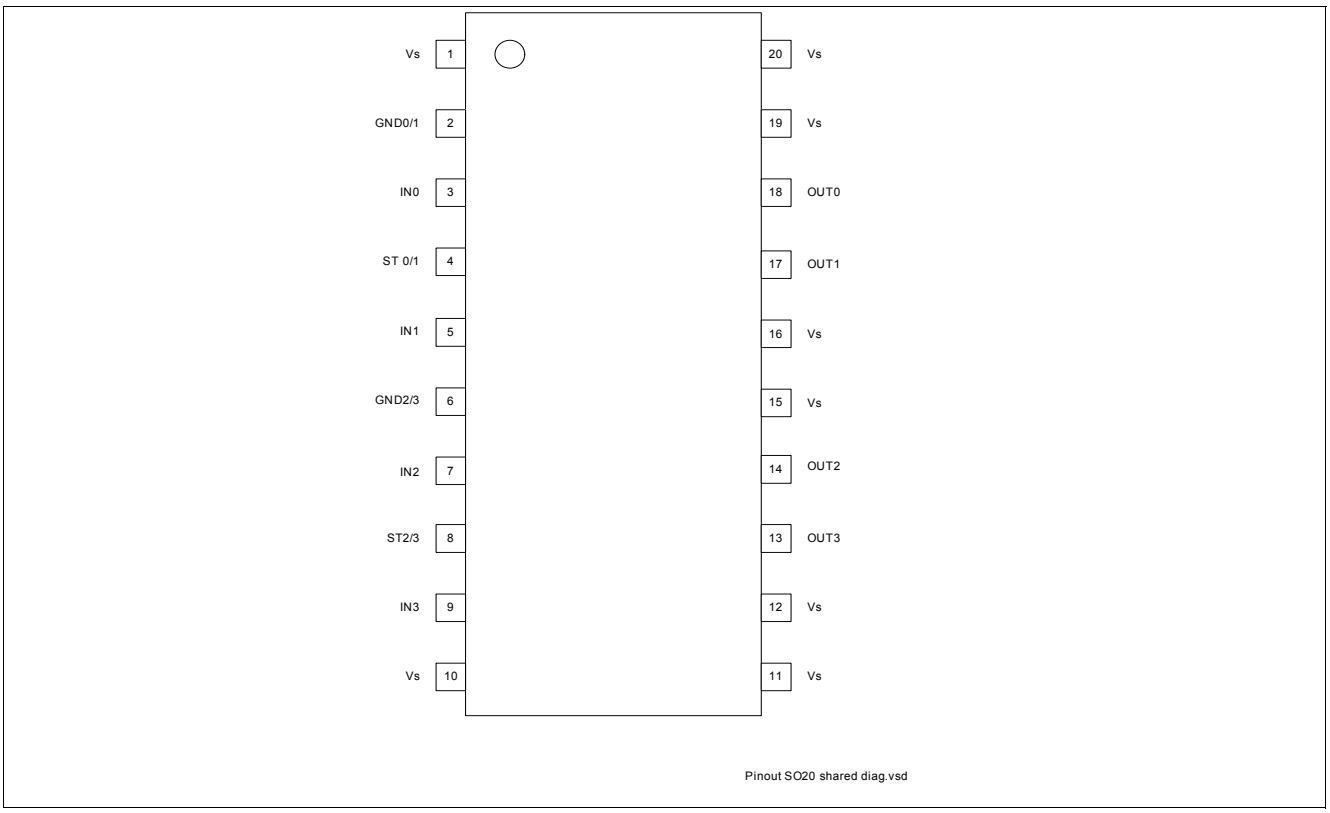



**Figure 2 Pin Configuration**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1, 10, 11, 12, 15, 16, 19, 20 | $V_S$ | **Battery voltage;** Design the wiring for the simultaneous maximum short circuit currents from channel 0 and 1 and also for low thermal resistance |
| 2 | GND0/1 | **Ground**; Ground connection for channel 0 and 1 |
| 3 | IN0 | **Input channel 0;** Input signal for channel 0. Activate the channel in case of logic high level |
| 4 | ST 0/1 | **Diagnostic feedback;** of channel 0/1. Open drain. |
| 5 | IN1 | **Input channel 1;** Input signal for channel 1. Activate the channel in case of logic high level |
| 6 | GND2/3 | **Ground**; Ground connection for channel 2 and 3 |
| 7 | IN2 | **Input channel 2;** Input signal for channel 2. Activate the channel in case of logic high level |
| 8 | ST 2/3 | **Diagnostic feedback;** of channel 2/3. Open drain. |
| 9 | IN3 | **Input channel 3;** Input signal for channel 3. Activate the channel in case of logic high level |

| Pin | Symbol | Function |
|---|---|---|
| 13 | OUT3 | **Output 3;** Protected High side power output channel 3 |
| 14 | OUT2 | **Output 2;** Protected High side power output channel 2 |
| 17 | OUT1 | **Output 1;** Protected High side power output channel 1 |
| 18 | OUT0 | **Output 0;** Protected High side power output channel 0 |

## 3.3 Voltage and Current Definition

**Figure 3** shows all terms used in this data sheet, with associated convention for positive values.

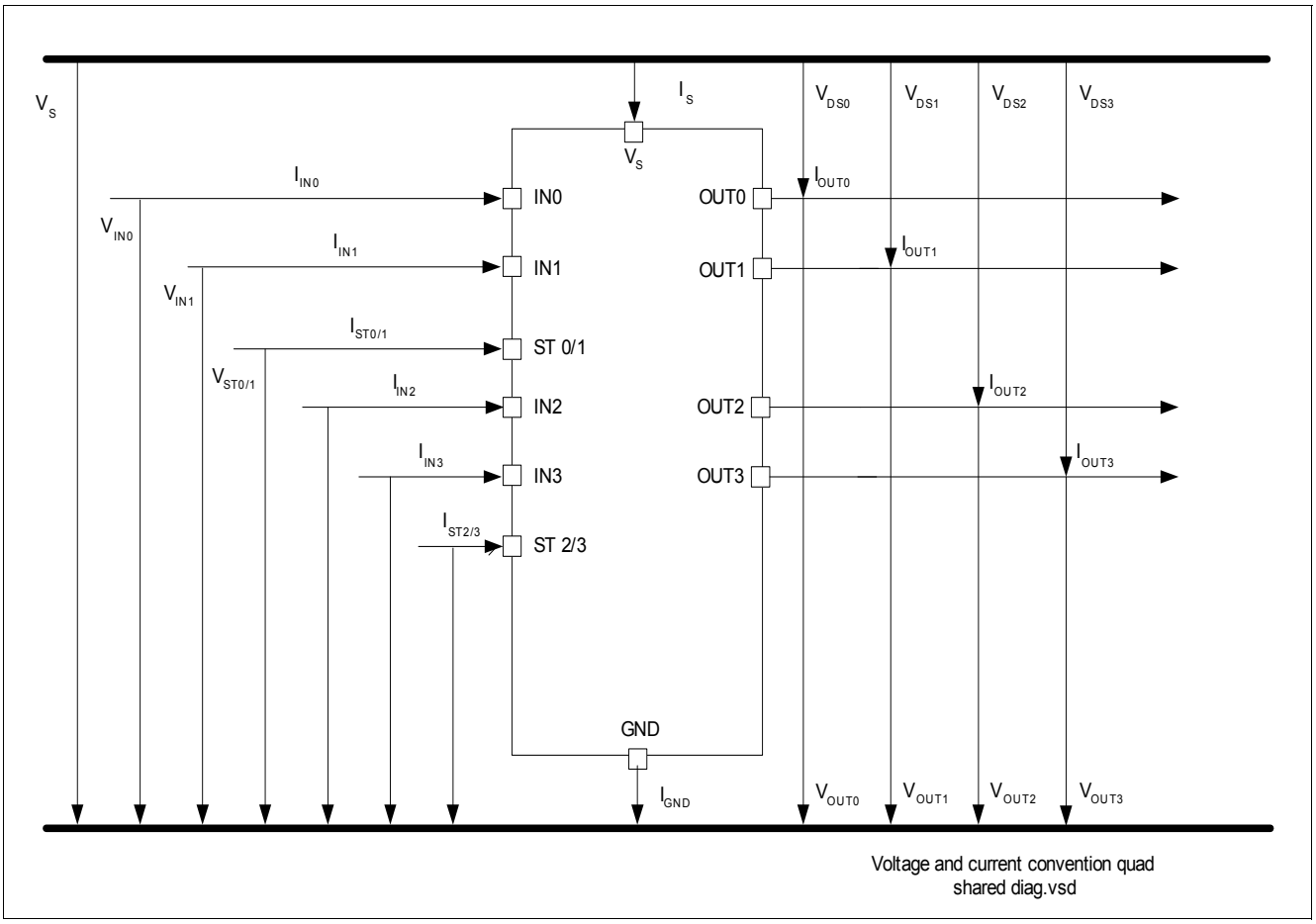



**Figure 3 Voltage and current definition**

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Absolute Maximum Ratings [1)]**

$T_J$ = 25°C; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| **Voltages** | | | | | | |
| 4.1.1 | Supply voltage | $V_S$ | -0.3 | 43 | V | – |
| 4.1.2 | Reverse polarity Voltage | $-V_{S(REV)}$ | – | 32 | V | – |
| 4.1.3 | Supply voltage for short circuit protection | $V_{bat(SC)}$ | 0 | 20 | V | $R_{ECU}$ = 20mΩ, $R_{Cable}$ = 16mΩ/m, $L_{Cable}$ = 1µH/m, $\ell$ = 0 or 5m [2)] see Chapter 6 |
| **Input pins** | | | | | | |
| 4.1.4 | Voltage at INPUT pins | $V_{IN}$ | -10 | 16 | V | – |
| 4.1.5 | Current through INPUT pins | $I_{IN}$ | -0.3 | 0.3 | mA | – |
| 4.1.6 | Current through INPUT pins pulsed | $I_{IN}$ | -5 | 5 | mA | Only for testing |
| **Status pin** | | | | | | |
| 4.1.7 | Current through ST 0/1 pin | $I_{ST0/1}$ | -5 | 5 | mA | – |
| 4.1.8 | Current through ST 2/3 pin | $I_{ST2/3}$ | -5 | 5 | mA | – |
| **Power stage** | | | | | | |
| 4.1.9 | Load current | $\lvert I_L \rvert$ | – | $I_{L(LIM)}$ | A | – |
| 4.1.10 | Power dissipation (DC), all channel active | $P_{TOT}$ | – | 1.4 | W | $T_A$ = 85°C, $T_j$ <150°C |
| 4.1.11 | Maximum Switchable energy, single pulse | $E_{AS}$ | – | 76 | mJ | $I_L$ = 2.3A, $V_S$ = 12V |
| **Temperatures** | | | | | | |
| 4.1.12 | Junction Temperature | $T_j$ | -40 | 150 | °C | – |
| 4.1.13 | Dynamic temperature increase while switching | $\Delta T_j$ | – | 60 | K | – |
| 4.1.14 | Storage Temperature | $T_{stg}$ | -55 | 150 | °C | – |
| **ESD Susceptibility** | | | | | | |
| 4.1.15 | ESD Resistivity IN pin | $V_{ESD}$ | -1 | 1 | kV | HBM[3)] |
| 4.1.16 | ESD Resistivity ST 0/1, 2/3 pins | $V_{ESD}$ | -4 | 4 | kV | HBM[3)] |
| 4.1.17 | ESD Resistivity OUT to all other pins shorted | $V_{ESD}$ | -5 | 5 | kV | HBM[3)] |

1) Not subject to production test, specified by design

2) Set up in accordance to AEC Q100-012 and AEC Q101-006

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

$T_j$ = -40 °C to +150 °C; (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| 4.2.1 | Operating Voltage | $V_{SOP}$ | 5.5 | 20 | V | $V_{IN}$ = 4.5V, $R_L$ = 12Ω, $V_{DS}$ < 0.5V |
| 4.2.2 | Undervoltage switch OFF | $V_{SUV}$ | – | 3.2 | V | -[1], $T_j$ = -40°C, $V_{DS}$ < 0.5V |
| 4.2.3 | Operating current<br>One channel active<br>Four channels active | $I_{GND}$ | <br>–<br>– | <br>0.9<br>3.3 | mA | $V_{IN}$ = 5V |
| 4.2.4 | Standby current for whole device with load | $I_{S(OFF)}$ | –<br>–<br>– | 16<br>16<br>24 | µA | $T_j$ = 25°C<br>$T_j$ = 85°C[2]<br>$T_j$ = 150°C, $V_s$ = 12V, $R_L$ = 12Ω, $V_{IN}$ = 0V |

1) Battery voltage is decreasing

2) Not subject to production test. Specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

| Pos. | Parameter | Symbol | Limit values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 4.3.1 | Junction to Soldering Point each channel | $R_{thJSP}$ | – | – | 15 | K/W | –[1] |
| 4.3.2 | Junction to Ambient | $R_{thJA}$ | – | 45 | – | K/W | with 6cm² cooling area[1] |

1) Not subject to production test, specified by design

# 5 Power Stage

The power stages are built by an N-channel vertical power MOSFET (DMOS) with charge pump.

## 5.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature $T_j$. **Figure 4** shows the dependencies for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

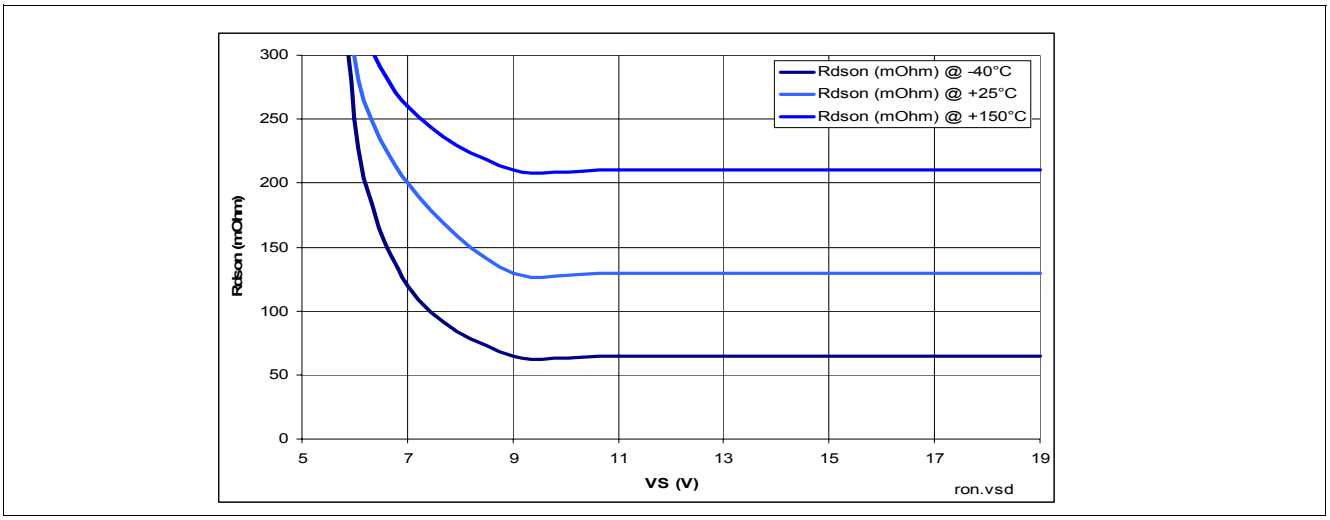



**Figure 4 Typical ON-state resistance**

A high signal (See **Chapter 8**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

## 5.2 Turn ON / OFF Characteristics

**Figure 5** shows the typical timing when switching a resistive load.

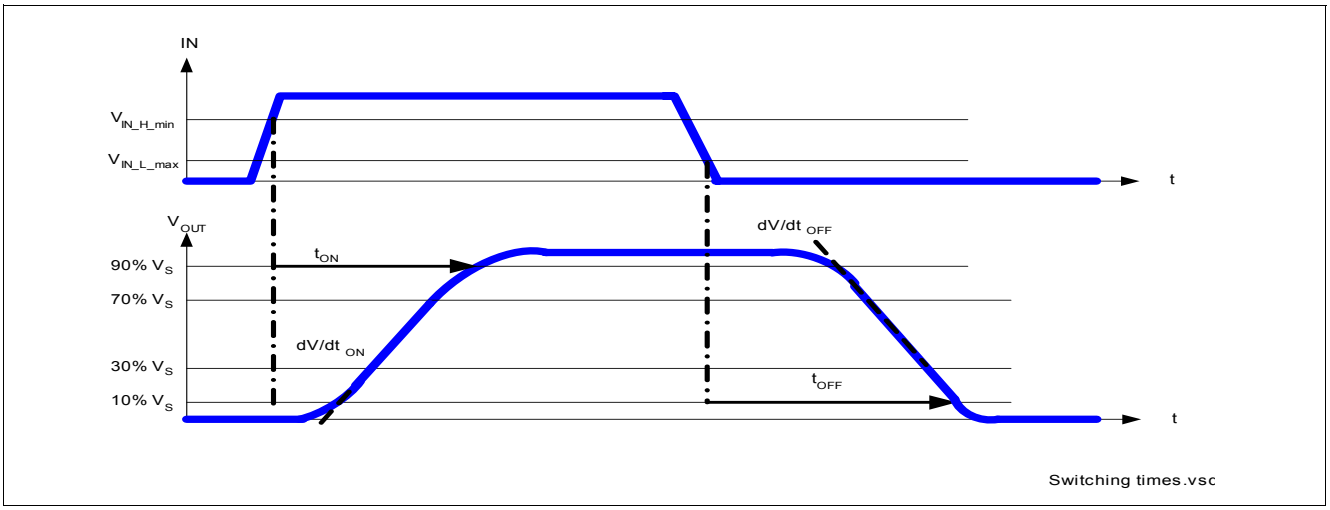



**Figure 5 Turn ON/OFF (resistive) timing**

## 5.3 Inductive Output Clamp

When switching OFF inductive loads with high side switches, the voltage $V_{OUT}$ drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a voltage clamp mechanism implemented that keeps the negative output voltage at a certain level ($V_S$-$V_{DS(AZ)}$). Please refers to **Figure 6** and **Figure 7** for details. Nevertheless, the maximum allowed load inductance is limited.

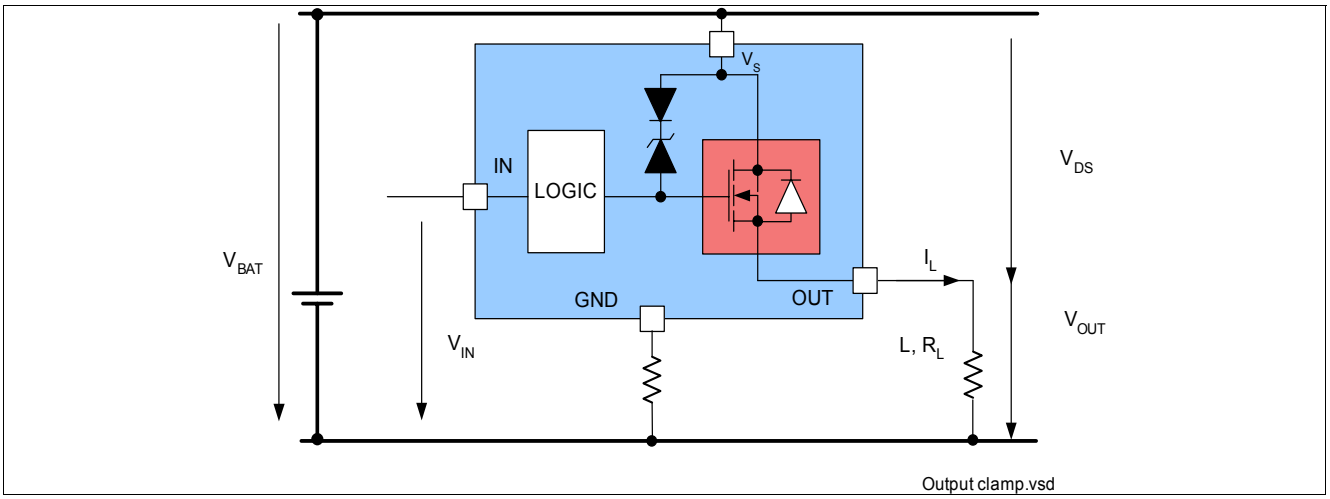



**Figure 6 Output clamp (OUT0 and OUT1)**

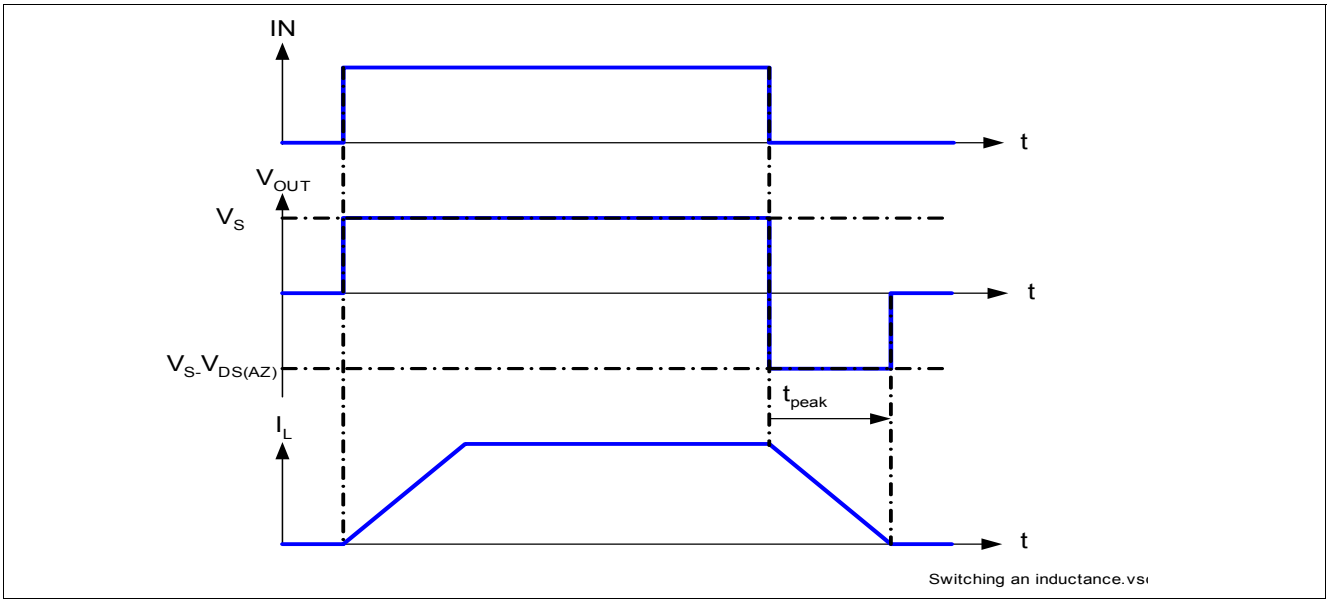



**Figure 7 Switching an inductance**

### 5.3.1 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTS4130QGA. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[ \frac{V_S - V_{DS(AZ)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right]$$

Following equation simplifies under the assumption of $R_L$ = 0Ω.

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 8** for the maximum allowed inductivity.

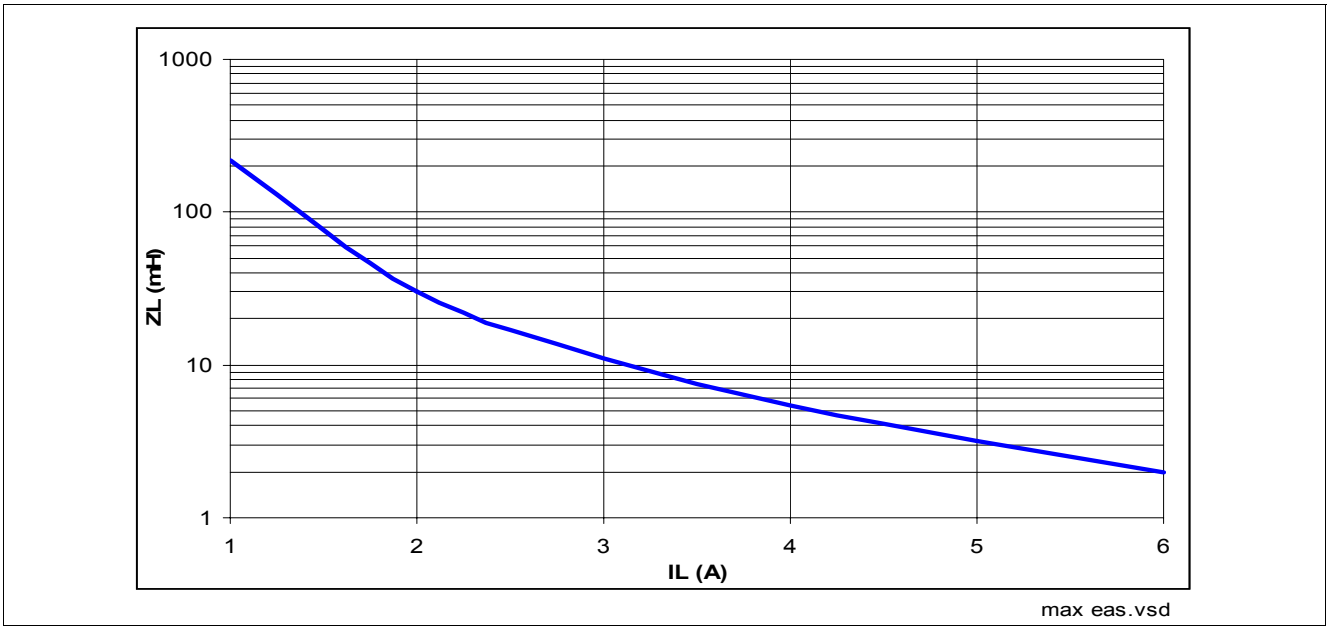



**Figure 8 Maximum energy dissipation single pulse, $T_{j,Start}$ = 150 °C**

## 5.4 Electrical Characteristics Power Stage

**Electrical Characteristics: Power stage**

$V_S$ = 12 V, $T_j$ = -40 °C to +150 °C. Typical values are given at $T_j$ = 25°C

| Pos. | Parameter | Symbol | Limit values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.4.1 | ON-state resistance per channel | $R_{DS(ON)}$ | – | 130 | – | mΩ | $T_j$ = 25°C,[1]<br>$I_L$ = 2A,<br>$V_{IN}$ = 5V,<br>See **Figure 4** |
| | | | – | 210 | 260 | | $T_j$ = 150°C |
| 5.4.2 | Nominal load current per channel<br>One channel active<br>Two channel active<br>Four channel active | $I_{L(nom)}$ | <br>2.1<br>1.5<br>1.1 | <br>–<br>–<br>– | <br>–<br>–<br>– | A | $T_A$ = 85°C[1],<br>$T_j$ <150°C |
| 5.4.3 | Drain to source clamping voltage<br>$V_{DS(AZ)} = V_S - V_{OUT}$ | $V_{DS(AZ)}$ | 41 | 47 | 52 | V | $I_{DS}$ = 40mA[2] |
| 5.4.4 | Output leakage current per channel | $I_{L(OFF)}$ | – | 1 | 5 | µA | $V_{IN}$ = 0V |
| 5.4.5 | Slew rate ON<br>10% to 30% $V_{OUT}$ | $dV/dt_{ON}$ | 0.2 | – | 1 | V/µs | $R_L$=12Ω,<br>$V_S$=12V<br>See **Figure 5** |
| 5.4.6 | Slew rate OFF<br>70% to 40% $V_{OUT}$ | $-dV/dt_{OFF}$ | 0.2 | – | 1.1 | V/µs | |
| 5.4.7 | Turn-ON time to 90% $V_S$<br>Includes propagation delay | $t_{ON}$ | – | 100 | 250 | µs | |
| 5.4.8 | Turn-OFF time to 10% $V_S$<br>Includes propagation delay | $t_{OFF}$ | – | 100 | 270 | µs | |

1) Not subject to production test, specified by design

2) Voltage is measured by forcing $I_{DS}$.

# 6 Protection Mechanisms

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

## 6.1 Loss of Ground Protection

In case of loss of the module ground, where the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pins. In that case, a maximum $I_{(OUTGND)}$ can flow out of the output.

## 6.2 Undervoltage Protection

Below $V_{SUV\_max}$, the under voltage mechanism is met. If the supply voltage is below the under voltage mechanism, the device is OFF (turns OFF). As soon as the supply voltage is above the under voltage mechanism, then the device can be switched ON and the protection functions are operational.

## 6.3 Overvoltage Protection

There is a clamp mechanism for over voltage protection. To guarantee this mechanism operates properly in the application, the current in the zener diode $ZD_{AZ}$ has to be limited by a ground resistor. **Figure 9** shows a typical application to withstand overvoltage issues. In case of supply greater than $V_{S(AZ)}$, the power transistor switches ON and the voltage across logic section is clamped. As a result, the internal ground potential rises to $V_S$ - $V_{S(AZ)}$. Due to the ESD zener diodes, the potential at pins IN and ST 0/1/2/3 rises almost to that potential, depending on the impedance of the connected circuitry. Integrated resistors are provided at the IN pins to protect the input circuitry from excessive current flow during this condition but an external resistor must be provided at the ST0/1/2/3 pins.

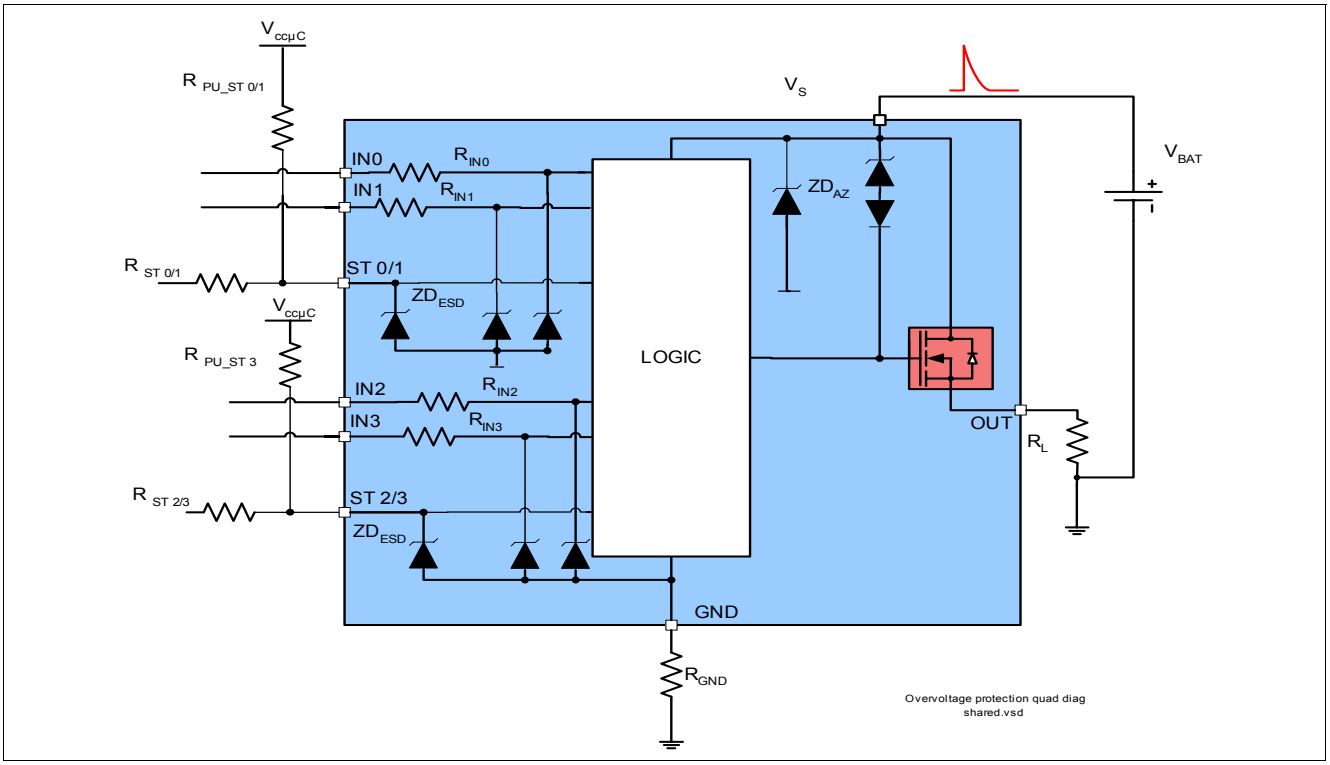



**Figure 9 Over voltage protection with external components**

In the case the supply voltage is in between of $V_{S(SC)\ max}$ and $V_{DS(AZ)}$, the output transistor is still operational and follow the input. If at least one channel is in ON state, parameters are no longer warranted and lifetime is reduced compared to normal mode. This specially impacts the short circuit robustness, as well as the maximum energy $E_{AS}$ the device can handle.

## 6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logical pins has to be limited to the maximum current described in **Chapter 4.1**, sometimes with an external resistor. **Figure 10** shows a typical application. The $R_{GND}$ resistor is used to limit the current in the zener protection of the device. Resistors $R_{IN}$ and $R_{ST}$ are used to limit the current in the logic of the device and in the ESD protection stage. The recommended value for $R_{GND}$ is 150Ω, for $R_{ST\ 0/1}$ = 15kΩ. In case the over voltage is not considered in the application, $R_{GND}$ can be replaced by a Shottky diode.

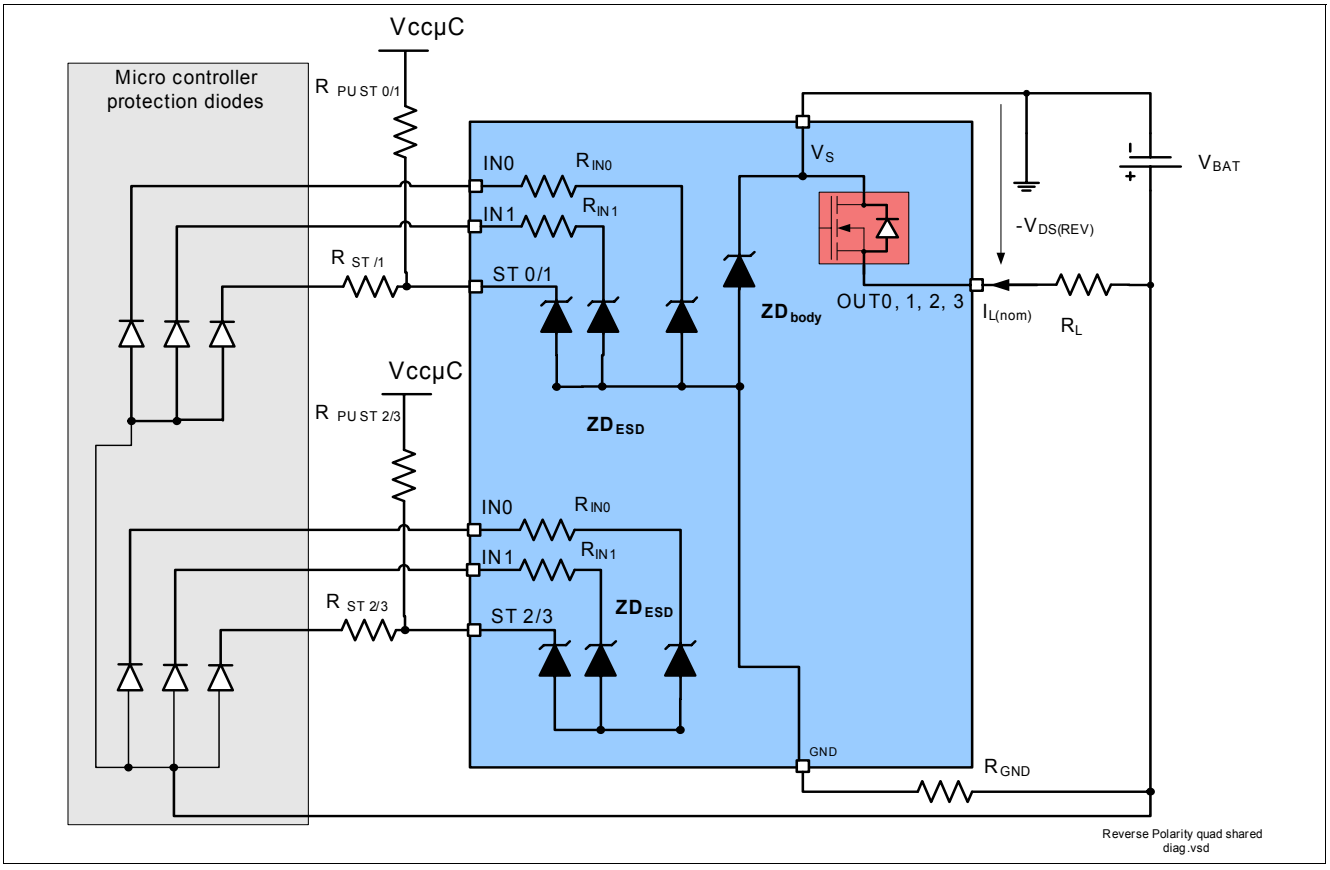



**Figure 10 Reverse polarity protection with external components**

## 6.5 Overload Protection

In case of overload, or short circuit to ground, the BTS4130QGA offers several protections mechanisms.

### 6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained to a safe level by limiting the current to the maximum current allowed in the switch $I_{L(LIM)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS. At thermal shutdown, the device turns OFF and cools down. A restart mechanism is used, after cooling down, the device restarts and limits the current to $I_{L(SCR)}$. **Figure 11** shows the behavior of the current limitation as a function of time.

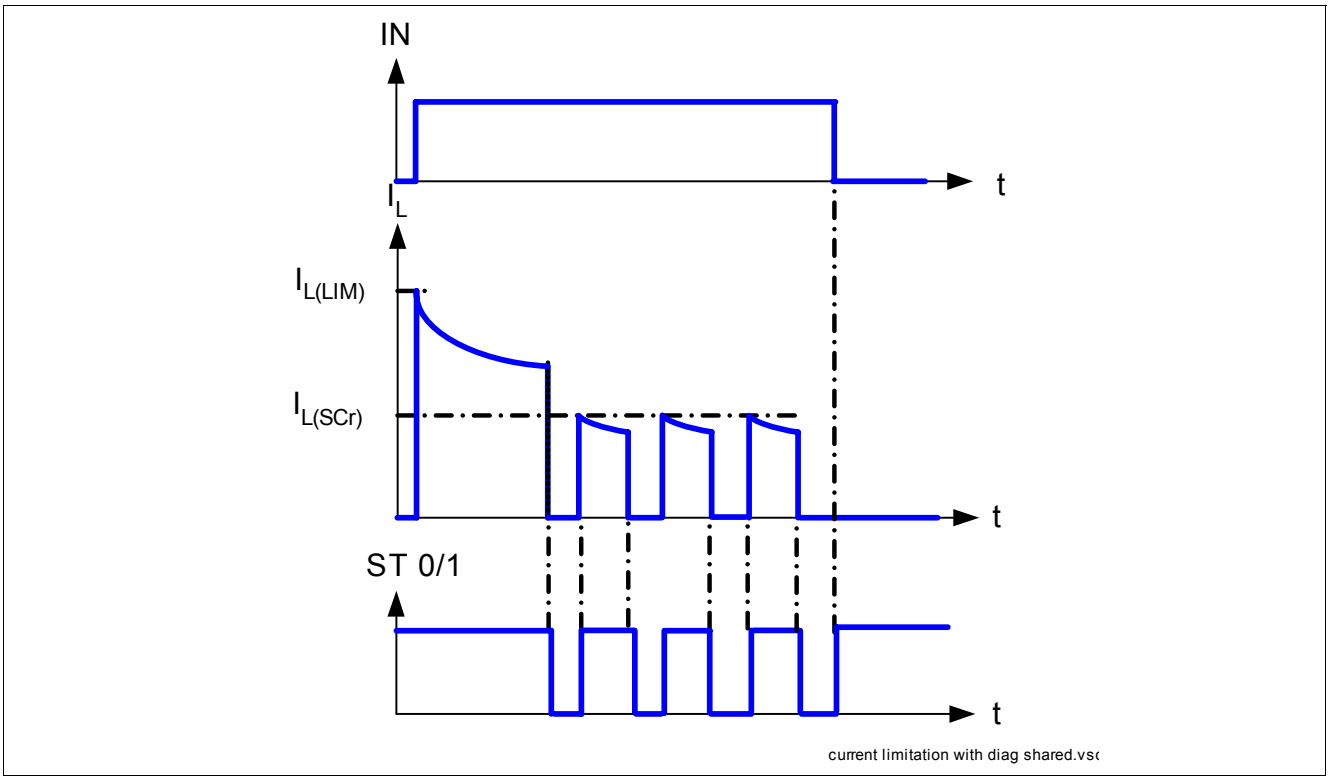



**Figure 11 Current limitation function of the time**

## 6.6 Electrical Characteristics Protection Functions

**Electrical Characteristics: Protection**

$V_S$ = 12 V, $T_j$ = -40 °C to +150 °C. Typical values are given at $T_j$ = 25°C

| Pos. | Parameter | Symbol | Limit values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **Loss of ground** | | | | | | | |
| 6.6.1 | Output leakage current while GND disconnected | $I_{OUT(GND)}$ | – | – | 2 | mA | $V_S$ = 32V<br>$V_{IN}$ = 0V |
| **Reverse polarity** | | | | | | | |
| 6.6.2 | Drain source diode voltage during reverse polarity | $-V_{DS(REV)}$ | – | 600 | – | mV | $I_L$= - 2A,<br>$T_j$ = 150°C<br>$V_{IN}$ = 0V |
| **Overvoltage** | | | | | | | |
| 6.6.3 | Over voltage protection | $V_{S(AZ)}$ | 41 | 47 | 52 | V | $I_s$ = 40mA |
| **Overload condition** | | | | | | | |
| 6.6.4 | Load current limitation | $I_{L(LIM)}$ | –<br>–<br>5 | –<br>9<br>– | 14<br>–<br>– | A | $T_j$ = -40°C,<br>$T_j$ = 25°C,<br>$T_j$ = 150°C |
| 6.6.5 | Repetitive short circuit current limit | $I_{L(SCR)}$ | –<br>– | 6.5<br>6.5 | –<br>– | A | One channel[1)]<br>Two channel[1)] parallel |
| 6.6.6 | Thermal shutdown temperature | $T_{jSC}$ | 150 | – | – | °C | – |
| 6.6.7 | Thermal shutdown hysteresis | $\Delta T_{JT}$ | – | 10 | – | K | – [1)] |

1) Not subject to production test, but specified by design

# 7 Diagnostic Mechanism

For diagnosis purpose, the BTS4130QGA provides status pin.

## 7.1 ST 0/1/2/3 Pin

BTS4130QGA status pins are an open drain, active low circuit. **Figure 12** shows the equivalent circuitry. As long as no “hard” failure mode occurs (Short circuit to GND / Over temperature or open load in OFF), the signal is permanently high, and due to a required external pull-up to the logic voltage will exhibit a logic high in the application. A suggested value for the $R_{PU\ ST01}$ is 15 kΩ.

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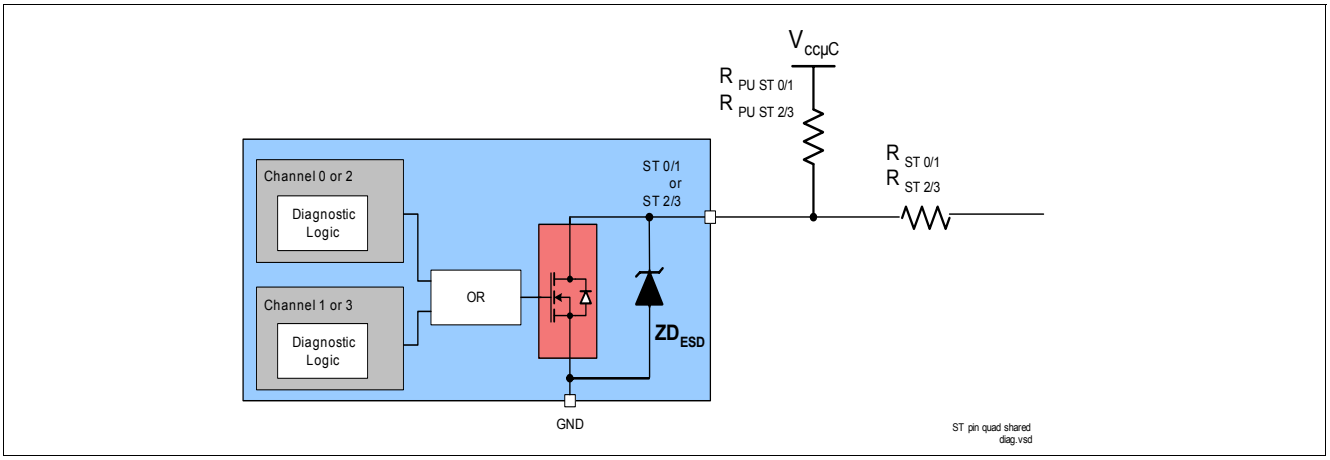



**Figure 12 Status output circuitry**

## 7.2 ST0/1/2/3 Signal in Case of Failures

**Table 2** gives a quick reference for the logical state of the ST 0/1/2/3 pins during device operation.

**Table 2 ST 0/1 2/3 truth table**

| Device operation | IN0/2 | IN1/3 | OUT0/2 | OUT1/3 | ST 0/1 ST2/3 |
|---|---|---|---|---|---|
| Normal operation | L | L | L | L | H |
| | L | H | L | H | |
| | H | L | H | L | |
| | H | H | H | H | |
| Open Load channel 0/2 | L | X | > $V_{(OL)}$ | X | L[1)] |
| | H | X | H | X | H |
| Open Load channel 1/3 | X | L | X | > $V_{(OL)}$ | L[1)] |
| | X | H | X | H | H |
| Over temperature both channel | L | L | L | L | H |
| | X | H | X | L | L |
| | H | X | L | X | L |
| Over temp channel 0/2 | L | X | L | X | H |
| | H | X | L | X | L |
| Over temp channel 1/3 | X | L | X | L | H |
| | X | H | X | L | L |

1) L if potential at the output exceeds the Openload detection voltage

### 7.2.1 Diagnostic in Open Load, Channel OFF

For open load diagnosis in OFF-state, an external output pull-up resistor ($R_{OL}$) is recommended. For calculation of the pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ has to be taken into account. **Figure 13** gives a sketch of the situation and **Figure 14** shows the typical timing diagram.

$I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ (see **Chapter 5.4**) and external leakages e.g. due to humidity, corrosion, etc... in the application.

To reduce the stand-by current of the system, an open load resistor switch $S_{OL}$ is recommended.

If the channel is OFF, the output is no longer pulled down by the load and $V_{OUT}$ voltage rises to nearly $V_S$. This is recognized by the device as open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the ST 0/1 signal is switched to a logical low $V_{ST01(L)}$.

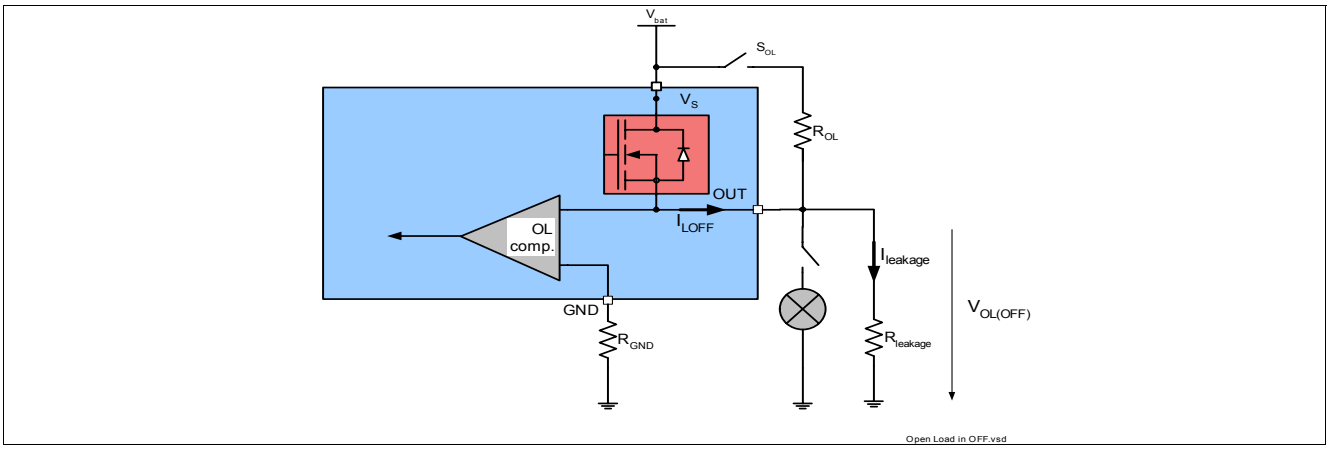



**Figure 13 Open load detection in OFF electrical equivalent circuit**

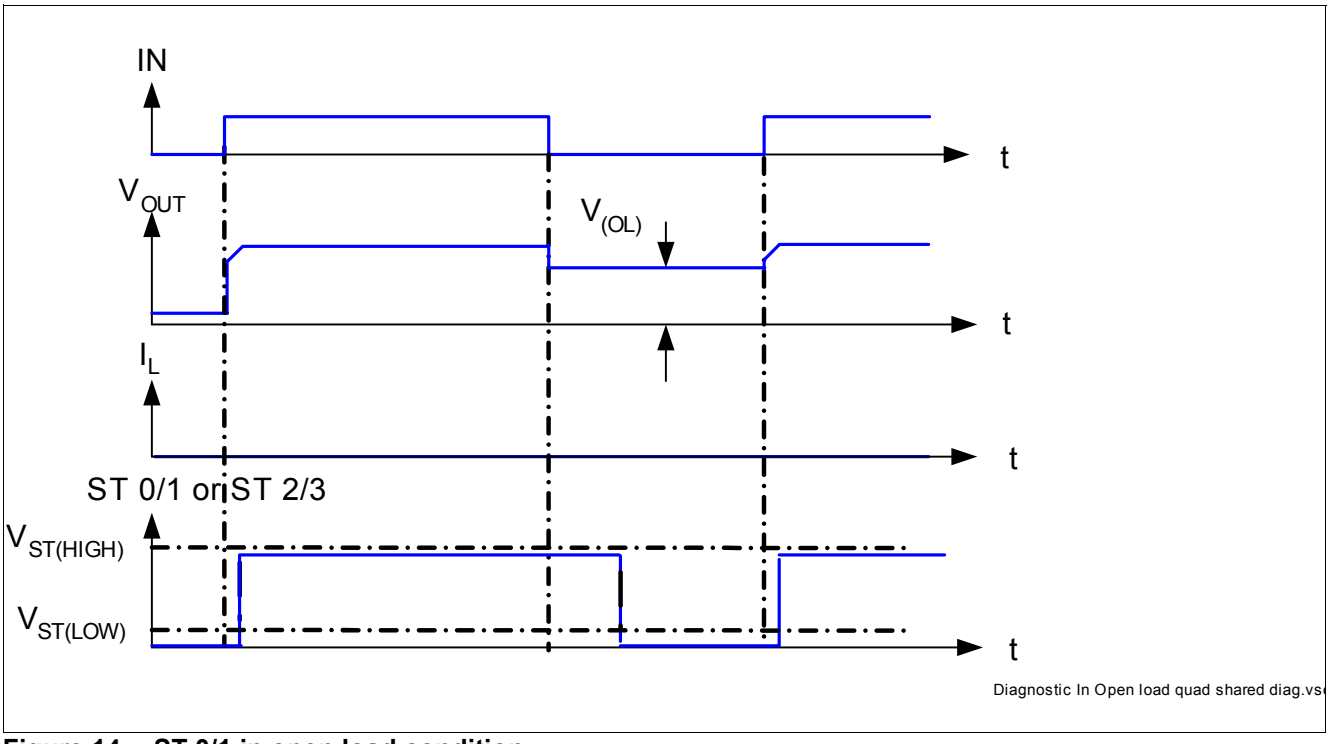



**Figure 14 ST 0/1 in open load condition**

### 7.2.2 ST 0/1 Signal in case of Over Temperature

In case of over temperature, the junction temperature reaches the thermal shutdown temperature $T_{jSC}$.
In that case, the ST 0/1 signal is toggling between $V_{ST01(L)}$ and $V_{ST01(H)}$. **Figure 15** gives a sketch of the situation.

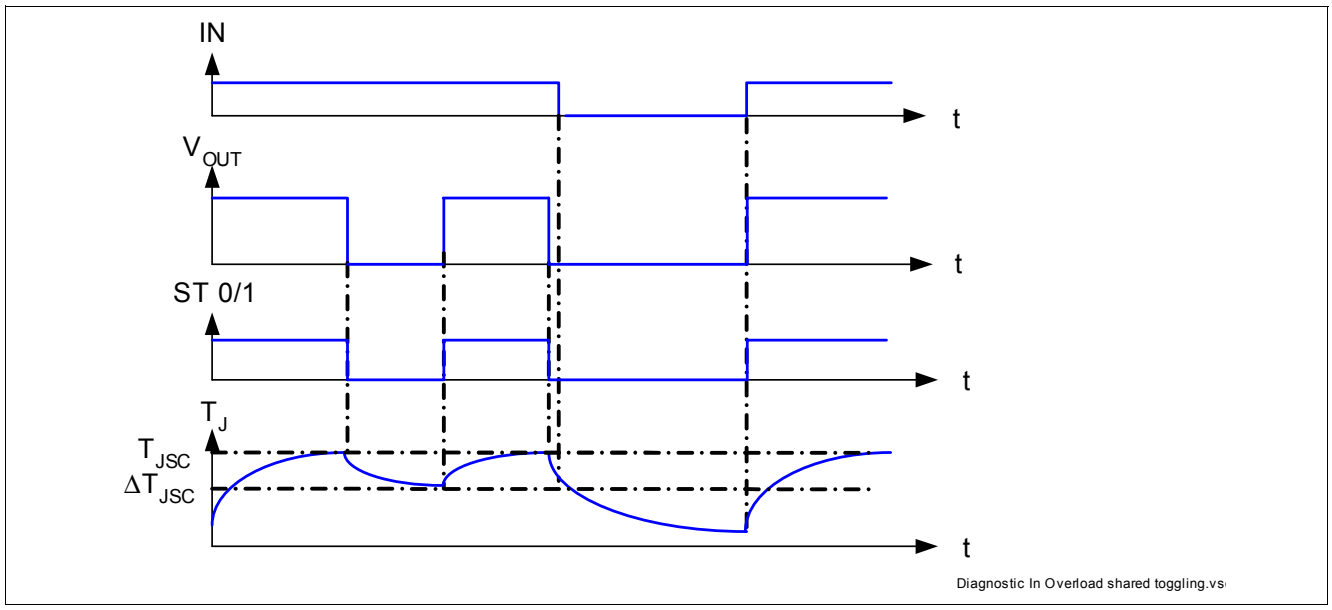



**Figure 15 Sense signal in overtemperature condition**

.

## 7.3 Electrical Characteristics Diagnostic Functions

**Electrical Characteristics: Diagnostics**

$V_S$ = 12 V, $T_j$ = -40 °C to +150 °C. Typical values are given at $T_j$ = 25°C

| Pos. | Parameter | Symbol | Limit values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **Load condition threshold for diagnostic** | | | | | | | |
| 7.3.1 | Open Load detection voltage | $V_{OL(OFF)}$ | 1.7 | 2.8 | 4.0 | V | – |
| **ST 0/1 or ST 2/3 pin** | | | | | | | |
| 7.3.2 | Status output (open drain) High level; Zener limit voltage | $V_{ST\ (HIGH)}$ | 5.4 | – | – | V | $I_{ST}$= +1.6mA[1], Zener Limit voltage |
| 7.3.3 | Status output (open drain) Low level | $V_{ST\ (LOW)}$ | – | – | 0.6 | V | $I_{ST}$= +1.6mA[1] |
| **Diagnostic timing** | | | | | | | |
| 7.3.4 | Status change after positive input slope with open load | $t_{dST(ON\_OL)}$ | – | 10 | 20 | µs | –[2] |
| 7.3.5 | Status change after positive input slope with overload | $t_{dST(ON\_OvL)}$ | 30 | – | – | µs | –[2] |
| 7.3.6 | Status change after negative input slope with open load | $t_{dST(OFF\_OL)}$ | – | – | 500 | µs | – |
| 7.3.7 | Status change after negative input slope with overtemperature | $t_{dST(OFF)}$ | – | – | 20 | µs | –[2] |

1) If ground resistor $R_{GND}$ is used, the voltage drop across this resistor has to be added

2) Not subject to production test, specified by design

# 8 Input Pins

## 8.1 Input Circuitry

The input circuitry is CMOS compatible. The concept of the Input pin is to react to voltage transition and not to voltage threshold. With the Schmidt trigger, it is impossible to have the device in an un-defined state, if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in an linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 16** shows the electrical equivalent input circuitry. The pull down current source ensures the channel is OFF with a floating input.

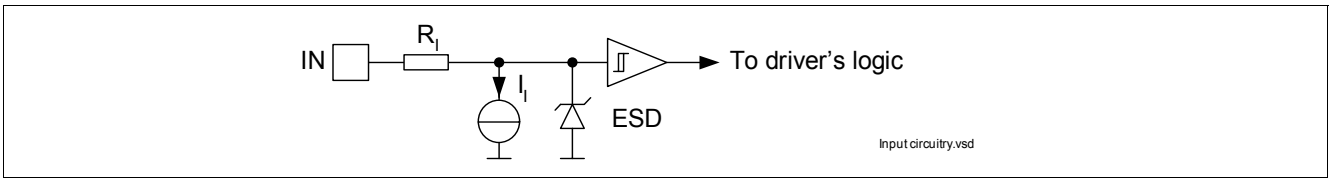



**Figure 16 Input pin circuitry**

## 8.2 Electrical Characteristics

**Electrical Characteristics: Diagnostics**

$V_S$ = 12 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) Typical values are given at $T_j$ = 25°C

| Pos. | Parameter | Symbol | Limit values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **INput pins characteristics** | | | | | | | |
| 8.2.1 | Low level input voltage | $V_{IN(L)}$ | – | – | 1 | V | –[1)] |
| 8.2.2 | High level input voltage | $V_{IN(H)}$ | 2.5 | – | – | V | –[1)] |
| 8.2.3 | Input voltage hysteresis | $V_{IN(HYS)}$ | – | 0.2 | – | V | –[2)] |
| 8.2.4 | Low level input current | $I_{IN(L)}$ | 5 | – | 20 | µA | $V_{IN}$ = 0.4V |
| 8.2.5 | High level input current | $I_{IN(H)}$ | 10 | 35 | 60 | µA | $V_{IN}$ = 5V |
| 8.2.6 | Input resistance | $R_I$ | 2.5 | 4 | 6 | kΩ | See **Figure 16** |

1) If ground resistor $R_{GND}$ is used, the voltage drop across this resistor has to be added

2) Not subject to production test, specified by design

# 9 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

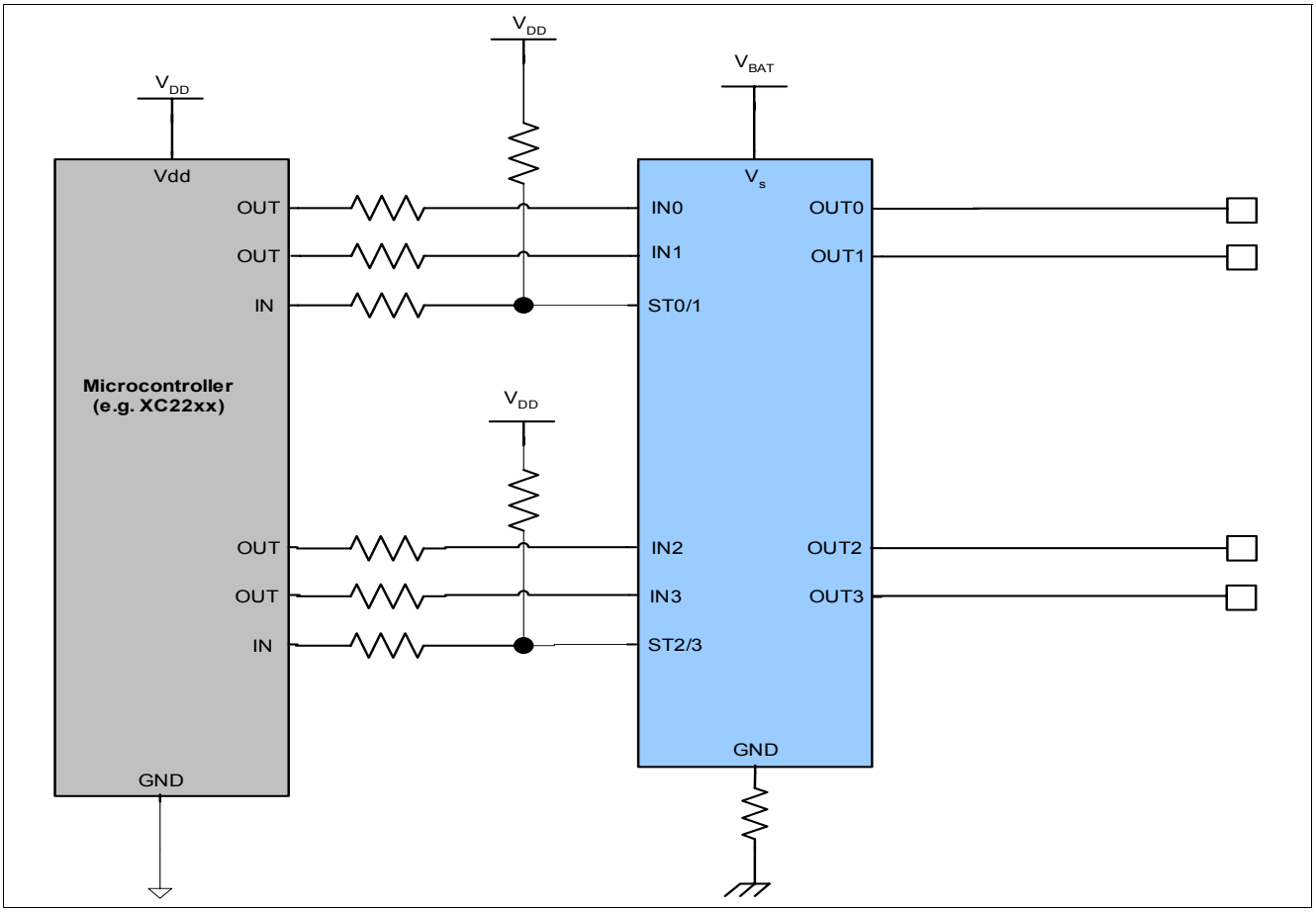


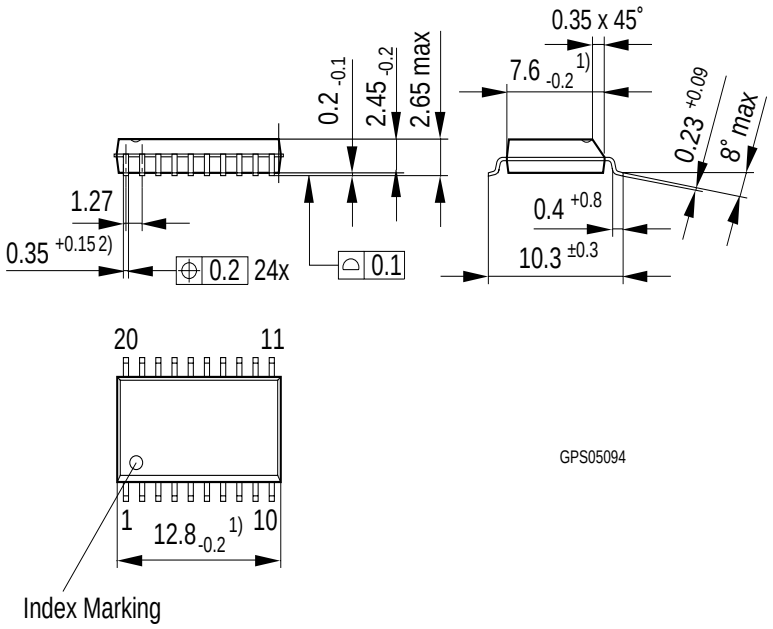

**Figure 17 Application diagram with BTS4130QGA**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

## 9.1 Further Application Information

- For further information you may visit **http://www.infineon.com/**

# 10 Package Outlines




1) Does not include plastic or metal protrusions of 0.15 max per side

2) Does not include dambar protrusion of 0.05 max per side

**Figure 18 PG-DSO-20-32** (Plastic Dual Small Outline Package)

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

# 11 Revision History

| Version | Date | Changes |
|---|---|---|
| 1.0 | 2008-03-18 | Creation of the data sheet |

**Edition 2008-03-18**

**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**



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