PROFET™+ 12V

BTS5020-1EKA

Smart High-Side Power Switch
Single Channel, 20mΩ

Data Sheet

Rev. 2.2, 2013-11-12

Automotive Power

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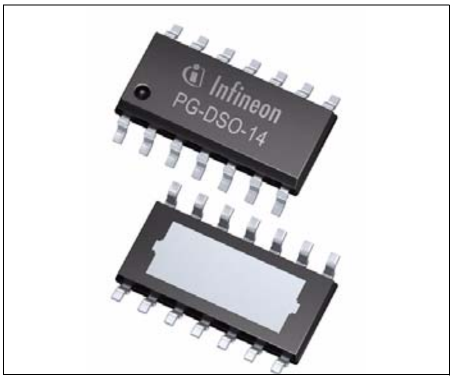
1 Overview



PG-DSO-14-47-EP

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps

Basic Features

- One channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant)
- AEC qualified

Description

The BTS5020-1EKA is a 20 mΩ single channel Smart High-Side Power Switch, embedded in a PG-DSO-14-47-EP, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device is integrated in Smart6 technology. It is specially designed to drive lamps up to 2 * P27W/P21W + R5W, as well as LEDs in the harsh automotive environment.

Table 1 Product Summary

Parameter	Symbol	Value
Operating voltage range	$V_{S(OP)}$	5 V ... 28 V
Maximum supply voltage	$V_{S(LD)}$	41 V
Maximum ON state resistance at T_J = 150 °C	$R_{DS(ON)}$	44 mΩ
Nominal load current	$I_{L(NOM)}$	6.5 A
Typical current sense ratio	k_{ILIS}	3000
Minimum current limitation	$I_{L5(SC)}$	50 A
Maximum standby current with load at T_J = 25 C	$I_{S(OFF)}$	500 nA

Type	Package	Marking
BTS5020-1EKA	PG-DSO-14-47-EP	BTS5020-1EKA

Diagnostic Functions

- Proportional load current sense
- Open load in ON and OFF
- Short circuit to battery and ground
- Overtemperature
- Stable diagnostic signal during short circuit
- Enhanced k_{ILIS} dependency with temperature and load current

Protection Functions

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during logic ground disconnect with external components
- Overtemperature protection with restart
- Overvoltage protection with external components
- Voltage dependent current limitation
- Enhanced short circuit operation

2 Block Diagram

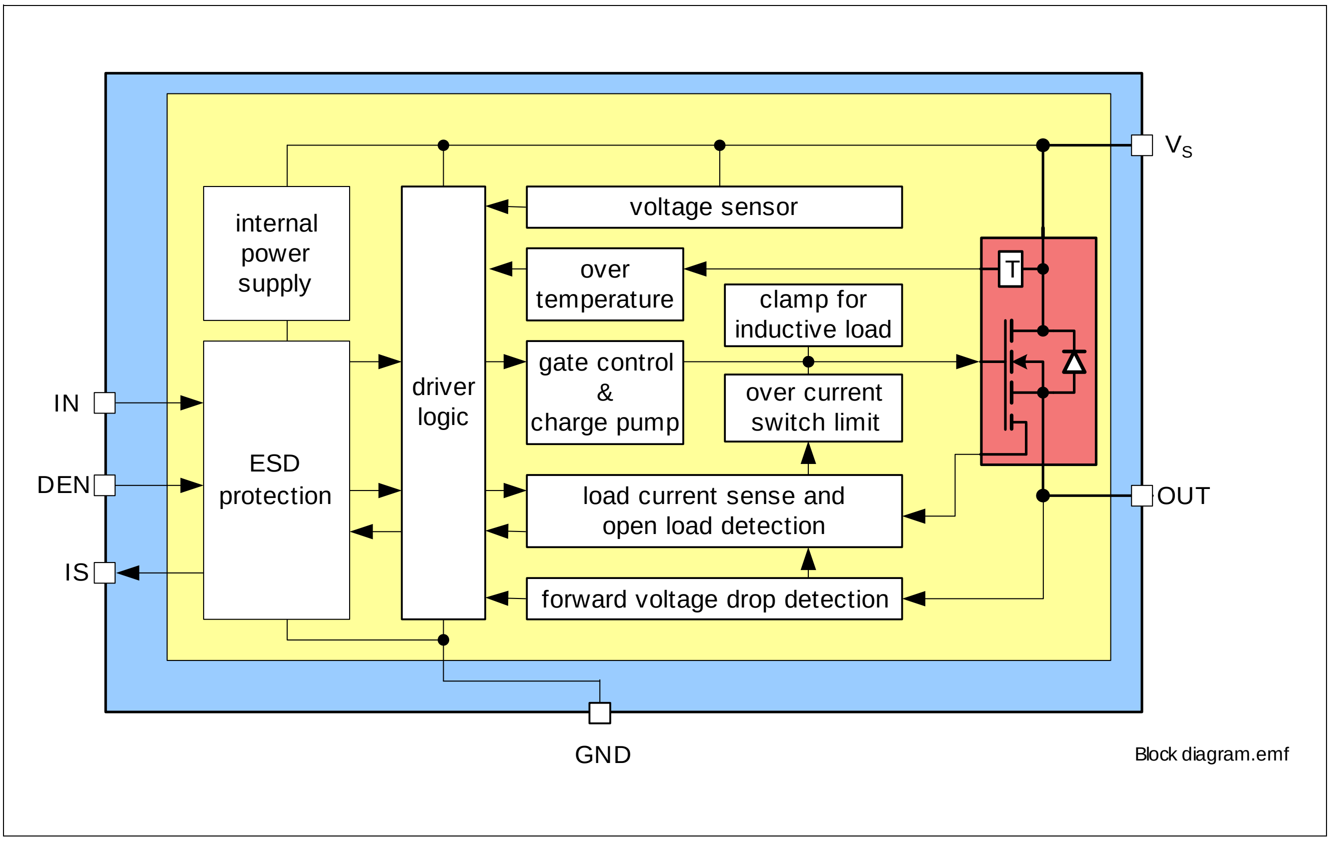


Figure 1 Block Diagram for the BTS5020-1EKA

3 Pin Configuration

3.1 Pin Assignment

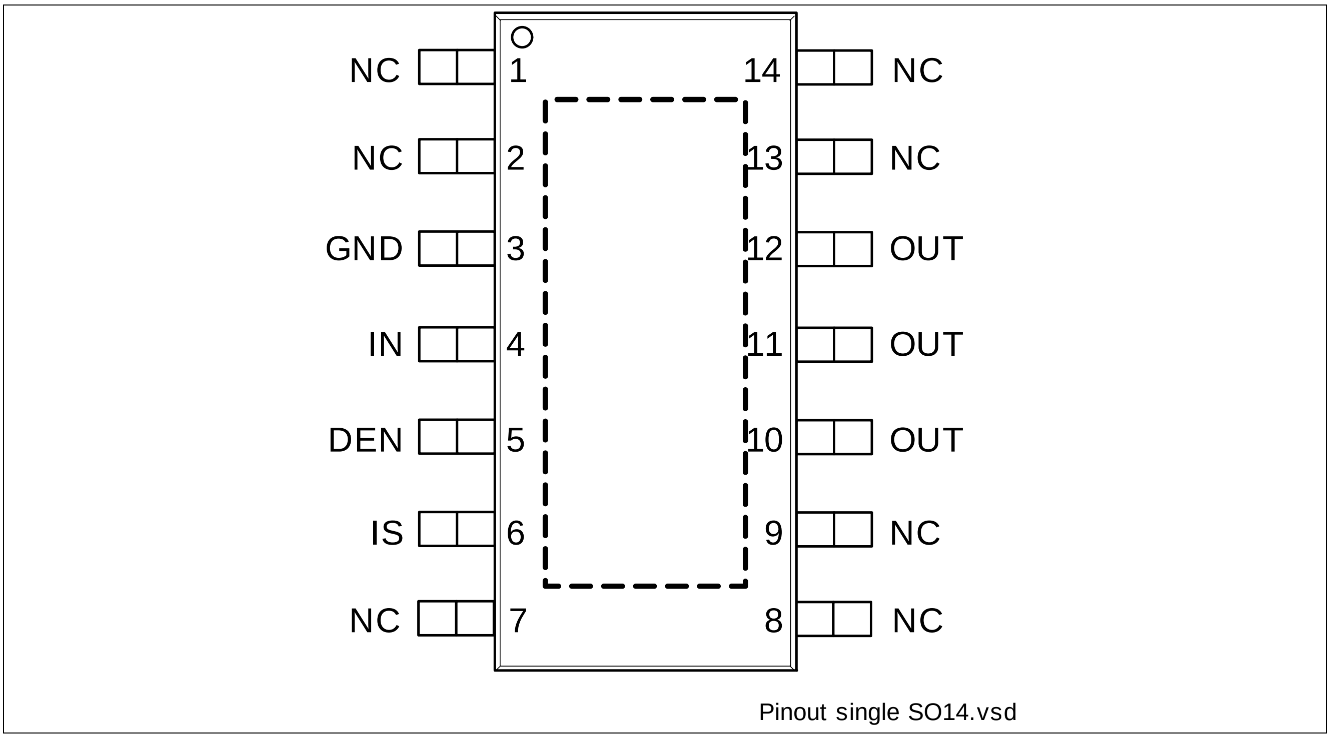


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
Cooling Tab	V_S	**Voltage Supply;** Battery voltage
1, 2, 7, 8, 9, 13, 14	NC	**Not Connected;** No internal connection to the chip
3	GND	**GrouND;** Ground connection
4	IN	**INput channel;** Input signal for channel activation
5	DEN	**Diagnostic ENable;** Digital signal to enable/disable the diagnosis of the device
6	IS	**Sense;** Sense current of the selected channel
10, 11, 12	OUT	**OUTput;** Protected high side power output channel[1]

[1] All output pins must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

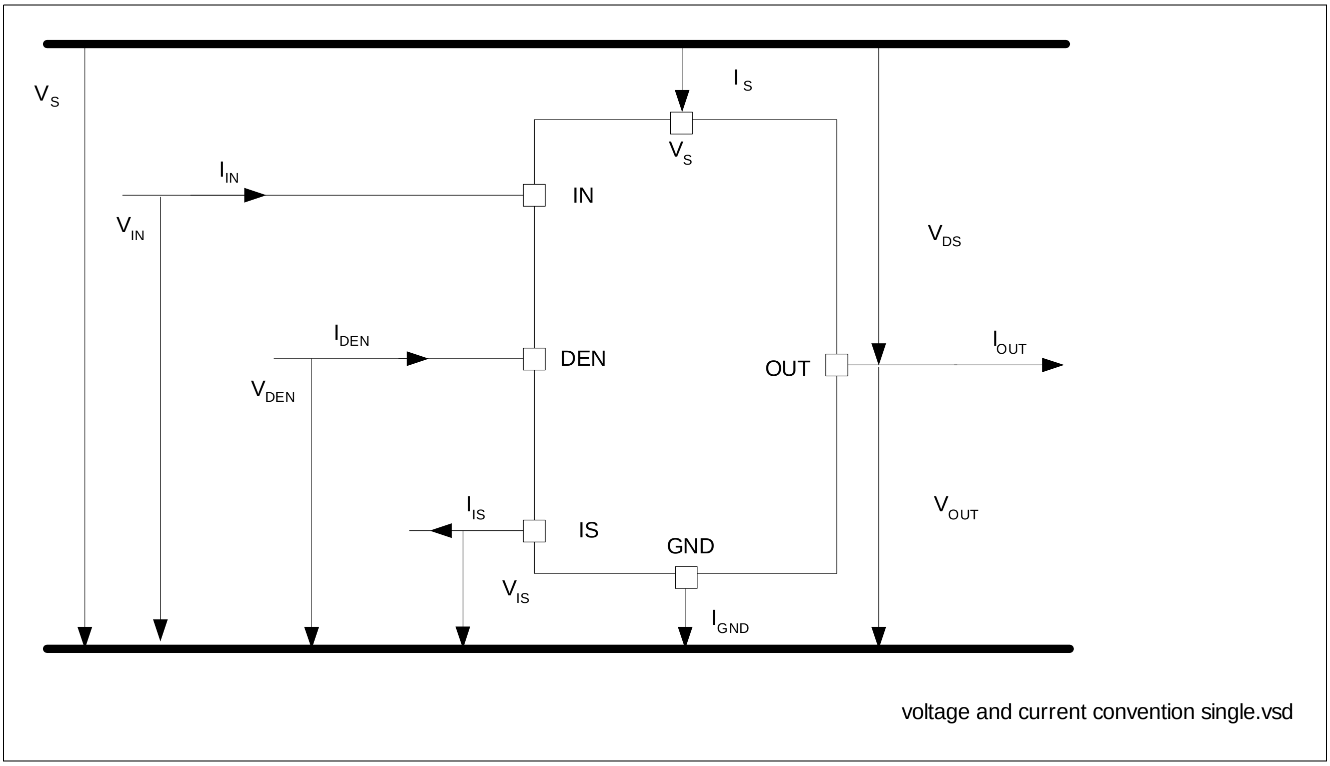


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply voltage	V_S	-0.3	–	28	V	–	P_4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	16	V	t < 2 min T_A = 25 °C $R_L \geq 4\ \Omega$ R_{GND} = 150 Ω	P_4.1.2
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	24	V	[2)] R_{ECU} = 20 mΩ R_{Cable}= 16 mΩ/m L_{Cable}= 1 µH/m, l = 0 or 5 m See **Chapter 6** and **Figure 52**	P_4.1.3
Supply voltage for Load dump protection	$V_{S(LD)}$	–	–	41	V	[3)] R_I = 2 Ω R_L = 4 Ω	P_4.1.12
Short Circuit Capability							
Permanent short circuit IN pin toggles	n_{RSC1}	–	–	100	k cycles	[4)] t_{ON} = 300ms	P_4.1.4
Input Pins							
Voltage at INPUT pin	V_{IN}	-0.3 –	–	6 7	V	– t < 2 min	P_4.1.13
Current through INPUT pin	I_{IN}	-2	–	2	mA	–	P_4.1.14
Voltage at DEN pin	V_{DEN}	-0.3 –	–	6 7	V	– t < 2 min	P_4.1.15
Current through DEN pin	I_{DEN}	-2	–	2	mA	–	P_4.1.16
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	P_4.1.19
Current through IS pin	I_{IS}	-25	–	50	mA	–	P_4.1.20
Power Stage							
Load current	$\|I_L\|$	–	–	$I_{L(LIM)}$	A	–	P_4.1.21
Power dissipation (DC)	P_{TOT}	–	–	1.8	W	T_A = 85 °C T_J < 150 °C	P_4.1.22
Maximum energy dissipation Single pulse	E_{AS}	–	–	90	mJ	$I_{L(0)}$ = 6 A $T_{J(0)}$ = 150 °C V_S = 13.5 V	P_4.1.23
Voltage at power transistor	V_{DS}	–	–	41	V	–	P_4.1.26

Table 2 Absolute Maximum Ratings (cont'd)[1]

T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
Currents							
Current through ground pin	I_{GND}	-10 -150	–	10 20	mA	– t < 2 min	P_4.1.27
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.28
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.30
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	[5] HBM	P_4.1.31
ESD susceptibility OUT Pin vs. GND and V_S connected	V_{ESD}	-4	–	4	kV	[5] HBM	P_4.1.32
ESD susceptibility	V_{ESD}	-500	–	500	V	[6] CDM	P_4.1.33
ESD susceptibility pin (corner pins)	V_{ESD}	-750	–	750	V	[6] CDM	P_4.1.34

1) Not subject to production test. Specified by design.

2) Hardware set-up in accordance to AEC Q100-012 and AEC Q101-006.

3) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1.

4) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability on Page 55 of this document

5) ESD susceptibility HBM according to EIA/JESD 22-A 114B.

6) "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range T_J = -40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_{NOM}	8	13.5	18	V	–	P_4.2.1
Extended operating voltage	$V_{S(OP)}$	5	–	28	V	[2] V_{IN} = 4.5 V R_L = 4 Ω V_{DS} < 0.5 V See **Figure 15**	P_4.2.2
Minimum functional supply voltage	$V_{S(OP)\_MIN}$	3.8	4.3	5	V	[1] V_{IN} = 4.5 V R_L = 4 Ω From I_{OUT} = 0 A to V_{DS} < 0.5 V; See **Figure 15**	P_4.2.3
Undervoltage shutdown	$V_{S(UV)}$	3	3.5	4.1	V	[1] V_{IN} = 4.5 V V_{DEN} = 0 V R_L = 4 Ω From V_{DS} < 1 V; to I_{OUT} = 0 A See **Figure 15** See **Figure 30**	P_4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	850	–	mV	[2] –	P_4.2.13
Operating current channel active	I_{GND_1}	–	3.5	6	mA	V_{IN} = 5.5 V V_{DEN} = 5.5 V Device in $R_{DS(ON)}$ V_S = 18 V See **Figure 31**	P_4.2.5
Standby current for whole device with load (ambiente)	$I_{S(OFF)}$	–	0.1	0.5	µA	[1] V_S = 18 V V_{OUT} = 0 V V_{IN} floating V_{DEN} floating $T_J \leq 85$ °C See **Figure 32**	P_4.2.7
Maximum standby current for whole device with load	$I_{S(OFF)\_150}$	–	5	20	µA	V_S = 18 V V_{OUT} = 0 V V_{IN} floating V_{DEN} floating T_J = 150 °C See **Figure 32**	P_4.2.10
Standby current for whole device with load, diagnostic active	$I_{S(OFF\_DEN)}$	–	0.6	–	mA	[2] V_S = 18 V V_{OUT} = 0 V V_{IN} floating V_{DEN} = 5.5 V	P_4.2.8

1) Test at T_J = -40°C only

2) Not subject to production test. Specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to soldering point	R_{thJS}	–	5	–	K/W	[1]	P_4.3.1
Junction to ambient	R_{thJA}	–	30	–	K/W	[1] [2]	P_4.3.2

1) Not subject to production test. Specified by design.

2)Specified R_{thja} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to **Figure 4** and **Figure 5**.

4.3.1 PCB set up

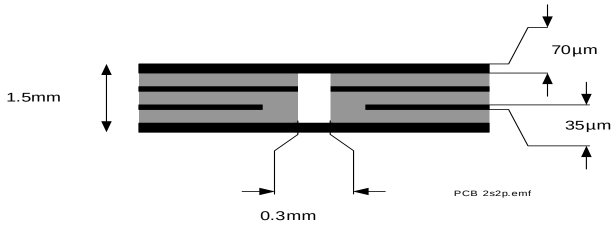


Figure 4 2s2p PCB Cross Section

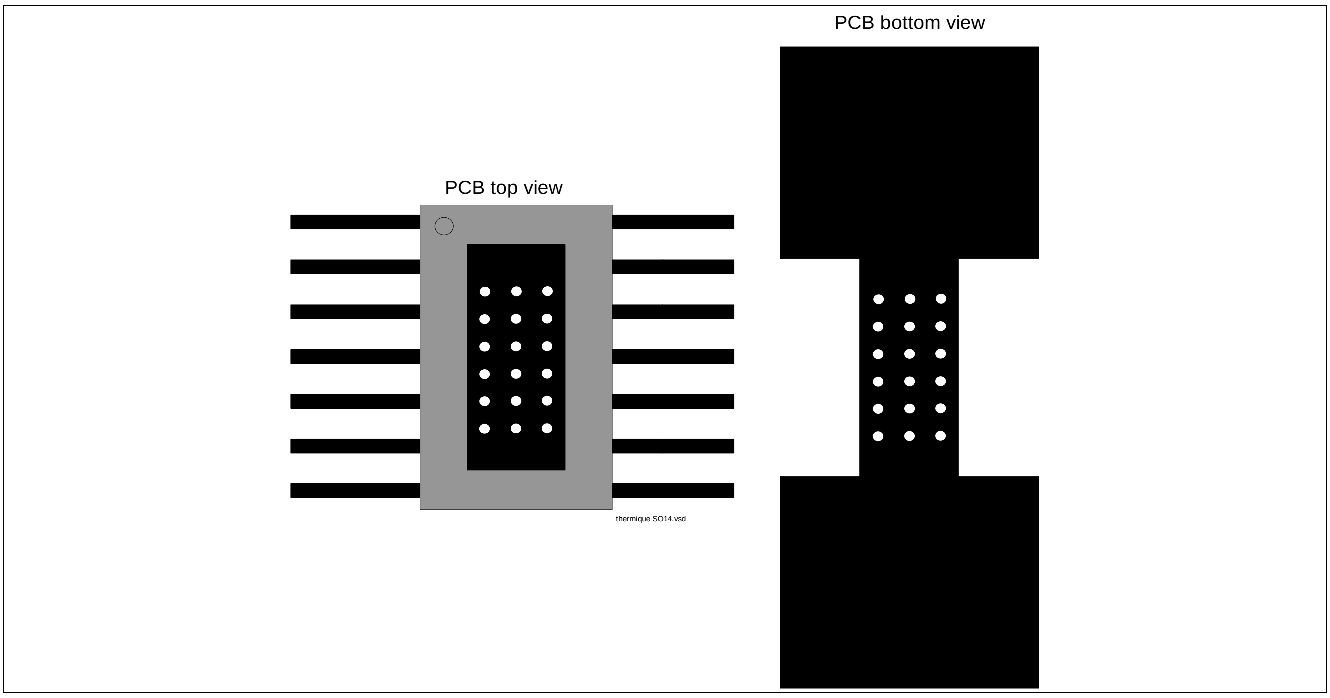


Figure 5 PC Board Top and Bottom View for Thermal Simulation with 600 mm² Cooling Area

4.3.2 Thermal Impedance

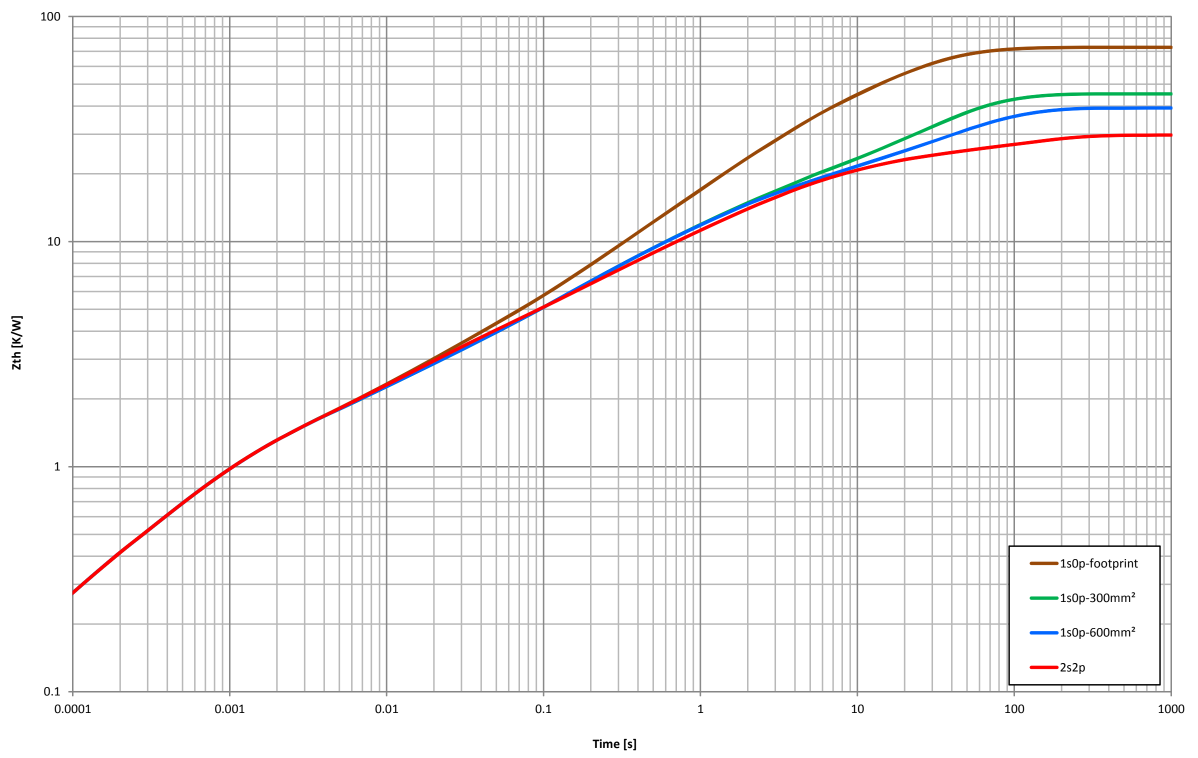


Figure 6 Typical Thermal Impedance. PCB set up according Figure 5

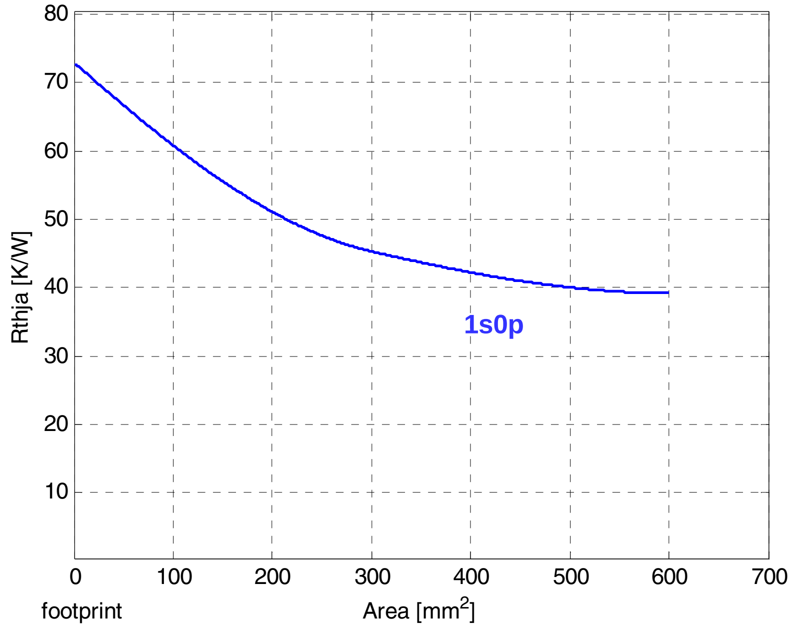


Figure 7 **Typical Thermal Resistance. PCB set up 1s0p**

5 Power Stage

The power stage is built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-state Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J. **Figure 8** shows the dependencies in terms of temperature and supply voltage for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

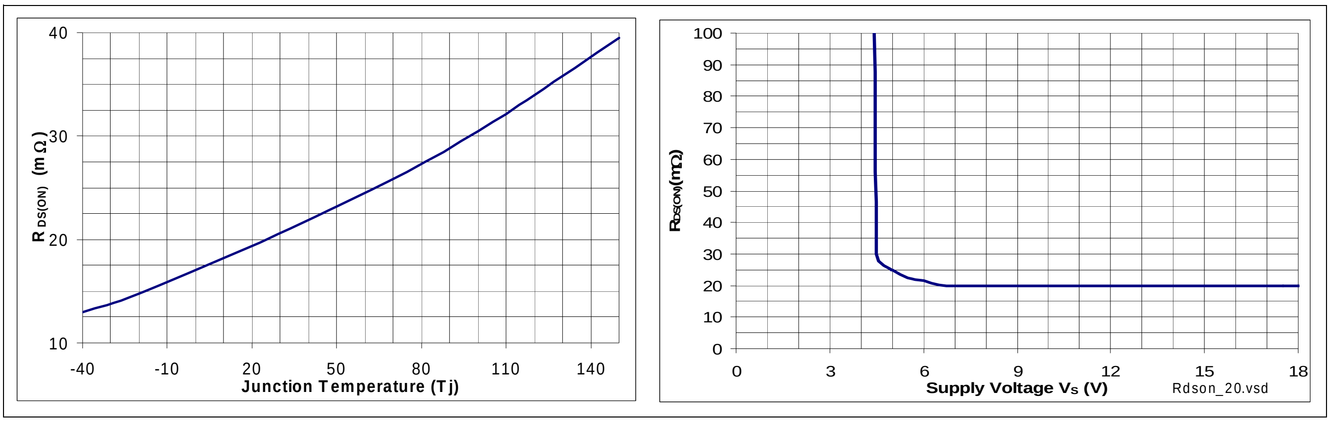


Figure 8 Typical ON-state Resistance

A high signal at the input pin (see **Chapter 8**) causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn ON/OFF Characteristics with Resistive Load

Figure 9 shows the typical timing when switching a resistive load.

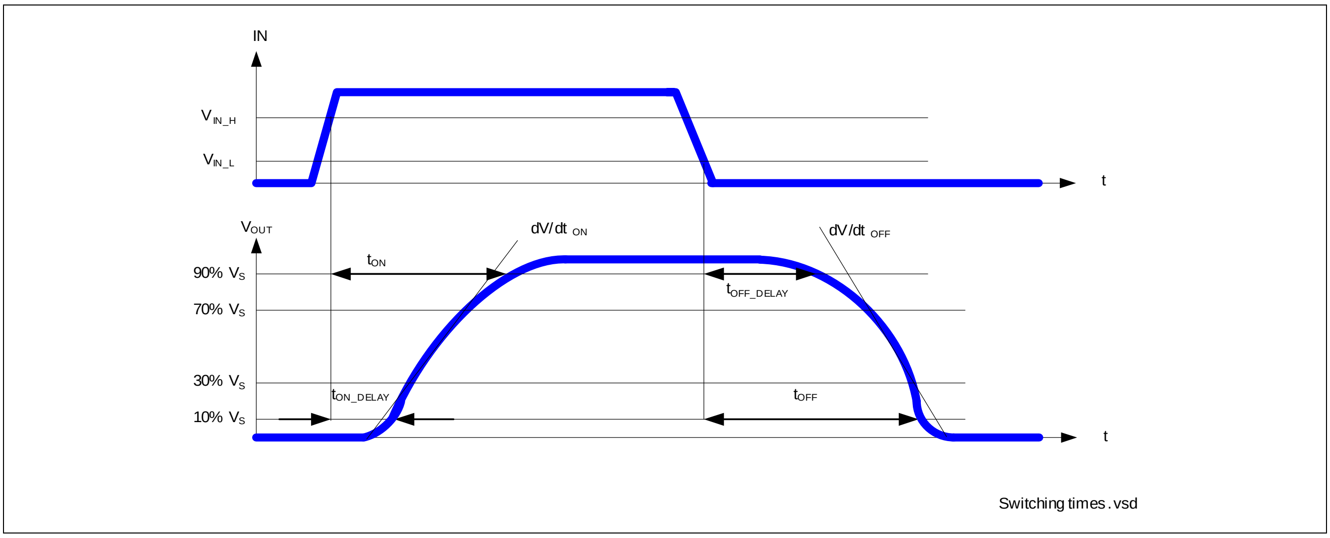


Figure 9 Switching a Resistive Load Timing

5.3 Inductive Load

5.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(AZ)}$ implemented that limits negative output voltage to a certain level (V_S - $V_{DS(AZ)}$). Please refer to **Figure 10** and **Figure 11** for details. Nevertheless, the maximum allowed load inductance is limited.

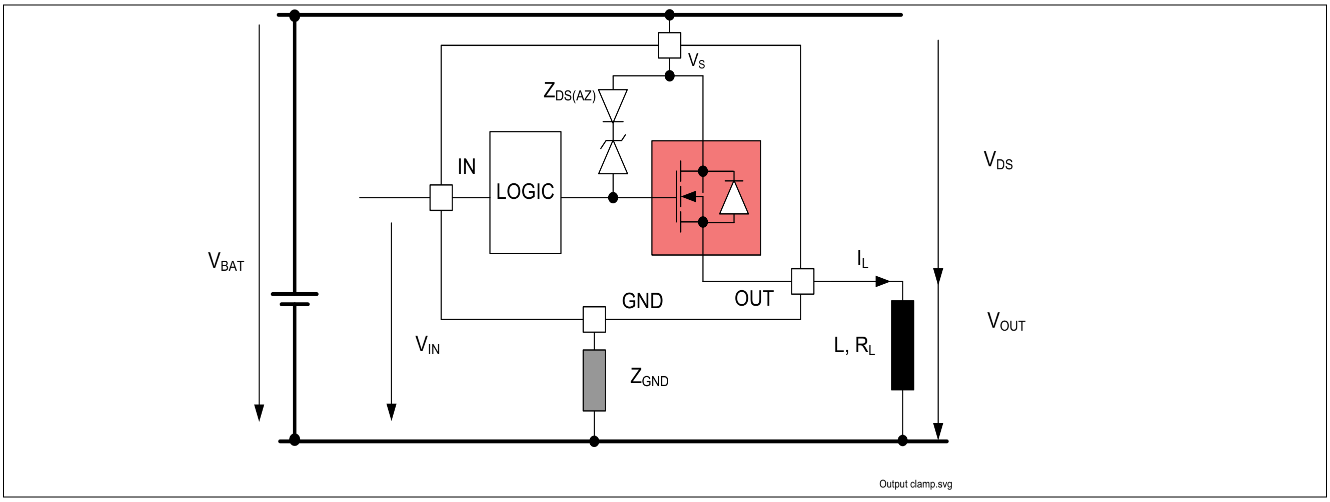


Figure 10 Output Clamp

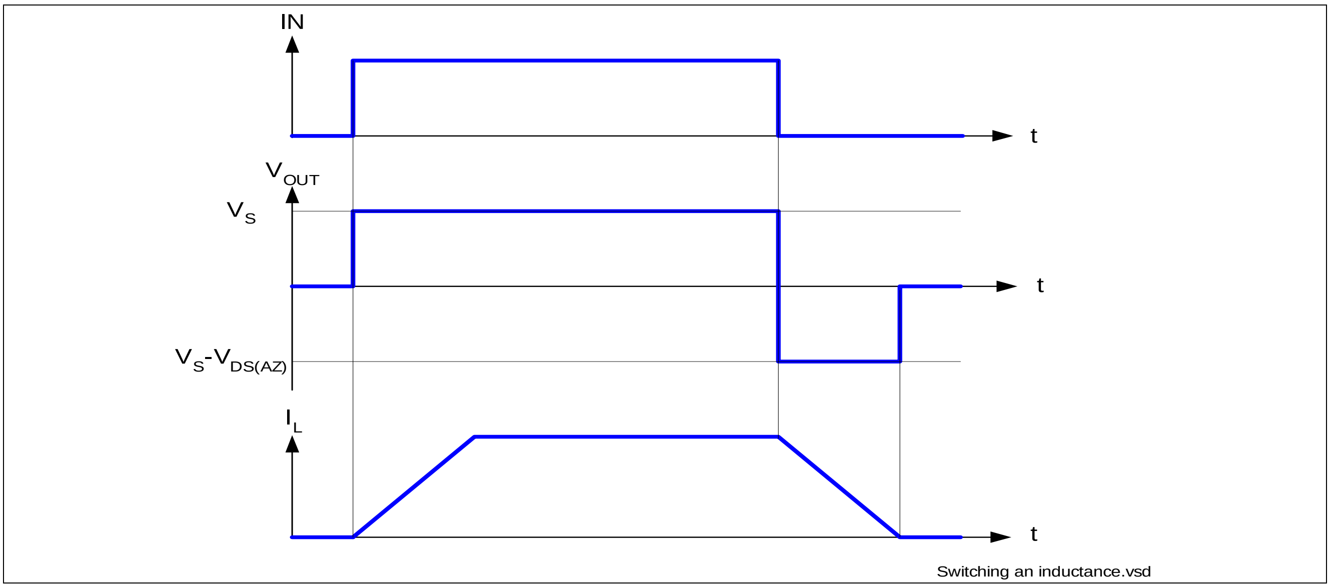


Figure 11 Switching an Inductive Load Timing

5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTS5020-1EKA. This energy can be calculated with following equation:

$$E = V_{\mathrm{DS(AZ)}} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{\mathrm{DS(AZ)}}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{\mathrm{DS(AZ)}}}\right) + I_L \right] \tag{1}$$

Following equation simplifies under the assumption of $R_L = 0\ \Omega$.

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{\mathrm{DS(AZ)}}}\right) \tag{2}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 12** for the maximum allowed energy dissipation as a function of the load current.

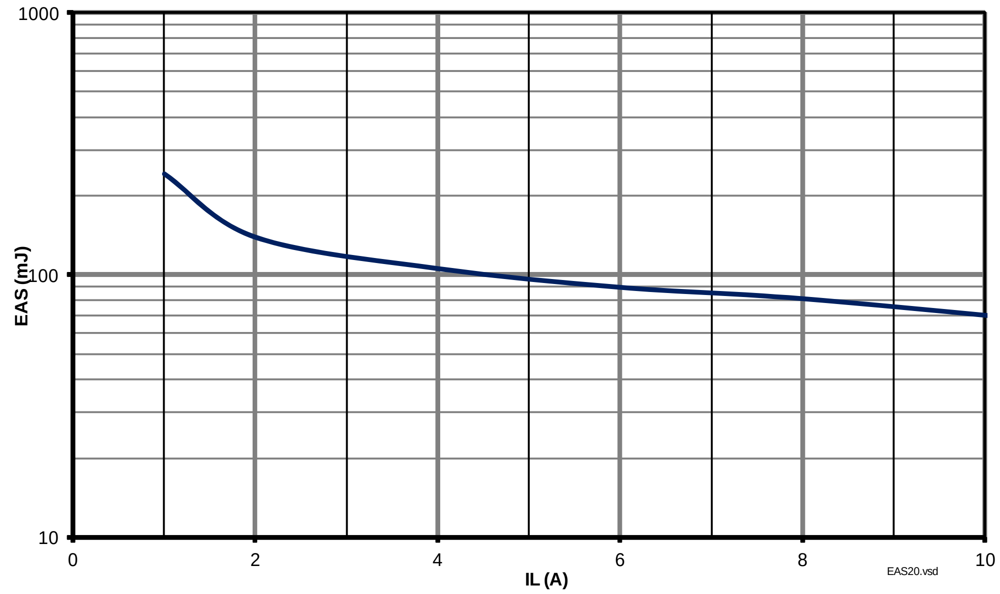


Figure 12 Maximum Energy Dissipation Single Pulse, $T_{\mathrm{J\_START}}$ = 150 °C; V_S = 13.5V

5.4 Inverse Current Capability

In case of inverse current, meaning a voltage V_{INV} at the OUTput higher than the supply voltage V_S, a current I_{INV} will flow from output to V_S pin via the body diode of the power transistor (please refer to **Figure 13**). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse. In that particular case, the output stage is kept OFF until the inverse current disappears. If the channel is OFF, the diagnostic will detect an open load at OFF. If the channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of V_{INV}, a parasitic diagnostic can be observed. After, the diagnosis is valid and reflects the output state. At V_{INV} vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection functions are available.

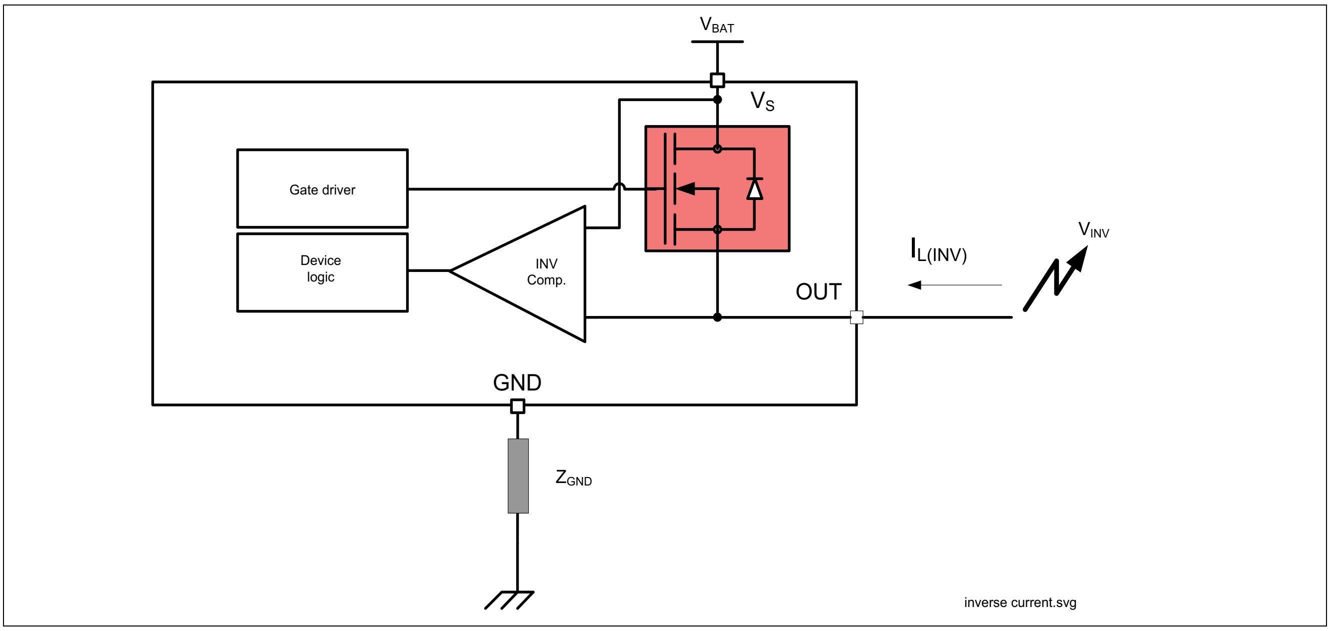


Figure 13 Inverse Current Circuitry

5.5 Electrical Characteristics Power Stage

Table 5 Electrical Characteristics: Power Stage

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance per channel	$R_{DS(ON)\_150}$	33	40	44	mΩ	$I_L = I_{L4}$ = 7 A V_{IN} = 4.5 V T_J = 150 °C See **Figure 8**	P_5.5.1
ON-state resistance per channel	$R_{DS(ON)\_25}$	–	20	–	mΩ	[1] T_J = 25 °C	P_5.5.21
Nominal load current	$I_{L(NOM)}$	–	6.5	–	A	[1] T_A= 85 °C T_J < 150 °C	P_5.5.2
Output voltage drop limitation at small load currents	$V_{DS(NL)}$	–	10	25	mV	$I_L = I_{L0}$ = 50 mA See **Figure 33**	P_5.5.4
Drain to source clamping voltage $V_{DS(AZ)} = [V_S - V_{OUT}]$	$V_{DS(AZ)}$	41	47	53	V	I_{DS} = 20 mA See **Figure 11** See **Figure 34**	P_5.5.5
Output leakage current$T_J \leq$ 85 °C	$I_{L(OFF)}$	–	0.1	0.5	µA	[2] V_{IN} floating V_{OUT} = 0 V $T_J \leq$ 85 °C	P_5.5.6
Output leakage currentT_J = 150 °C	$I_{L(OFF)\_150}$	–	2.5	10	µA	V_{IN} floating V_{OUT} = 0 V T_J = 150 °C	P_5.5.8
Inverse current capability	$I_{L(INV)}$	–	5	–	A	[1] $V_S < V_{OUT}$	P_5.5.9
Slew rate 30% to 70% V_S	dV/dt_{ON}	0.1	0.25	0.5	V/µs	R_L = 4 Ω V_S = 13.5 V See **Figure 9** See **Figure 35** See **Figure 36** See **Figure 37** See **Figure 38** See **Figure 39**	P_5.5.11
Slew rate 70% to 30% V_S	$-dV/dt_{OFF}$	0.1	0.25	0.5	V/µs		P_5.5.12
Slew rate matching $dV/dt_{ON} - dV/dt_{OFF}$	$\Delta dV/dt$	-0.15	0	0.15	V/µs		P_5.5.13
Turn-ON time to V_{OUT} = 90% V_S	t_{ON}	30	90	230	µs		P_5.5.14
Turn-OFF time to V_{OUT} = 10% V_S	t_{OFF}	30	90	230	µs		P_5.5.15
Turn-ON / OFF matching $t_{OFF} - t_{ON}$	Δt_{SW}	-50	0	50	µs		P_5.5.16
Turn-ON time to V_{OUT} = 10% V_S	t_{ON_delay}	10	35	100	µs		P_5.5.17
Turn-OFF time to V_{OUT} = 90% V_S	t_{OFF_delay}	10	35	100	µs		P_5.5.18

Table 5 Electrical Characteristics: Power Stage (cont'd)

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
Switch ON energy	E_{ON}	–	1	–	mJ	[1] $R_L = 4\ \Omega$ V_{OUT} = 90% V_S V_S = 18 V See **Figure 40**	P_5.5.19
Switch OFF energy	E_{OFF}	–	0.9	–	mJ	[1] $R_L = 4\ \Omega$ V_{OUT} = 10% V_S V_S = 18 V See **Figure 41**	P_5.5.20

1) Not subject to production test, specified by design.

2) Test at T_J = -40°C only

6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pin.

In case of loss of device ground, it’s recommended to use input resistors between the microcontroller and the BTS5020-1EKA to ensure switching OFF of channel.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS. **Figure 14** sketches the situation.

Z_{GND} can be either resistor or diode.

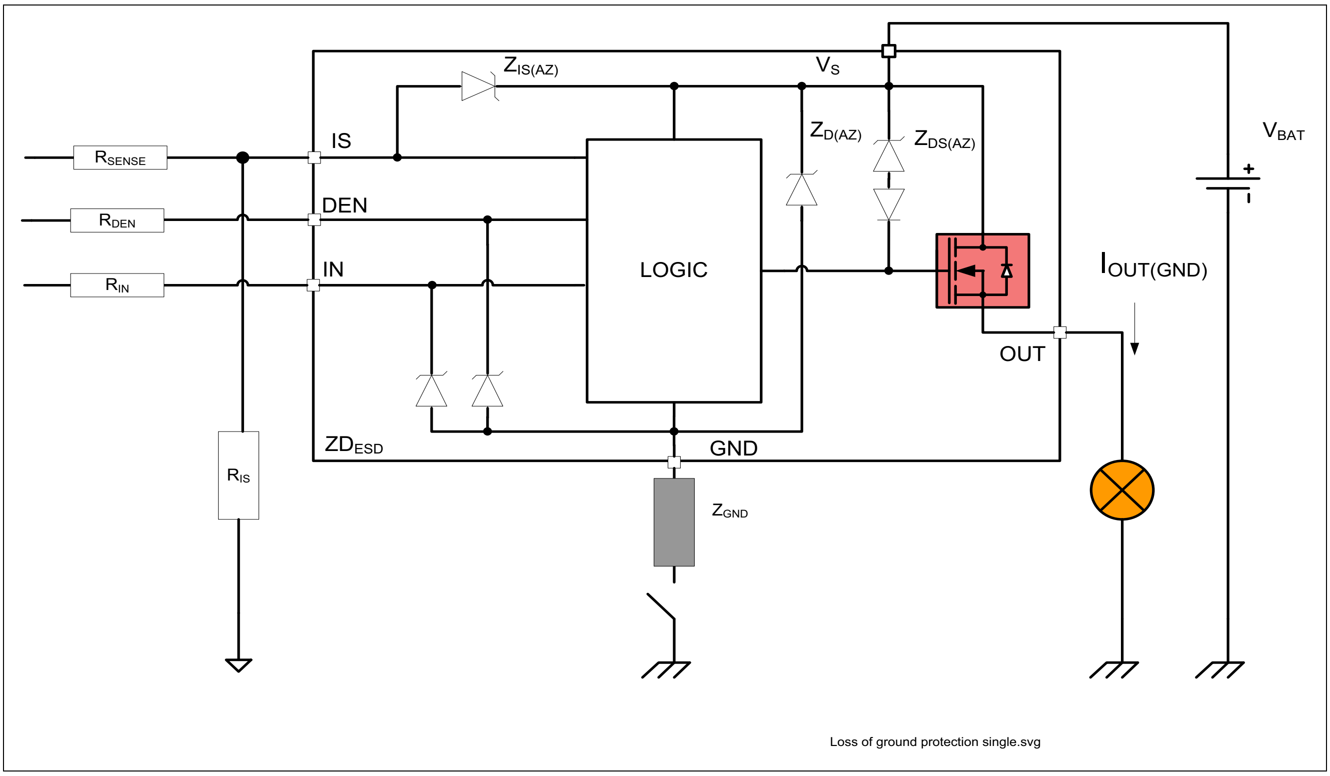


Figure 14 Loss of Ground Protection with External Components

6.2 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can takes place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the V_{NOM} range. **Figure 15** sketches the undervoltage mechanism.

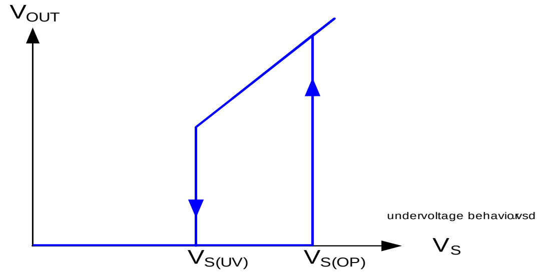


Figure 15 Undervoltage Behavior

6.3 Overvoltage Protection

There is an integrated clamp mechanism for overvoltage protection ($Z_{D(AZ)}$). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. **Figure 16** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the power transistor switches ON and the voltage across the logic section is clamped. As a result, the internal ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin IN and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTS5020-1EKA remains ON. In the case the BTS5020-1EKA was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{BAT(SC)}$ and below $V_{DS(AZ)}$, the output transistor is still operational and follows the input. If the channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability. Z_{GND} as a resistor (150 Ω) will offer superior results compared to a diode and resistor (1 kΩ).

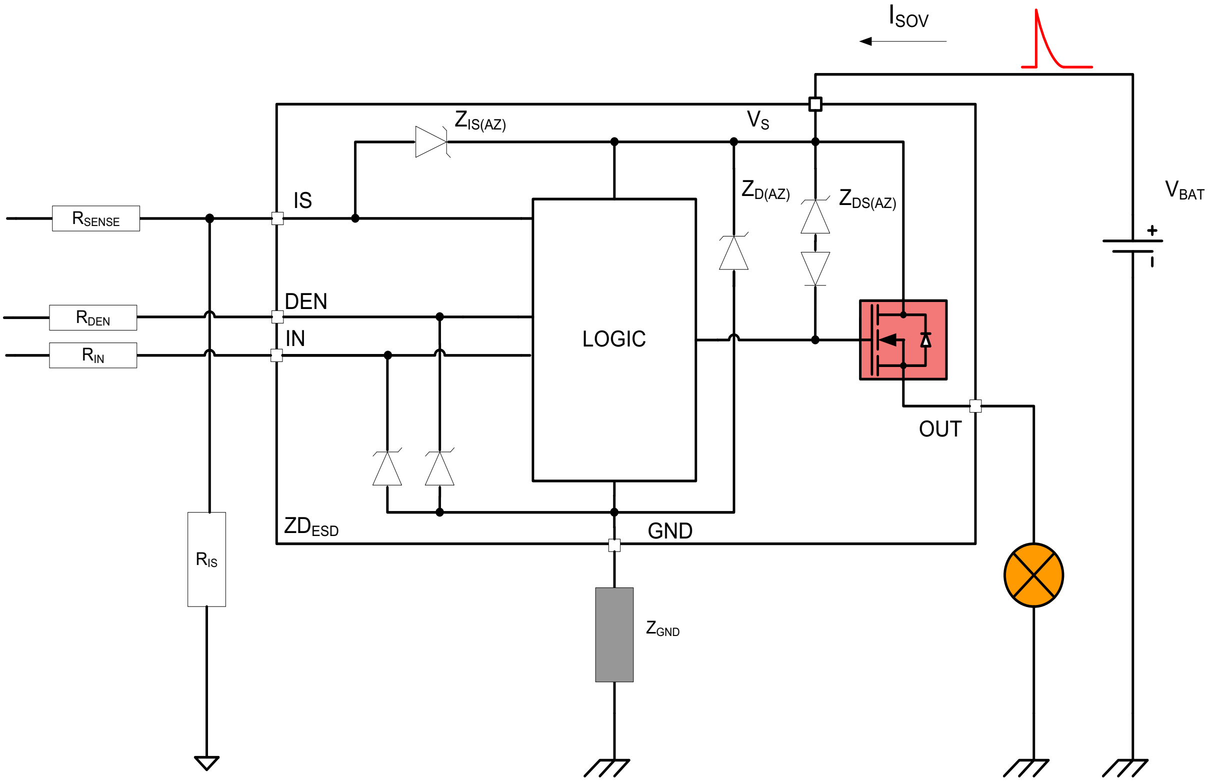


Figure 16 Overvoltage Protection with External Components

6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in **Chapter 4.1** with an external resistor. **Figure 17** shows a typical application. R_{GND} resistor is used to limit the current in the Zener protection of the device. Resistors R_{DEN} and R_{IN} are used to limit the current in the logic of the device and in the ESD protection stage. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode. The recommended value for $R_{DEN} = R_{IN} = R_{SENSE}$ = 4.7 kΩ. Z_{GND} can be either a 150 Ω resistor or Schottky diode with 1 kΩ resistor in parallel.

In case the overvoltage is not considered in the application, R_{GND} can be replaced by a Schottky diode and 1kΩ resistor in parallel. Optionally a capacitor in parallel is recommended for EMC reasons.

During reverse polarity, no protection functions are available.

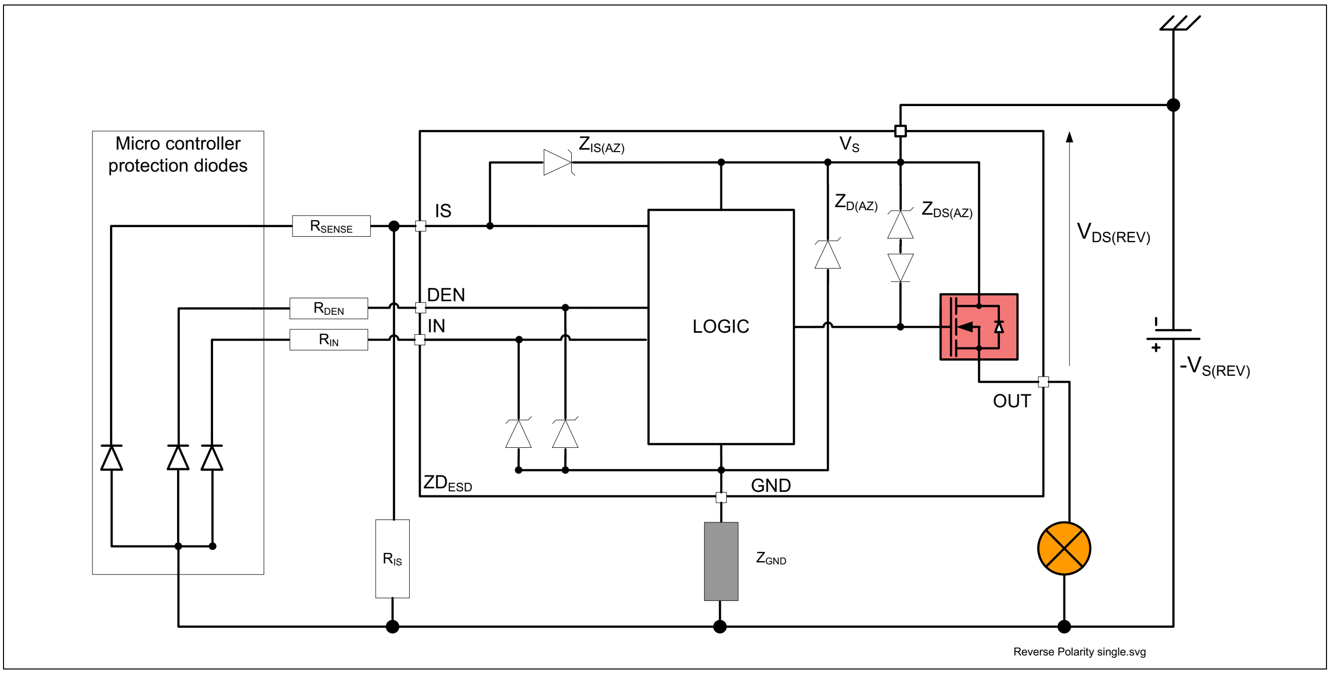


Figure 17 Reverse Polarity Protection with External Components

6.5 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTS5020-1EKA offers several protection mechanisms.

6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch $I_{L(SC)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS. The current limitation value is V_{DS} dependent. **Figure 18** shows the behavior of the current limitation as a function of the drain to source voltage.

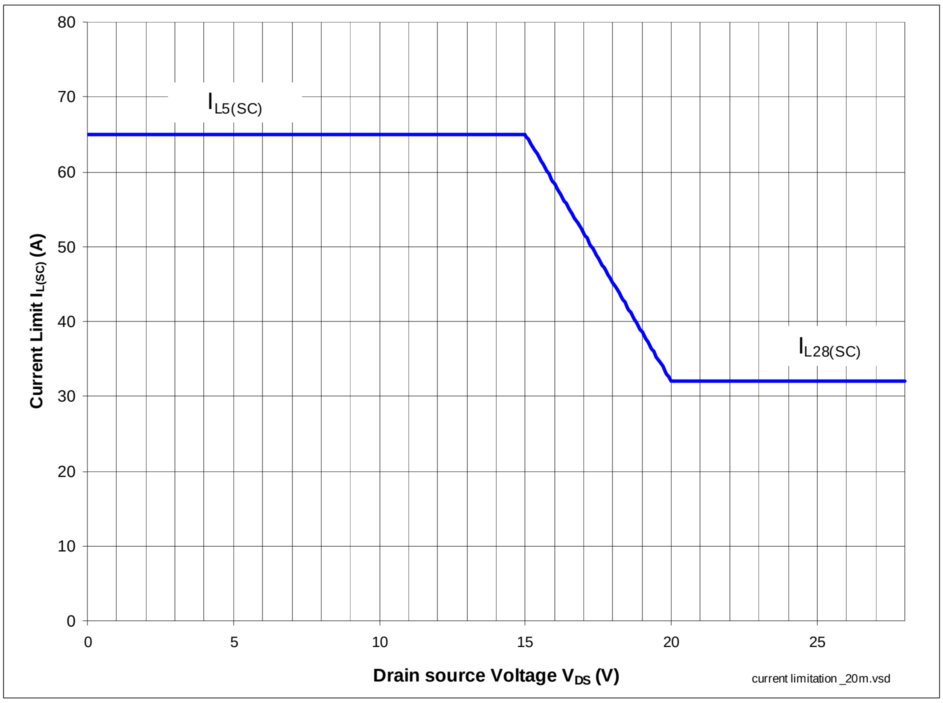


Figure 18 Current Limitation (typical behavior)

6.5.2 Temperature Limitation in the Power DMOS

The channel incorporates both an absolute ($T_{J(SC)}$) and a dynamic ($T_{J(SW)}$) temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value. **Figure 19** gives a sketch of the situation. The ΔT_{STEP} describes the device's warming, due to the overcurrent in the channel.

A retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again, if the IN pin signal is still high (restart behavior).

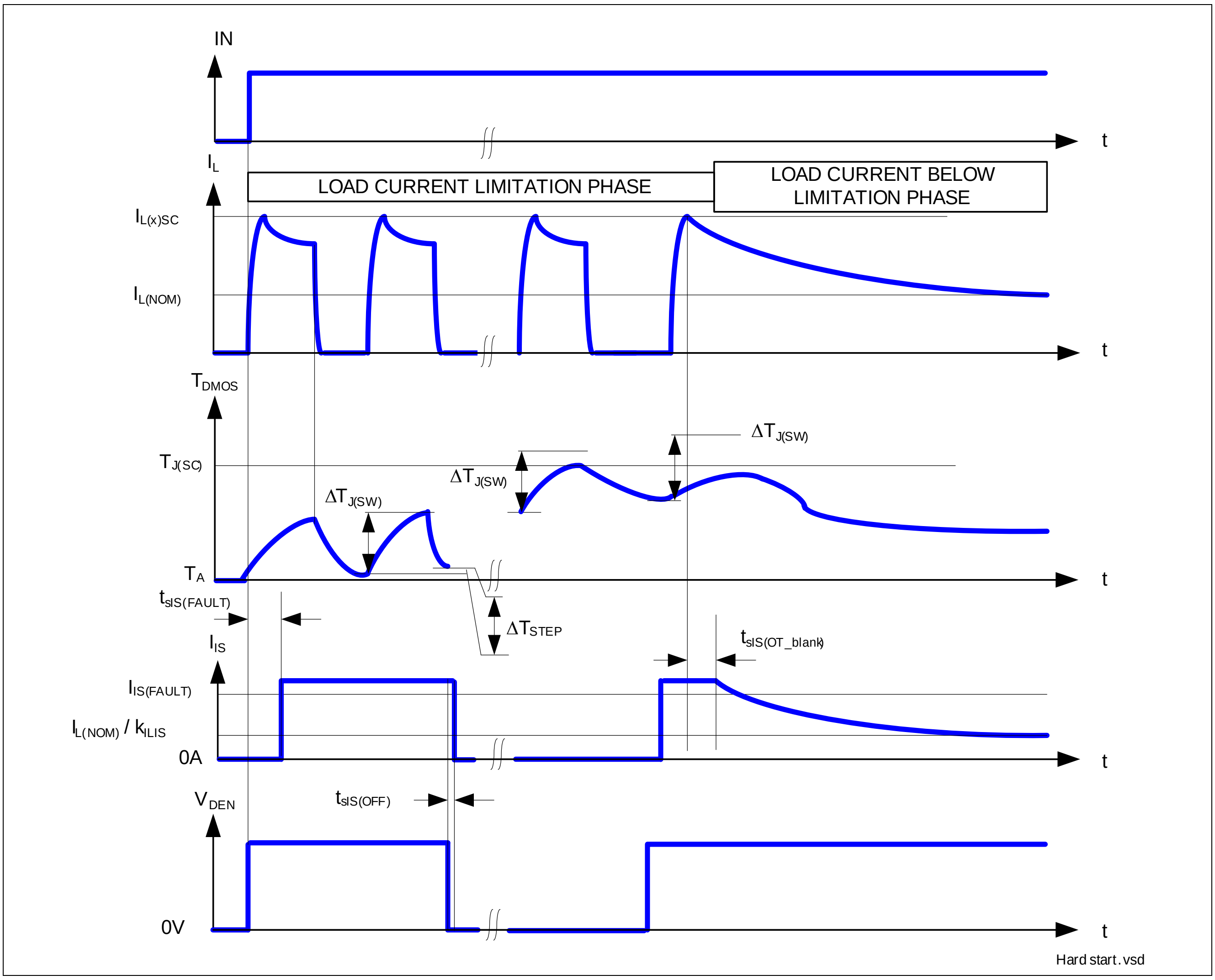


Figure 19 Overload Protection

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

6.6 Electrical Characteristics for the Protection Functions

Table 6 Electrical Characteristics: Protection

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	1) 2) V_S = 28 V See **Figure 14**	P_6.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	200	650	700	mV	I_L = - 4 A T_J = 150 °C See **Figure 17**	P_6.6.2
Overvoltage							
Overvoltage protection	$V_{S(AZ)}$	41	47	53	V	I_{SOV} = 5 mA See **Figure 16**	P_6.6.3
Overload Condition							
Load current limitation	$I_{L5(SC)}$	50	65	80	A	3) V_{DS} = 5 V See **Figure 18** See **Figure 42**	P_6.6.4
Load current limitation	$I_{L28(SC)}$	–	32	–	A	2) V_{DS} = 28 V See **Figure 18** See **Figure 43**	P_6.6.7
Short circuit current during over temperature toggling	$I_{L(RMS)}$	–	6.5	–	A	2) V_{IN} = 4.5 V R_{SHORT} = 100 mΩ L_{SHORT} = 5 µH	P_6.6.12
Dynamic temperature increase while switching	$\Delta T_{J(SW)}$	–	80	–	K	4) See **Figure 19**	P_6.6.8
Thermal shutdown temperature	$T_{J(SC)}$	150	170 4)	200 4)	°C	5) See **Figure 19**	P_6.6.10
Thermal shutdown hysteresis	$\Delta T_{J(SC)}$	–	20	–	K	5) 4) See **Figure 19**	P_6.6.11

1) All pins are disconnected except V_S and OUT.
2) Not Subject to production test, specified by design
3) Test at T_J = -40°C only
4) Functional test only
5) Test at T_J = +150°C only

7 Diagnostic Functions

For diagnosis purpose, the BTS5020-1EKA provides a combination of digital and analog signals at pin IS. These signals are called SENSE. In case the diagnostic is disabled via DEN, pin IS becomes high impedance. In case DEN is activated, the SENSE of the channel is enabled.

7.1 IS Pin

The BTS5020-1EKA provides a SENSE current written I_{IS} at pin IS. As long as no "hard" failure mode occurs (short circuit to GND / current limitation / overtemperature / excessive dynamic temperature increase or open load at OFF) a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$) is provided. The complete IS pin and diagnostic mechanism is described on **Figure 20**. The accuracy of the SENSE depends on temperature and load current.

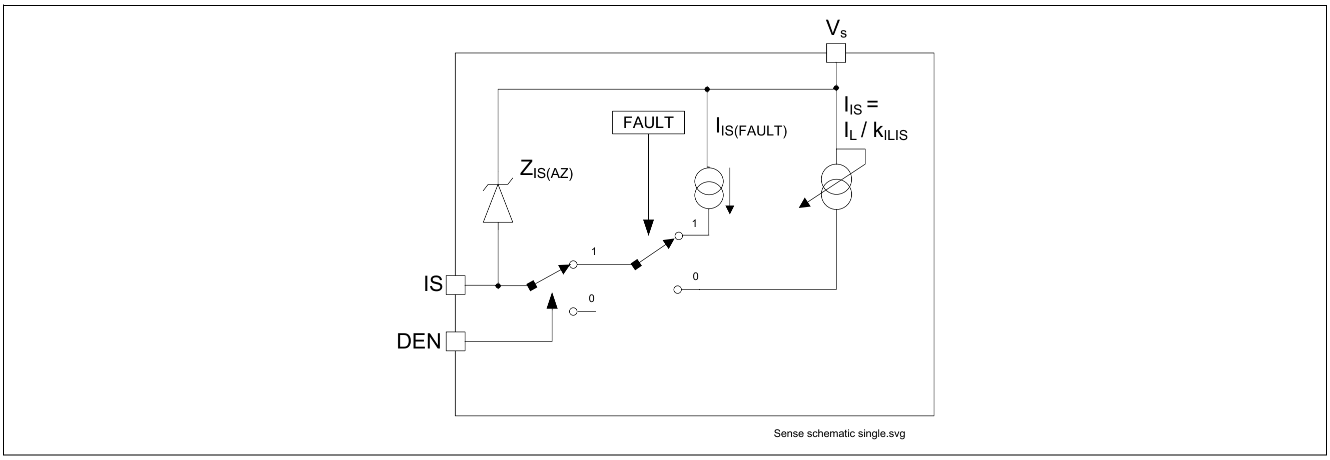


Figure 20 Diagnostic Block Diagram

7.2 SENSE Signal in Different Operating Modes

Table 7 gives a quick reference for the state of the IS pin during device operation.

Table 7 Sense Signal, Function of Operation Mode

Operation Mode	Input level Channel X	DEN	Output Level	Diagnostic Output
Normal operation	OFF	H	Z	Z
Short circuit to GND			~ GND	Z
Overtemperature			Z	Z
Short circuit to V_S			V_S	$I_{IS(FAULT)}$
Open Load			$< V_{OL(OFF)}$ $> V_{OL(OFF)}$ 1)	Z $I_{IS(FAULT)}$
Inverse current			$\sim V_{INV}$	$I_{IS(FAULT)}$
Normal operation	ON		$\sim V_S$	$I_{IS} = I_L / k_{ILIS}$
Current limitation			$< V_S$	$I_{IS(FAULT)}$
Short circuit to GND			~ GND	$I_{IS(FAULT)}$
Overtemperature $T_{J(SW)}$ event			Z	$I_{IS(FAULT)}$
Short circuit to V_S			V_S	$I_{IS} < I_L / k_{ILIS}$
Open Load			$\sim V_S$ 2)	$I_{IS} < I_{IS(OL)}$
Inverse current			$\sim V_{INV}$	$I_{IS} < I_{IS(OL)}$ 3)
Underload			$\sim V_S$ 4)	$I_{IS(OL)} < I_{IS} < I_{L(NOM)} / k_{ILIS}$
Don't care	Don't care	L	Don't care	Z

1) With additional pull-up resistor.

2) The output current has to be smaller than $I_{L(OL)}$.

3) After maximum t_{INV}.

4) The output current has to be higher than $I_{L(OL)}$.

7.3 SENSE Signal in the Nominal Current Range

Figure 21 and **Figure 22** show the current sense as a function of the load current in the power DMOS. Usually, a pull-down resistor R_{IS} is connected to the IS pin. This resistor has to be higher than 560 Ω to limit the power losses in the sense circuitry. A typical value is 1.2 kΩ. The blue curve represents the ideal SENSE, assuming an ideal k_{ILIS} factor value. The red curves show the accuracy the device provides across full temperature range, at a defined current.

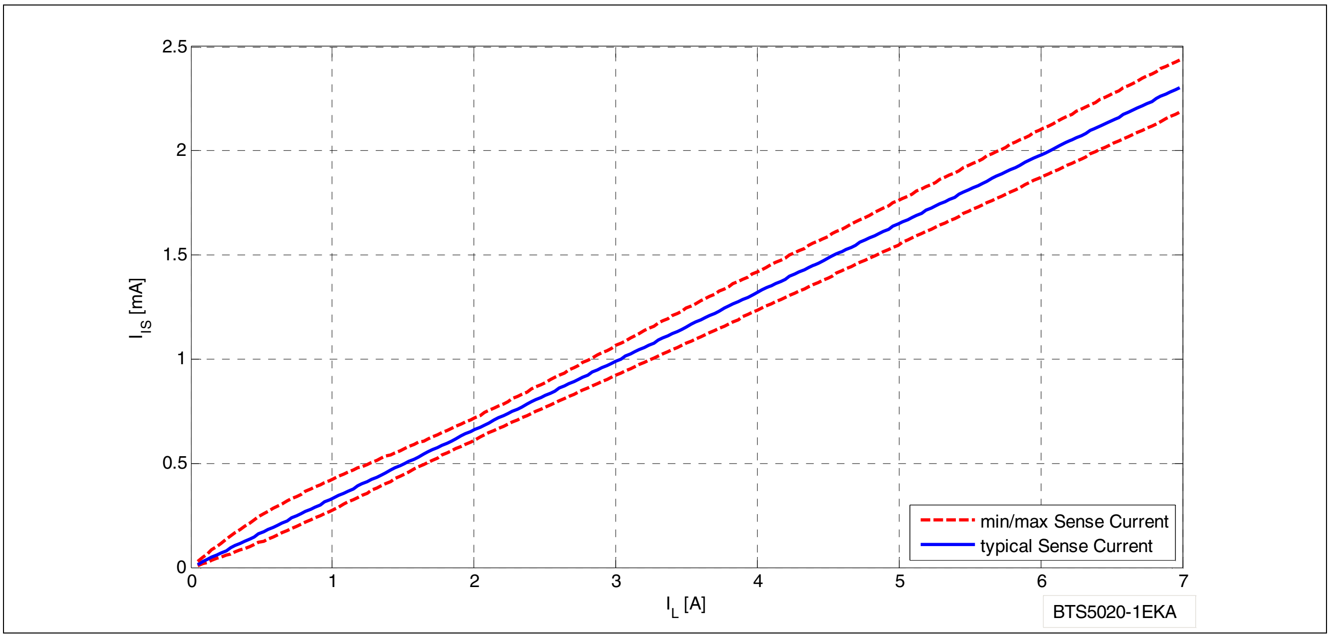


Figure 21 Current Sense for Nominal Load

7.3.1 SENSE Signal Variation as a Function of Temperature and Load Current

In some applications a better accuracy is required around half the nominal current $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. To avoid multiple calibration points at different load and temperature conditions, the BTS5020-1EKA allows limited derating of the k_{ILIS} value, at a given point (I_{L3}; T_J = +25 °C). This derating is described by the parameter Δk_{ILIS}. **Figure 22** shows the behavior of the SENSE current, assuming one calibration point at nominal load at +25 °C.

The blue line indicates the ideal k_{ILIS} ratio.

The green lines indicate the derating on the parameter across temperature and voltage, assuming one calibration point at nominal temperature and nominal battery voltage.

The red lines indicate the k_{ILIS} accuracy without calibration.

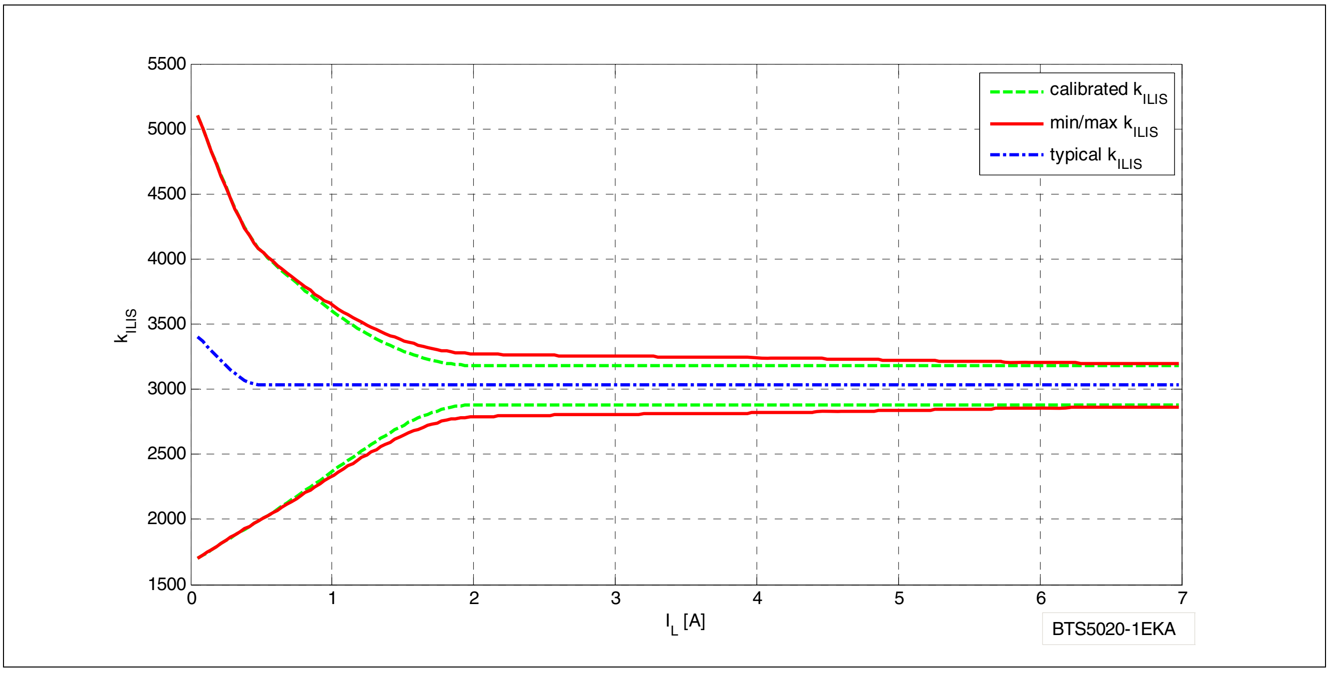


Figure 22 Improved Current SENSE Accuracy with One Calibration Point at 2A

7.3.2 SENSE Signal Timing

Figure 23 shows the timing during settling and disabling of the SENSE.

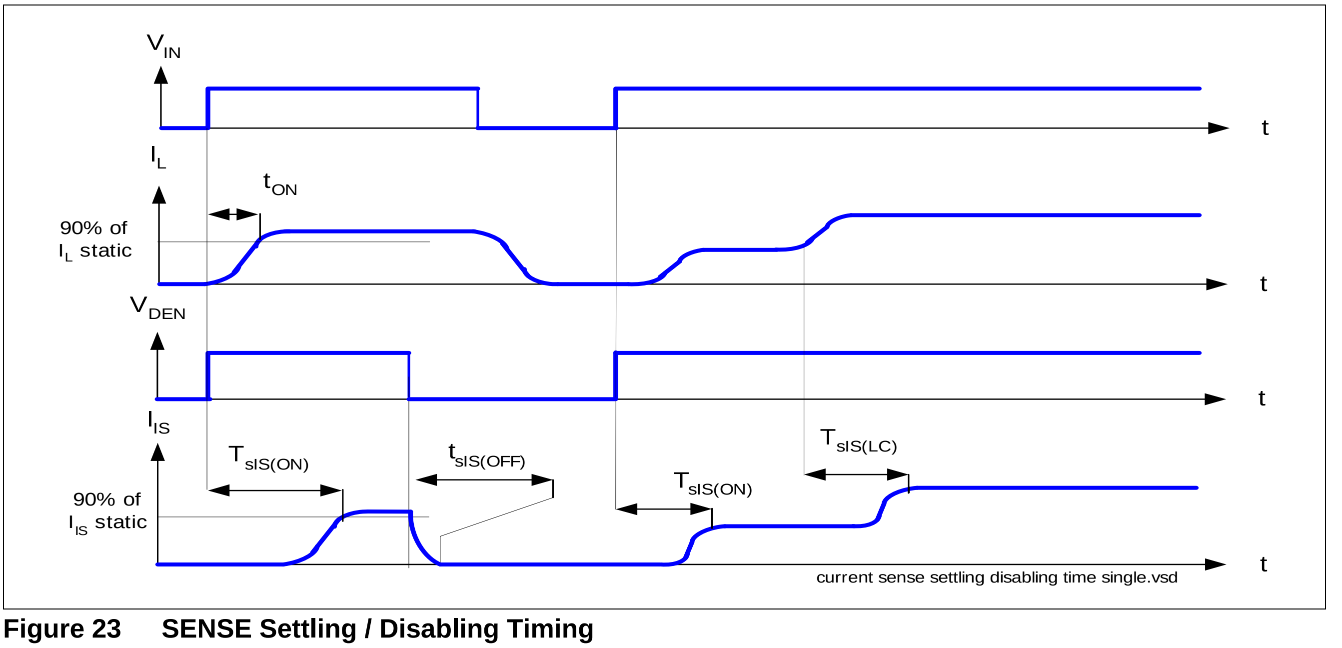


Figure 23 SENSE Settling / Disabling Timing

7.3.3 SENSE Signal in Open Load

7.3.3.1 Open Load in ON Diagnostic

If the channel is ON, a leakage current can still flow through an open load, for example due to humidity. The parameter $I_{L(OL)}$ gives the threshold of recognition for this leakage current. If the current I_L flowing out the power DMOS is below this value, the device recognizes a failure, if the DEN is selected. In that case, the SENSE current is below $I_{IS(OL)}$. Otherwise, the minimum SENSE current is given above parameter $I_{IS(OL)}$. **Figure 24** shows the SENSE current behavior in this area. The red curve shows a typical product curve. The blue curve shows the ideal k_{ILIS} ratio.

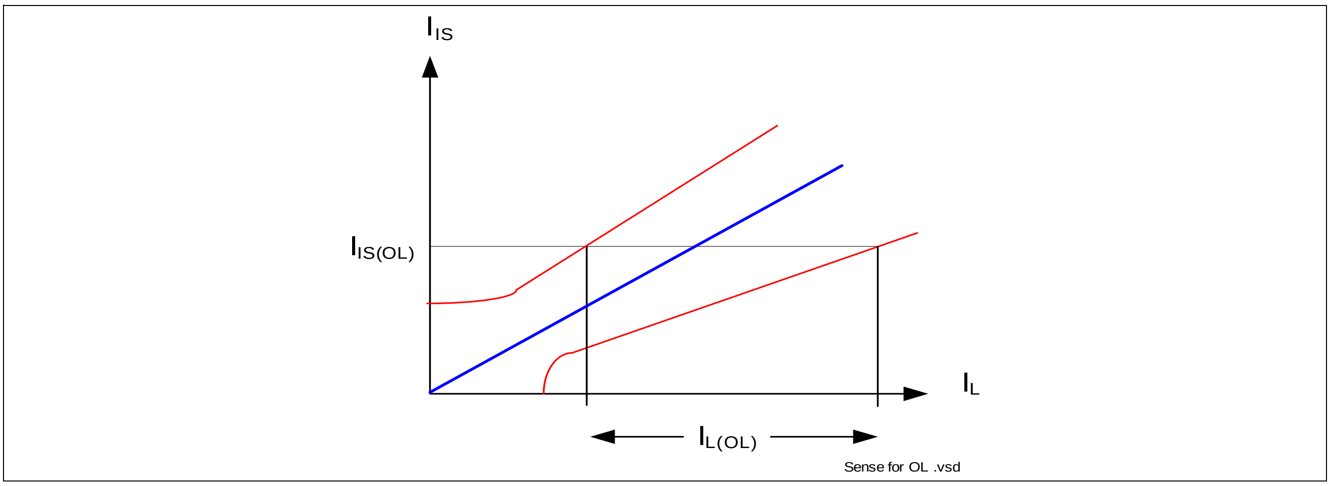


Figure 24 Current Sense Ratio for Low Currents

7.3.3.2 Open Load in OFF Diagnostic

For open load diagnosis in OFF-state, an external output pull-up resistor (R_{OL}) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ have to be taken into account. **Figure 25** gives a sketch of the situation. $I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ (see **Chapter 5.5**) and external leakages, e.g, due to humidity, corrosion, etc.... in the application.

To reduce the stand-by current of the system, an open load resistor switch S_{OL} is recommended. If the channel is OFF, the output is no longer pulled down by the load and V_{OUT} voltage rises to nearly V_S. This is recognized by the device as an open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the SENSE signal is switched to the $I_{IS(FAULT)}$.

An additional R_{PD} resistor can be used to pull V_{OUT} to 0V. Otherwise, the OUT pin is floating. This resistor can be used as well for short circuit to battery detection, see **Chapter 7.3.4**.

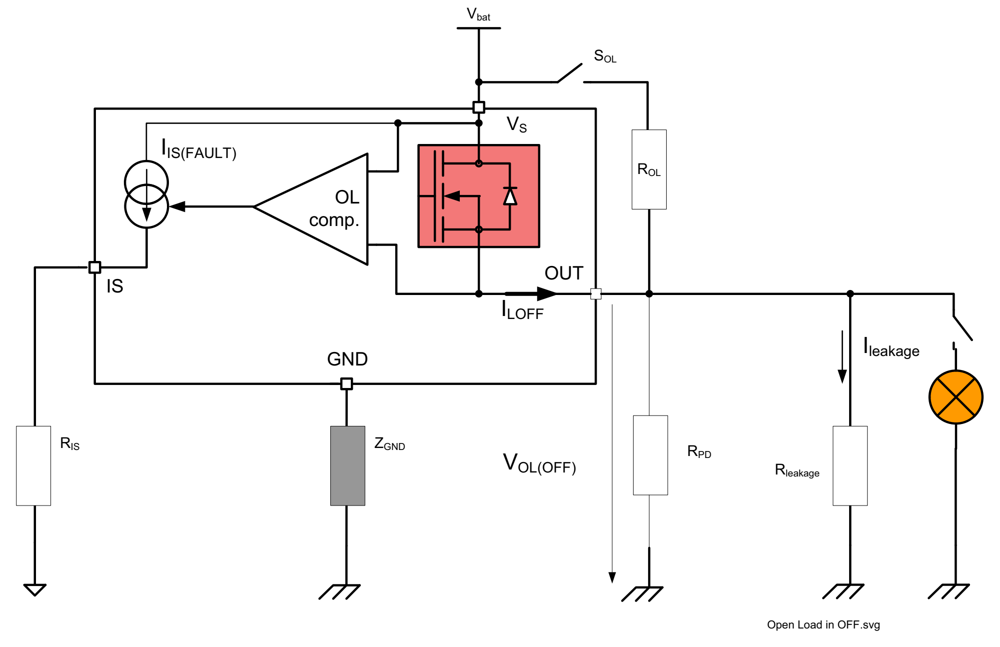


Figure 25 Open Load Detection in OFF Electrical Equivalent Circuit

7.3.3.3 Open Load Diagnostic Timing

Figure 26 shows the timing during either Open load in ON or OFF condition. Please note that a delay $t_{\mathrm{sIS(FAULT\_OL\_OFF)}}$ has to be respected between the falling edge of the input and rising edge of the DEN, when applying an open load in OFF diagnosis request, otherwise the diagnosis can be wrong.

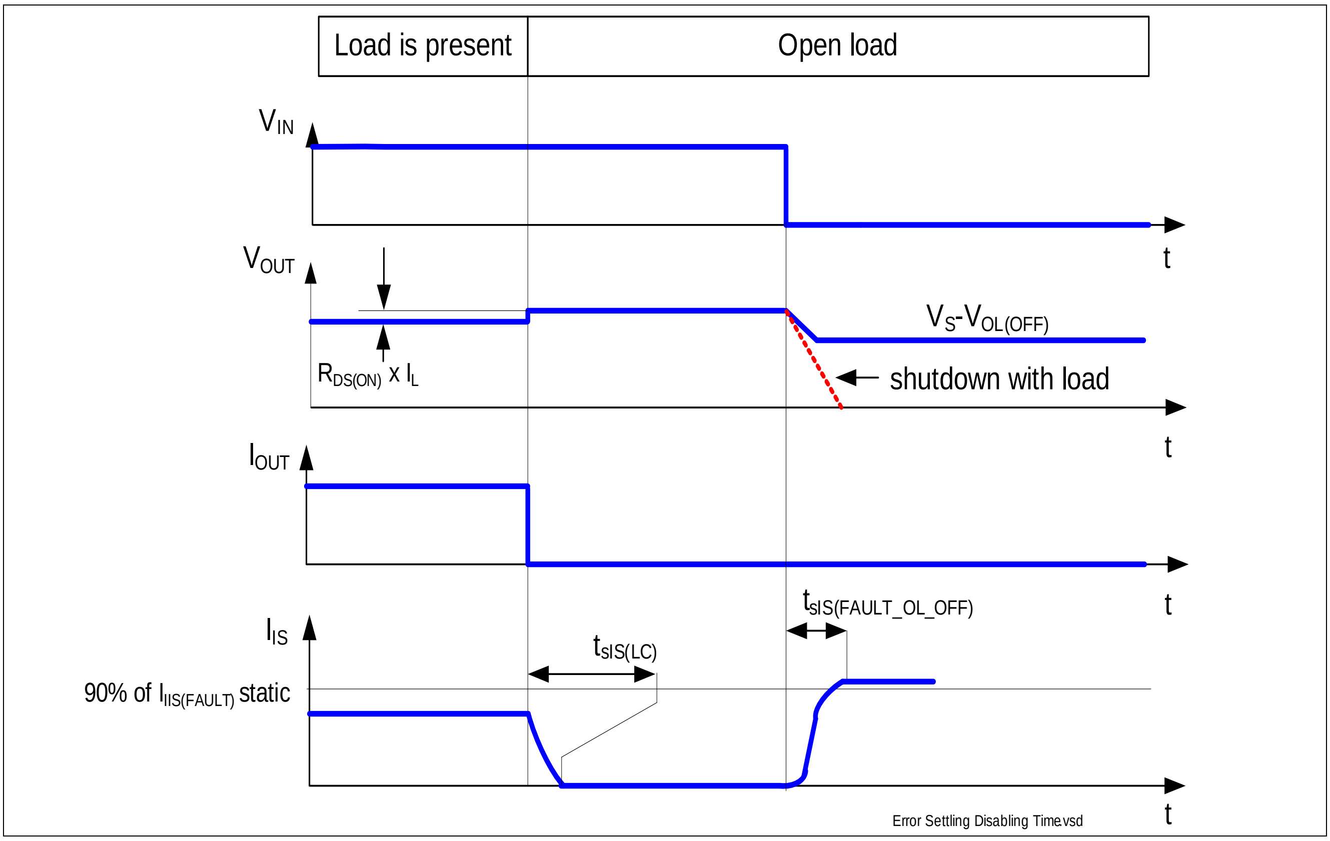


Figure 26 SENSE Signal in Open Load Timing

7.3.4 SENSE Signal with OUT in Short Circuit to V_S

In case of a short circuit between the OUTput-pin and the V_S pin, all or portion (depending on the short circuit impedance) of the load current will flow through the short circuit. As a result, a lower current compared to the normal operation will flow through the DMOS of the BTS5020-1EKA, which can be recognized at the SENSE signal. The open load at OFF detection circuitry can also be used to distinguish a short circuit to V_S. In that case, an external resistor to ground R_{SC_VS} is required. **Figure 27** gives a sketch of the situation.

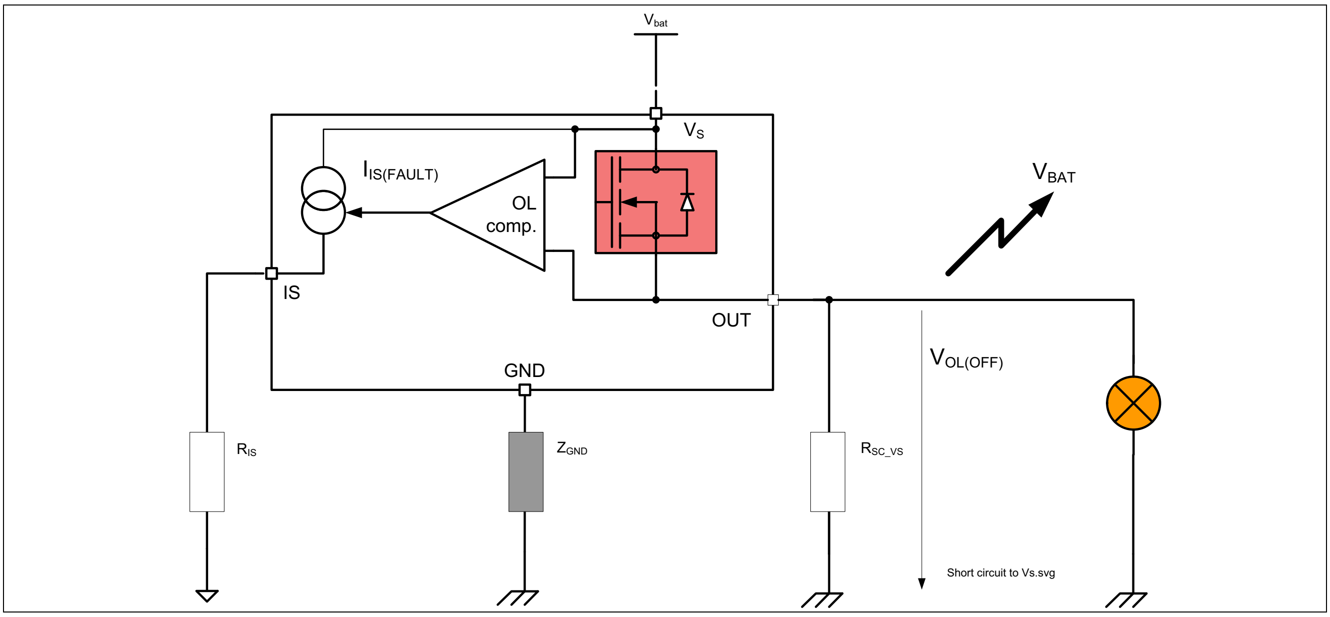


Figure 27 Short Circuit to Battery Detection in OFF Electrical Equivalent Circuit

7.3.5 SENSE Signal in Case of Overload

An overload condition is defined by a current flowing out of the DMOS reaching the current limitation and / or the absolute dynamic temperature swing $T_{J(SW)}$ is reached, and / or the junction temperature reaches the thermal shutdown temperature $T_{J(SC)}$. Please refer to Chapter 6.5 for details.

In that case, the SENSE signal given is by $I_{IS(FAULT)}$ when the diagnostic is selected.

The device has a thermal restart behavior, such that when the overtemperature or the exceed dynamic temperature condition has disappeared, the DMOS is reactivated if the IN is still at logical level one. If the DEN pin is activated, the IS pin is not toggling with the restart mechanism and remains to $I_{IS(FAULT)}$.

7.3.6 SENSE Signal in Case of Inverse Current

In the case of inverse current, the channel will indicate open load in OFF state and indicate open load in ON state.

7.4 Electrical Characteristics Diagnostic Function

Table 8 Electrical Characteristics: Diagnostics

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Load Condition Threshold for Diagnostic							
Open load detection threshold in OFF state	$V_S - V_{OL(OFF)}$	4	–	6	V	$V_{IN} = 0$ V $V_{DEN} = 4.5$ V	P_7.5.1
Open load detection threshold in ON state	$I_{L(OL)}$	5	–	30	mA	$V_{IN} = V_{DEN} = 4.5$ V $I_{IS(OL)} = 4$ µA See **Figure 24** See **Figure 45**	P_7.5.2
Sense Pin							
IS pin leakage current when sense is disabled	$I_{IS\_(DIS)}$	–	–	1	µA	$V_{IN} = 4.5$ V $V_{DEN} = 0$ V $I_L = I_{L4} = 7$ A	P_7.5.4
Sense signal saturation voltage	$V_S - V_{IS}$ (RANGE)	0	–	3	V	1) $V_{IN} = 0$ V $V_{OUT} = V_S > 10$ V $V_{DEN} = 4.5$ V $I_{IS} = 6$ mA See **Figure 46**	P_7.5.6
Sense signal maximum current in fault condition	$I_{IS(FAULT)}$	6	15	35	mA	$V_{IS} = V_{IN} = 0$ V $V_{OUT} = V_S > 10$ V $V_{DEN} = 4.5$ V See **Figure 20** See **Figure 47**	P_7.5.7
Sense pin maximum voltage	$V_{IS(AZ)}$	41	47	53	V	$I_{IS} = 5$ mA See **Figure 20**	P_7.5.3
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition							
Current sense ratio $I_{L0} = 50$ mA	k_{ILIS0}	-50%	3400	+50%		$V_{IN} = 4.5$ V $V_{DEN} = 4.5$ V See **Figure 21** T_J = -40 °C; 150 °C	P_7.5.8
Current sense ratio $I_{L1} = 0.5$ A	k_{ILIS1}	-34%	3030	+34%			P_7.5.9
Current sense ratio $I_{L2} = 2$ A	k_{ILIS2}	-8%	3030	+8%			P_7.5.10
Current sense ratio $I_{L3} = 4$ A	k_{ILIS3}	-7%	3030	+7%			P_7.5.11
Current sense ratio $I_{L4} = 7$ A	k_{ILIS4}	-5.5%	3030	+5.5%			P_7.5.12
k_{ILIS} derating with current and temperature	Δk_{ILIS}	-5	0	+5	%	1) k_{ILIS3} versus k_{ILIS2} See **Figure 22**	P_7.5.17
Diagnostic Timing in Normal Condition							

Table 8 Electrical Characteristics: Diagnostics (cont'd)

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense settling time to k_{ILIS} function stable after positive input slope on both INput and DEN	$t_{\mathrm{sIS(ON)}}$	0	–	250	µs	[1] V_{DEN}=V_{IN}= 0 to 4.5 V V_S = 13.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_L = I_{L3}= 4 A See Figure 23	P_7.5.18
Current sense settling time with load current stable and transition of the DEN	$t_{\mathrm{sIS(ON\_DEN)}}$	0	–	20	µs	V_{IN} = 4.5 V V_{DEN} = 0 to 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_L = I_{L3} = 4 A See Figure 23	P_7.5.19
Current sense settling time to I_{IS} stable after positive input slope on current load	$t_{\mathrm{sIS(LC)}}$	0	–	20	µs	V_{IN} = 4.5 V V_{DEN} = 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_L = 2 A to I_L = 4 A See Figure 23	P_7.5.20
Diagnostic Timing in Open Load Condition							
Current sense settling time to I_{IS} stable for open load detection in OFF state	$t_{\mathrm{sIS(FAULT\_OL\_OFF)}}$	0	–	150	µs	V_{IN} = 0V V_{DEN} = 0 to 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF V_{OUT} = V_S = 13.5 V See Figure 26	P_7.5.22
Diagnostic Timing in Overload Condition							
Current sense settling time to I_{IS} stable for overload detection	$t_{\mathrm{sIS(FAULT)}}$	0	–	250	µs	[2] V_{IN} = V_{DEN} = 0 to 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF V_{DS} = 5 V See Figure 19	P_7.5.24
Current sense over temperature blanking time	$t_{\mathrm{sIS(OT\_blank)}}$	–	350	–	µs	[1] V_{IN} = V_{DEN} = 4.5 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF V_{DS} = 5 V to 0 V See Figure 19	P_7.5.32
Diagnostic disable time DEN transition to I_{IS} < 50% I_L /k_{ILIS}	$t_{\mathrm{sIS(OFF)}}$	0	–	30	µs	V_{IN} = 4.5 V V_{DEN} = 4.5 V to 0 V R_{IS} = 1.2 kΩ C_{SENSE} < 100 pF I_L = I_{L3} = 4 A See Figure 23	P_7.5.25

1) Not subject to production test, specified by design.
2) Test at T_J = -40°C only.

8 Input Pins

8.1 Input Circuitry

The input circuitry is compatible with 3.3 and 5 V microcontrollers. The concept of the input pin is to react to voltage thresholds. An implemented Schmidt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry is compatible with PWM applications. **Figure 28** shows the electrical equivalent input circuitry. In case the pin is not needed, it must be left opened, or must be connected to device ground (and not module ground) via an input resistor.

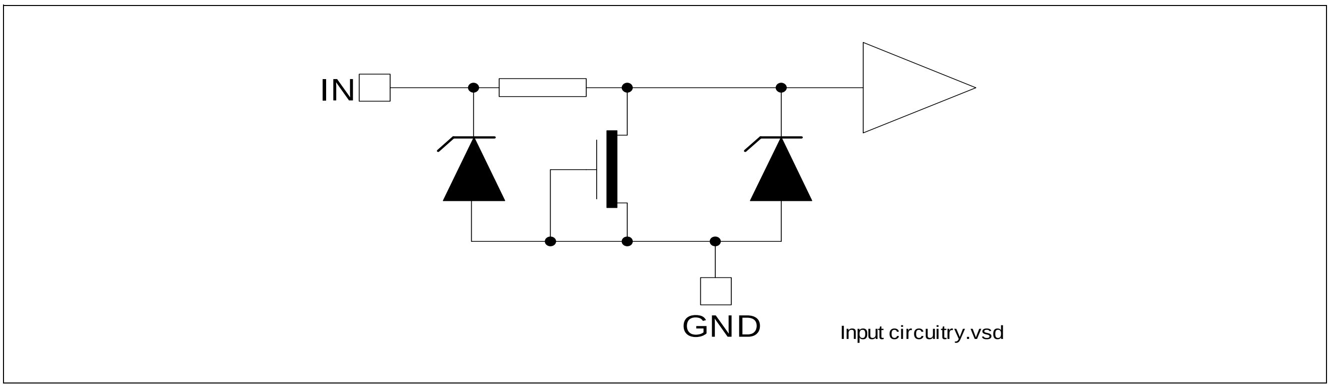


Figure 28 Input Pin Circuitry

8.2 DEN Pin

The DEN pin enable and disable the diagnostic functionality of the device. The pin has the same structure as the INput pin, please refer to **Figure 28**.

8.3 Input Pin Voltage

The IN and DEN use a comparator with hysteresis. The switching ON / OFF takes place in a defined region, set by the thresholds $V_{\mathrm{IN(L)}}$ Max. and $V_{\mathrm{IN(H)}}$ Min. The exact value where the ON and OFF take place are unknown and depends on the process, as well as the temperature. To avoid cross talk and parasitic turn ON and OFF, a hysteresis is implemented. This ensures a certain immunity to noise.

8.4 Electrical Characteristics

Table 9 Electrical Characteristics: Input Pins

V_S = 8 V to 18 V, T_J = -40°C to +150°C (unless otherwise specified).
Typical values are given at V_S = 13.5 V, T_J = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
INput Pins Characteristics							
Low level input voltage range	$V_{IN(L)}$	-0.3	–	0.8	V	See **Figure 48**	P_8.4.1
High level input voltage range	$V_{IN(H)}$	2	–	6	V	See **Figure 49**	P_8.4.2
Input voltage hysteresis	$V_{IN(HYS)}$	–	250	–	mV	[1] See **Figure 50**	P_8.4.3
Low level input current	$I_{IN(L)}$	1	10	25	µA	V_{IN} = 0.8 V	P_8.4.4
High level input current	$I_{IN(H)}$	2	10	25	µA	V_{IN} = 5.5 V See **Figure 51**	P_8.4.5
DEN Pin							
Low level input voltage range	$V_{DEN(L)}$	-0.3	–	0.8	V	–	P_8.4.6
High level input voltage range	$V_{DEN(H)}$	2	–	6	V	–	P_8.4.7
Input voltage hysteresis	$V_{DEN(HYS)}$	–	250	–	mV	[1]	P_8.4.8
Low level input current	$I_{DEN(L)}$	1	10	25	µA	V_{DEN} = 0.8 V	P_8.4.9
High level input current	$I_{DEN(H)}$	2	10	25	µA	V_{DEN} = 5.5 V	P_8.4.10

1) Not subject to production test, specified by design

9 Characterization Results

The characterization have been performed on 3 lots, with 3 devices each. Characterization have been performed at 8 V, 13.5 V and 18 V over temperature range. When no dependency to voltage is seen, only one curve (13,5V) is sketched.

9.1 General Product Characteristics

9.1.1 Minimum Functional Supply Voltage

P_4.2.3

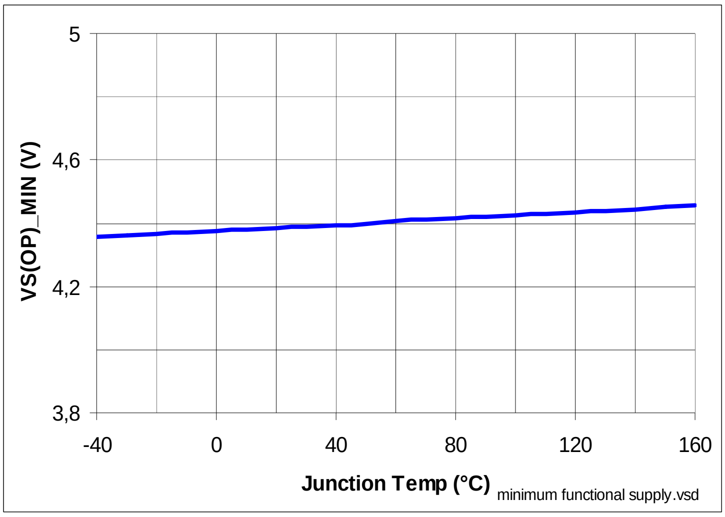


Figure 29 Minimum Functional Supply Voltage $V_{\mathrm{S(OP)\_MIN}} = f(T_{\mathrm{J}})$

9.1.2 Undervoltage Shutdown

P_4.2.4

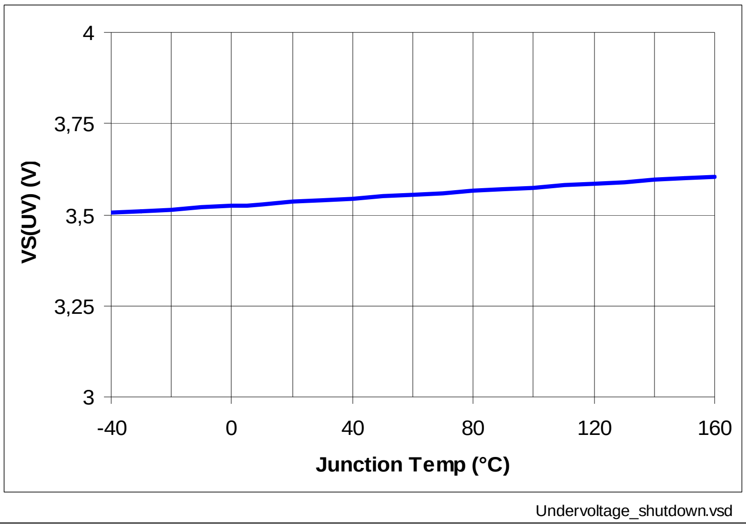
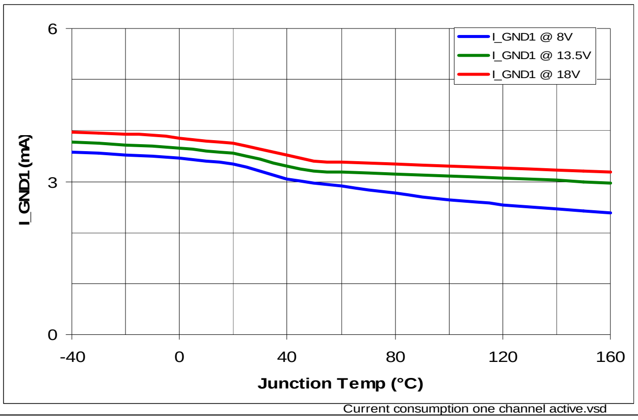


Figure 30 Undervoltage Threshold $V_{\mathrm{S(UV)}} = f(T_{\mathrm{J}})$

9.1.3 Current Consumption Channel active

P_4.2.5



Current consumption one channel active.vsd

Figure 31 Current Consumption for Whole Device with Load, Channel Active $I_{GND\_1} = f(T_J;V_S)$

9.1.4 Standby Current for Whole Device with Load

P_4.2.7, P_4.2.10

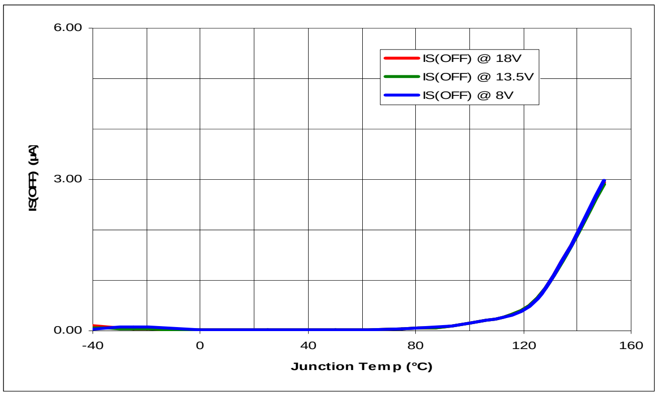


Figure 32 Standby Current for Whole Device with Load. $I_{S(OFF)} = f(T_J;V_S)$

9.2 Power Stage

9.2.1 Output Voltage Drop Limitation at Low Load Current

P_5.5.4

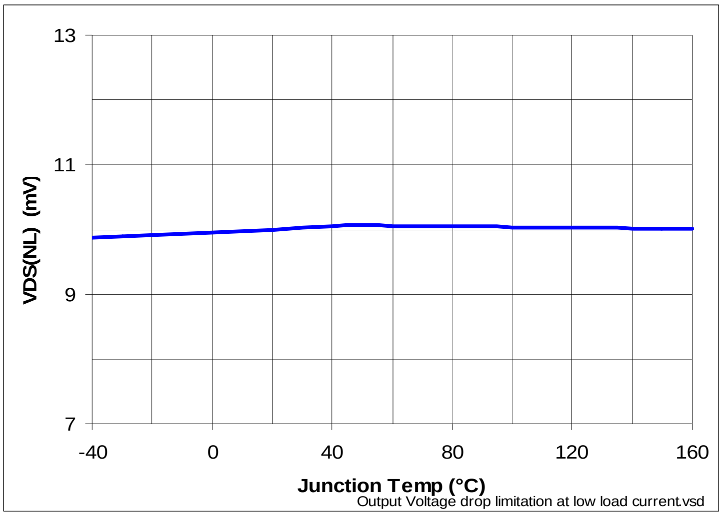


Figure 33 Output Voltage Drop Limitation at Low Load Current $V_{DS(NL)} = f(T_J;V_S)$

9.2.2 Drain to Source Clamp Voltage

P_5.5.5

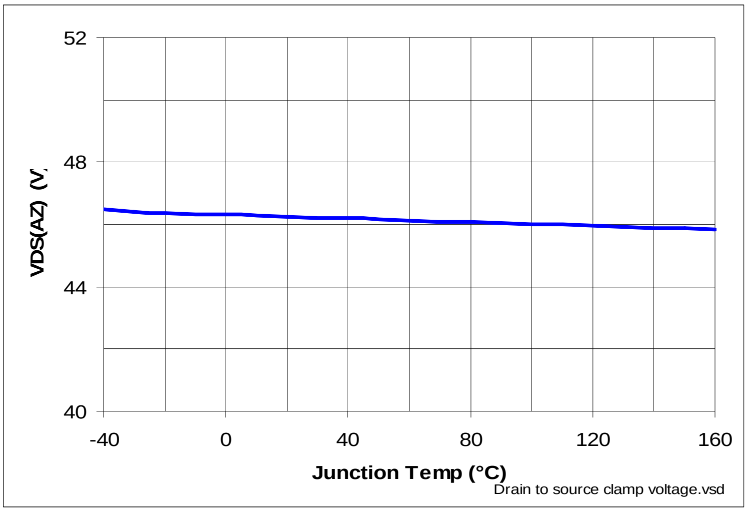


Figure 34 Drain to Source Clamp Voltage $V_{DS(AZ)} = f(T_J)$

9.2.3 Slew Rate at Turn ON

P_5.5.11

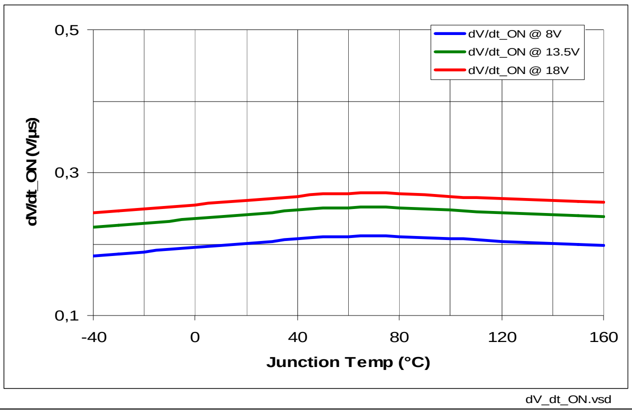


Figure 35 Slew Rate at Turn ON $dV/dt_{ON} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.2.4 Slew Rate at Turn OFF

P_5.5.12

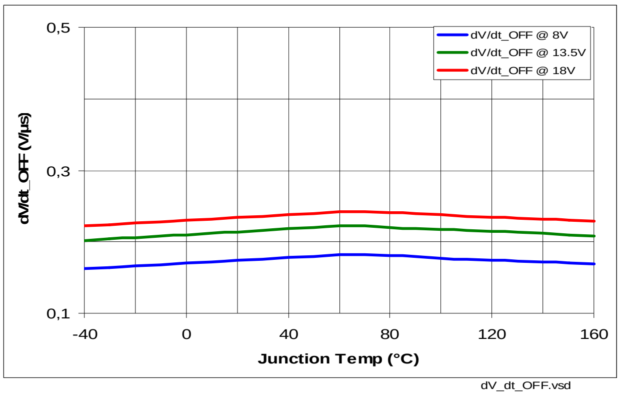


Figure 36 Slew Rate at Turn OFF - $dV/dt_{OFF} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.2.5 Turn ON

P_5.5.14

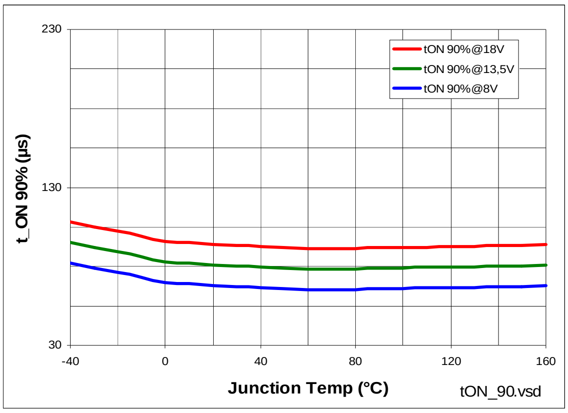


Figure 37 Turn ON $t_{ON} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.2.6 Turn OFF

P_5.5.11

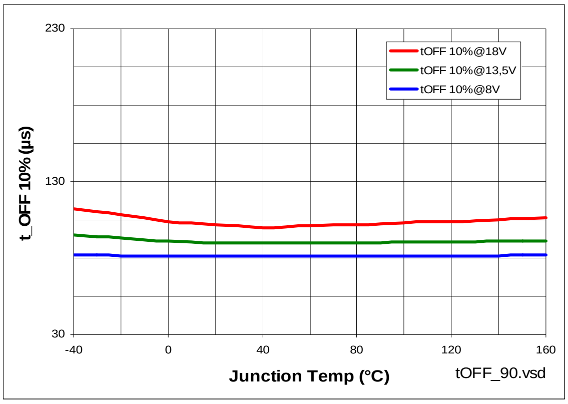


Figure 38 Turn OFF $t_{OFF} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.2.7 Turn ON / OFF matching

P_5.5.16

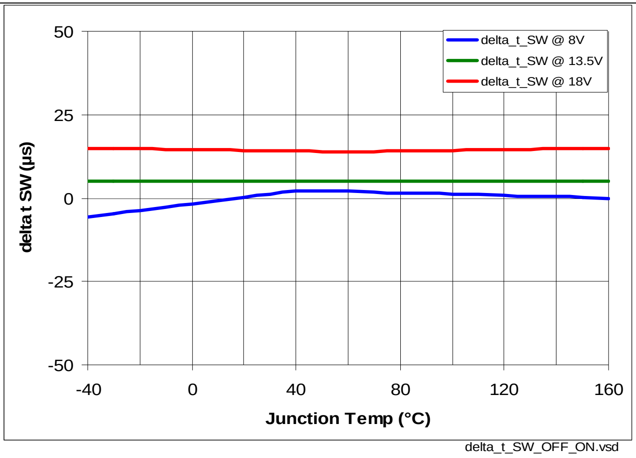


Figure 39 Turn ON / OFF matching $\Delta t_{SW} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.2.8 Switch ON Energy

P_5.5.19

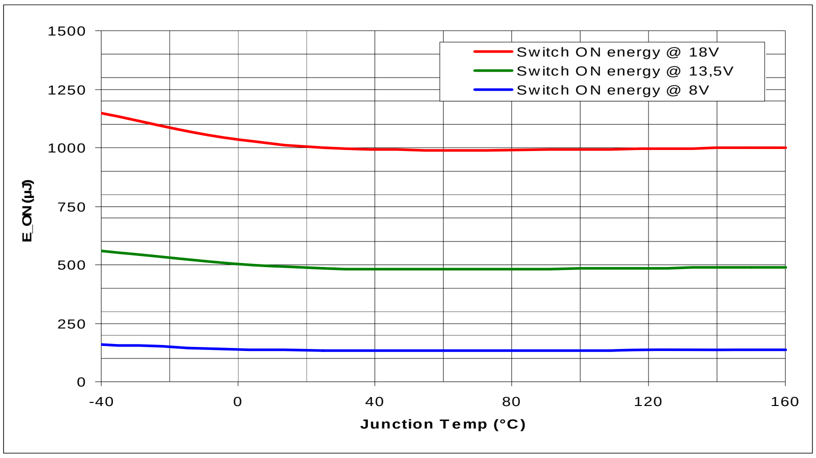


Figure 40 Switch ON Energy $E_{ON} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.2.9 Switch OFF Energy

P_5.5.20

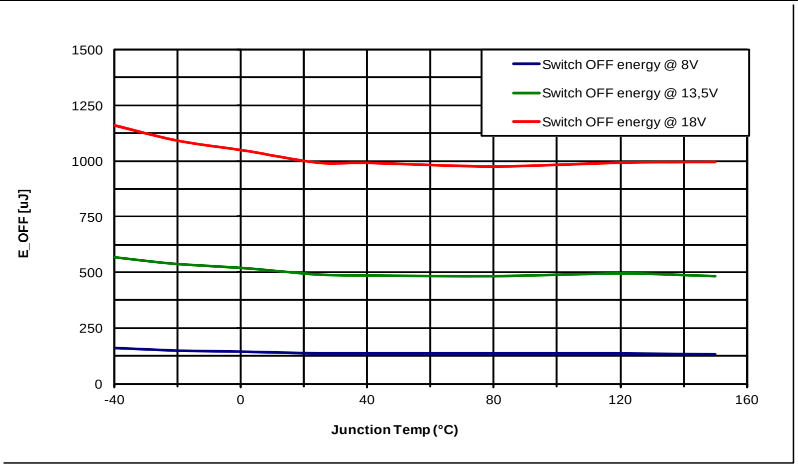


Figure 41 Switch OFF Energy $E_{OFF} = f(T_J;V_S)$, $R_L = 4\ \Omega$

9.3 Protection Functions

9.3.1 Overload Condition in the Low Voltage Area

P_6.6.4

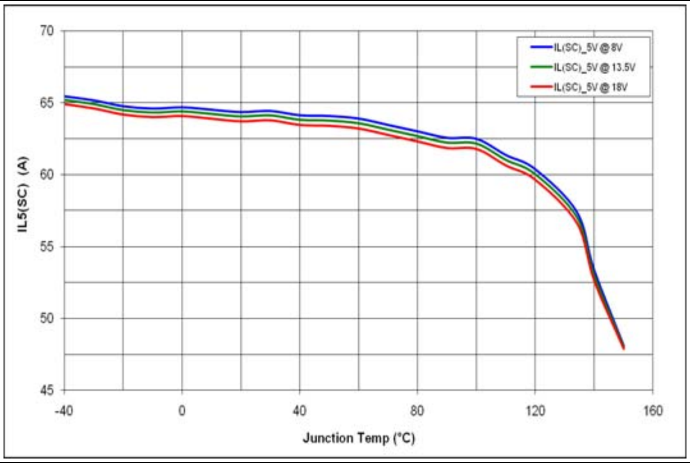


Figure 42 Overload Condition in the Low Voltage Area $I_{L5(SC)} = f(T_J;V_S)$

9.3.2 Overload Condition in the High Voltage Area

P_6.6.7

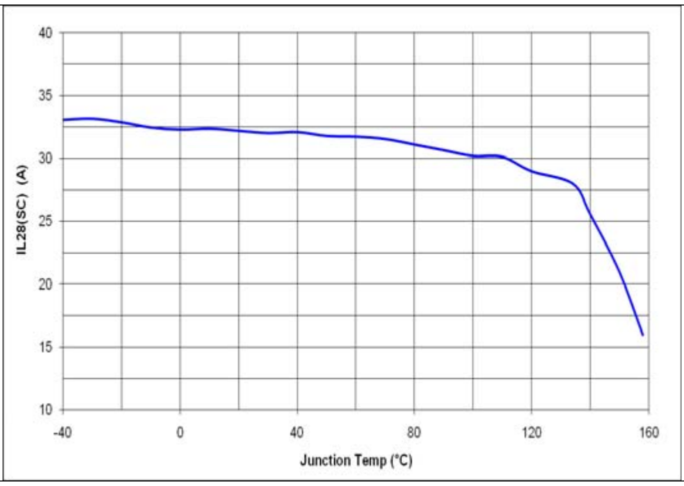


Figure 43 Overload Condition in the High Voltage Area $I_{L28(SC)} = f(T_J;V_S)$

9.4 Diagnostic Mechanism

9.4.1 Current Sense at no Load

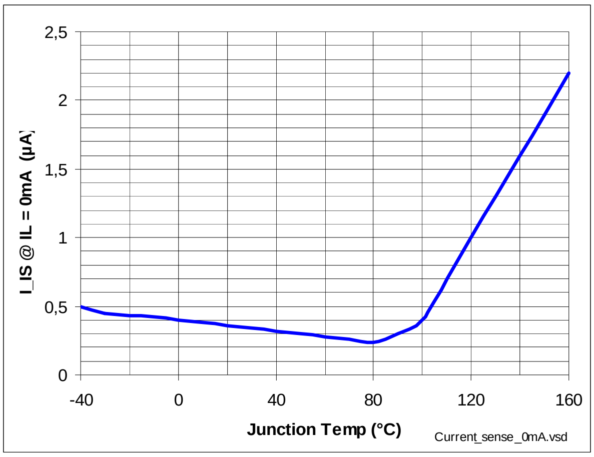


Figure 44 Current Sense at no Load $I_{L(OL)} = f(T_J;V_S)$; I_L = 0A

9.4.2 Open Load Detection Threshold in ON State

P_7.5.2

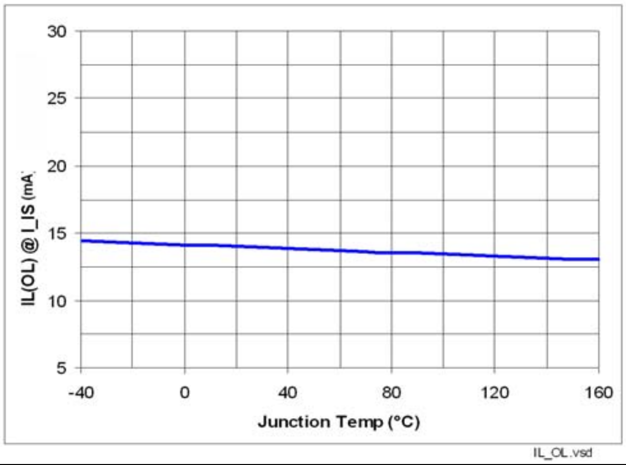


Figure 45 Open Load Detection ON State Threshold $I_{L(OL)} = f(T_J;V_S)$

9.4.3 Sense Signal Maximum Voltage

P_7.5.3

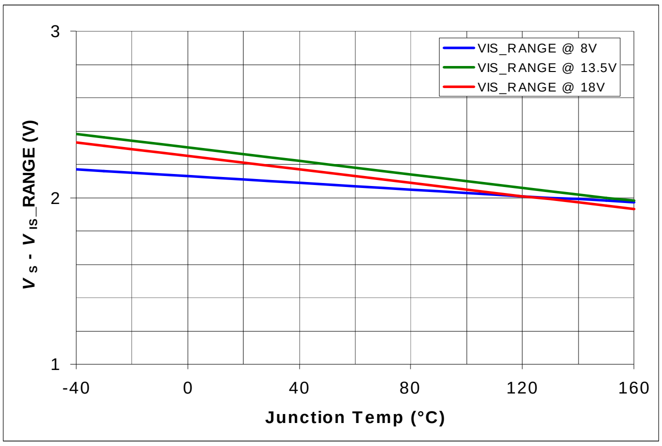


Figure 46 Sense Signal Maximum Voltage V_S - $V_{IS(RANGE)}$ = $f(T_J;V_S)$

9.4.4 Sense Signal maximum Current

P_7.5.7

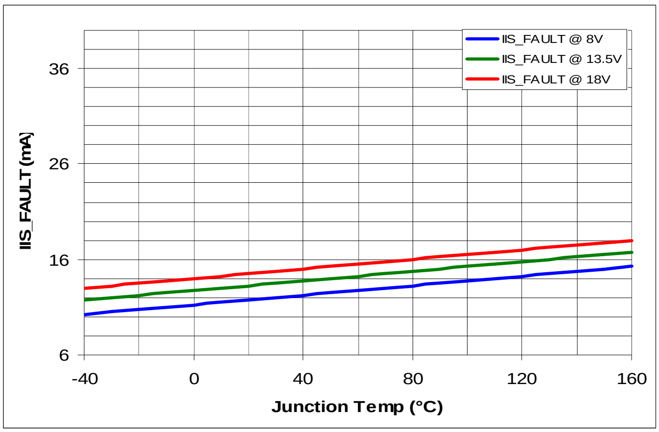
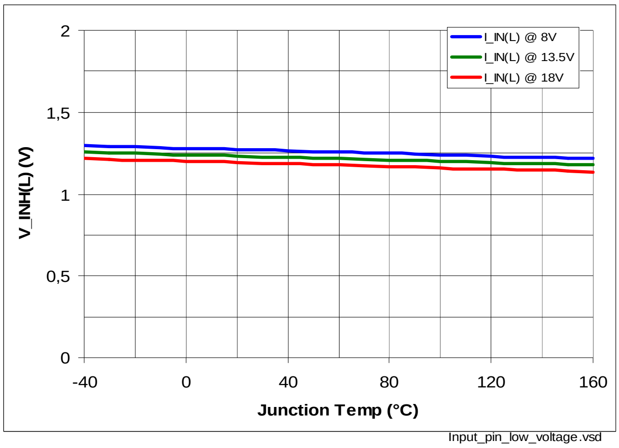


Figure 47 Sense Signal Maximum Current in Fault Condition $I_{IS(FAULT)}$ = $f(T_J;V_S)$

9.5 Input Pins

9.5.1 Input Voltage Threshold ON to OFF

P_8.4.1

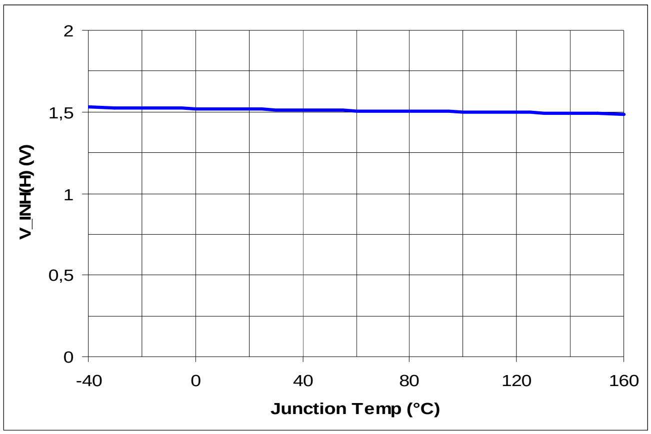


Input_pin_low_voltage.vsd

Figure 48 Input Voltage Threshold $V_{\mathrm{IN(L)}} = f(T_J;V_S)$

9.5.2 Input Voltage Threshold OFF to ON

P_8.4.2

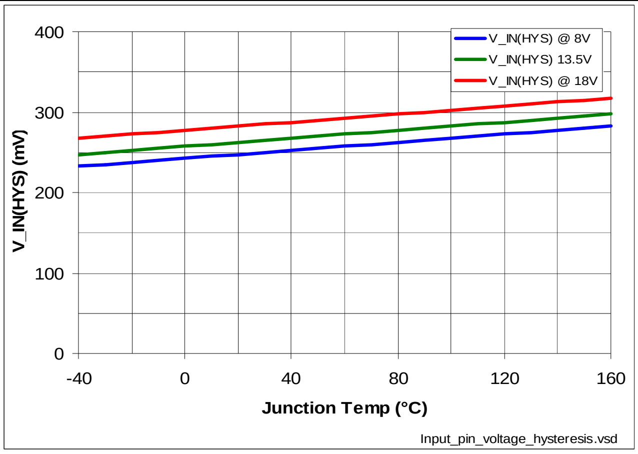


Input_pin_high_voltage.vsd

Figure 49 Input Voltage Threshold $V_{\mathrm{IN(H)}} = f(T_J;V_S)$

9.5.3 Input Voltage Hysteresis

P_8.4.3

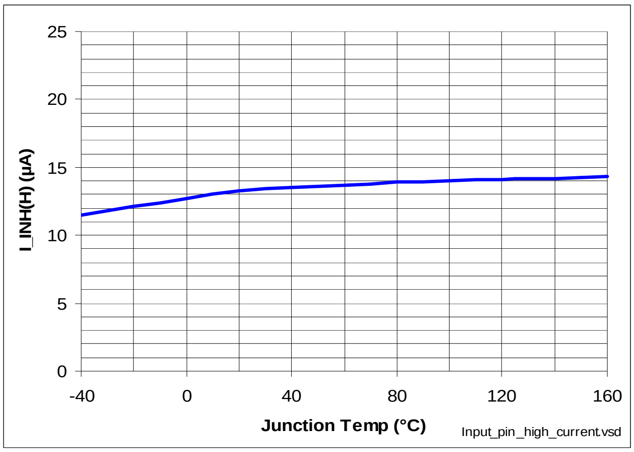


Input_pin_voltage_hysteresis.vsd

Figure 50 Input Voltage Hysteresis $V_{IN(HYS)} = f(T_J;V_S)$

9.5.4 Input Current High Level

P_8.4.5



Input_pin_high_current.vsd

Figure 51 Input Current High Level $I_{IN(H)} = f(T_J;V_S)$

10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

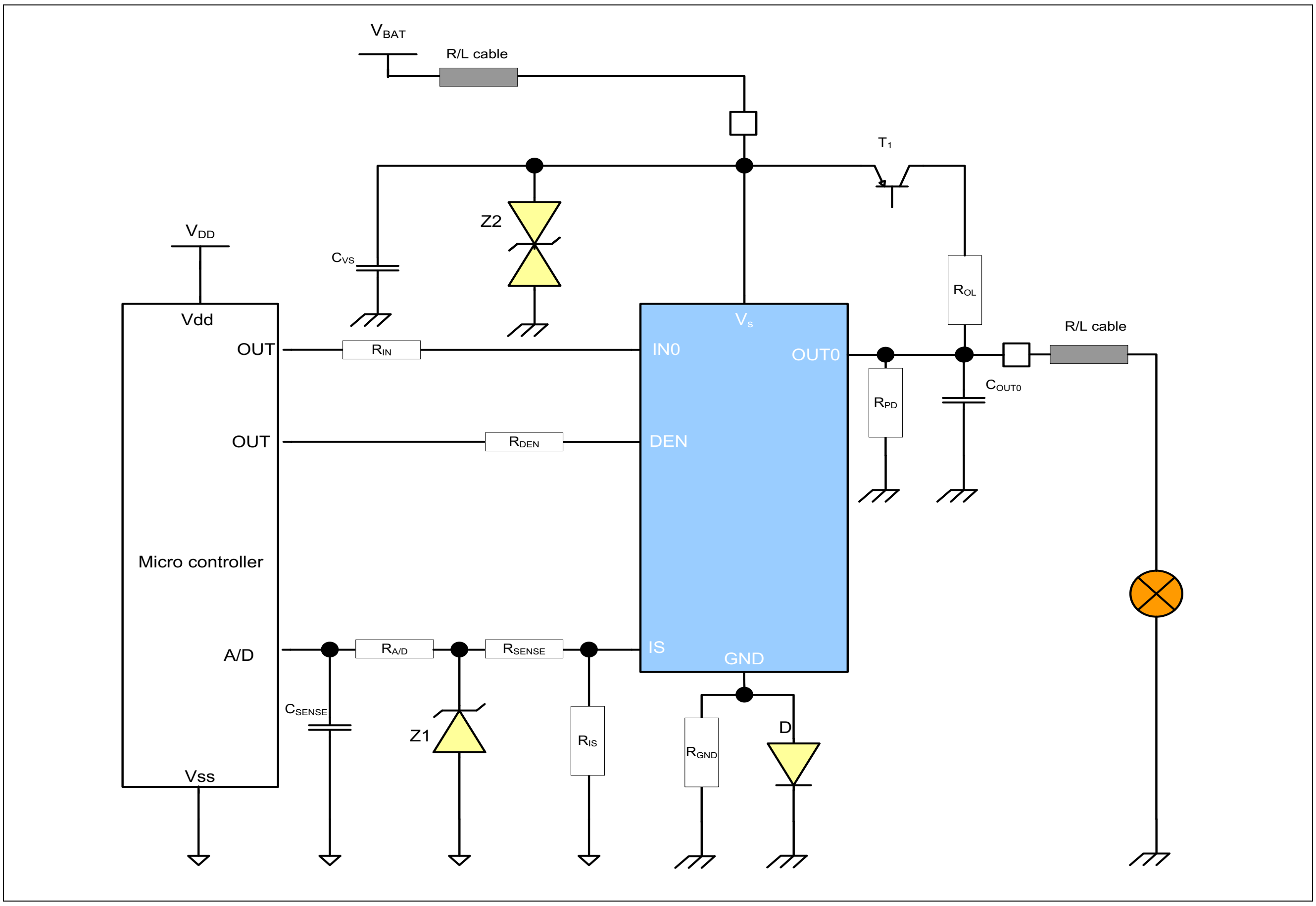


Figure 52 Application Diagram with BTS5020-1EKA

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 10 Bill of Material

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the micro controller during overvoltage, reverse polarity Guarantee BTS5020-1EKA channel OFF during loss of ground
R_{DEN}	4.7 kΩ	Protection of the micro controller during overvoltage, reverse polarity Guarantee BTS5020-1EKA channel OFF during loss of ground
R_{PD}	47 kΩ	Polarization of the output Improve BTS5020-1EKA immunity to electromagnetic noise
R_{IS}	1.2 kΩ	Sense resistor
R_{SENSE}	4.7 kΩ	Overvoltage, reverse polarity, loss of ground. Value to be tuned with micro controller specification.
R_{OL}	1.5 kΩ	Ensure polarization of the BTS5020-1EKA output during open load in OFF diagnostic
$R_{A/D}$	4.7 kΩ	Protection of the micro controller during overvoltage, reverse polarity

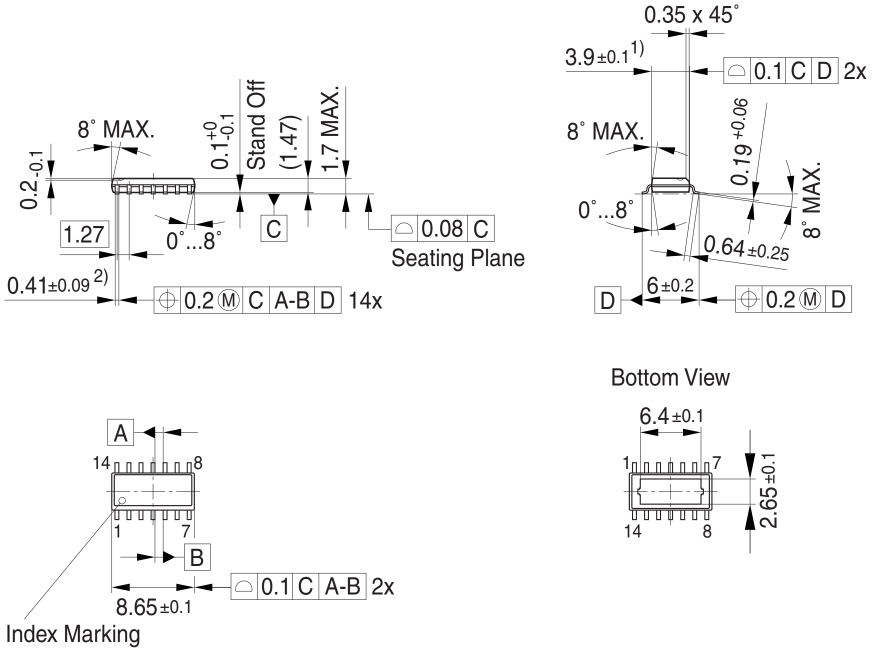
Table 10 Bill of Material (cont'd)

Reference	Value	Purpose
D	BAS21	Protection of the BTS5020-1EKA during reverse polarity
R_{GND}	1 kΩ	To keep the device GND at a stable potential during clamping
$Z1$	7 V Zener diode	Protection of the micro controller during overvoltage
$Z2$	36 V Zener diode	Protection of the device during overvoltage
$T1$	BC 807	Switch the battery voltage for open load in OFF diagnostic
C_{SENSE}	100 pF	Sense signal filtering
C_{VS}	100 nF	Filtering of the voltage spikes on the battery line
C_{OUT0}	4.7 nF	Protection of the BTS5020-1EKA during ESD and BCI

10.1 Further Application Information

- Please contact us to get the pin FMEA
- Existing App. Notes
- For further information you may visit **http://www.infineon.com/profet**

11 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.13 max.
3) JEDEC reference MS-012 variation BB

Figure 53 PG-DSO-14-47-EP (Plastic Dual Small Outline Package) (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

12 Revision History

Version	Date	Parameter	Changes
2.0	2011-12-09		Creation of the Data Sheet
2.1	2013-09-06		changed kilis specification parameters and figures 21/22 accordingly
		P_7.5.8	typical value changed from 3600 to 3400
		P_7.5.9	typical value changed from 3000 to 3030
		P_7.5.10	changed from 13% to 8%, typical value changed from 3000 to 3030
		P_7.5.11	changed from 9% to 6.5%, typical value changed from 3000 to 3030
		P_7.5.12	changed from 8% to 5.5%, typical value changed from 3000 to 3030
		P_7.5.17	changed from 8% to 5%
			Updated Fig 4) PCB 2s2p Cross Section
2.2	2013-11-12	P_4.3.2	Changed typical value to 30K/W Updated Figure 6 and Figure 7

Edition 2013-11-12

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