SPOC - BTS5566G

SPI Power Controller

Automotive Power

Never stop thinking

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SPI Power Controller **SPOC - BTS5566G**

for Advanced Light Control

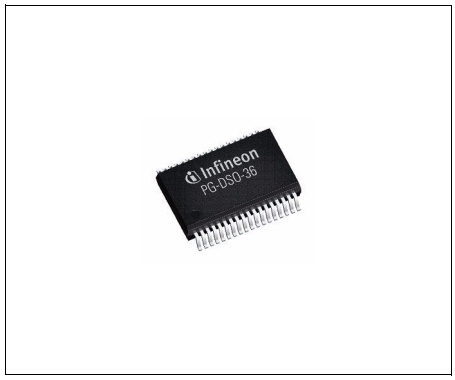
AEC Qualified RoHS

1 Overview

The SPOC - BTS5566G is a five channel high-side smart power switch in PG-DSO-36-34 package providing embedded protective functions. It is especially designed to control standard exterior lighting in automotive applications. It is designed to drive lamps up to 3*27W + 2*10W.

Configuration and status diagnosis is done via SPI. Additionally, there is a current sense signal available for each channel that is routed via a multiplexer to a single diagnosis pin.

The SPOC - BTS5566G provides a fail-safe function via limp home input pin.



PG-DSO-36-34

Product Summary

Operating Voltage Power Switch	V_{BB}	4.5 … 28 V
Logic Supply Voltage	V_{DD}	3.8 … 5.5 V
Over Voltage Protection	$V_{BB(AZ,min)}$	40 V
Maximum Stand-By Current at 25 °C	$I_{BB(OFF)}$	3 µA
On-State Resistance at T_j = 150 ° channel 0, 1 channel 2 channel 3,4	$R_{DS(ON)\ max}$	 49 mΩ 64 mΩ 180 mΩ
SPI Access Frequency	$f_{SCLK(max)}$	2 MHz

Type	Package	Marking
SPOC - BTS5566G	PG-DSO-36-34	BTS5566G

Basic Features

- 8 bit serial peripheral interface (daisy chain capable SPI) for control and diagnostics
- CMOS compatible parallel input pins for each channel provide straightforward PWM operation
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Very low stand-by current
- Optimized electromagnetic compatibility (EMC) for bulbs
- Stable behavior at under voltage
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

Protective Functions

- Reverse battery protection with external components
- Short circuit protection
- Over load protection
- Multi step current limitation
- Thermal shutdown with latch
- Over voltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signals (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Feedback on over temperature and over load via SPI
- Multiplexed switch bypass monitor provides short circuit to V_{bb} detection

Application Specific Functions

- Fail-safe activation via LHI pin and configuration via input pins

Applications

- High-side power switch for 12 V grounded loads in automotive application
- Especially designed for standard exterior lighting like tail light, brake light, reverse light, parking light, license plate lighting and turn signal indicators
- Replaces electromechanical relays, fuses and discrete circuits

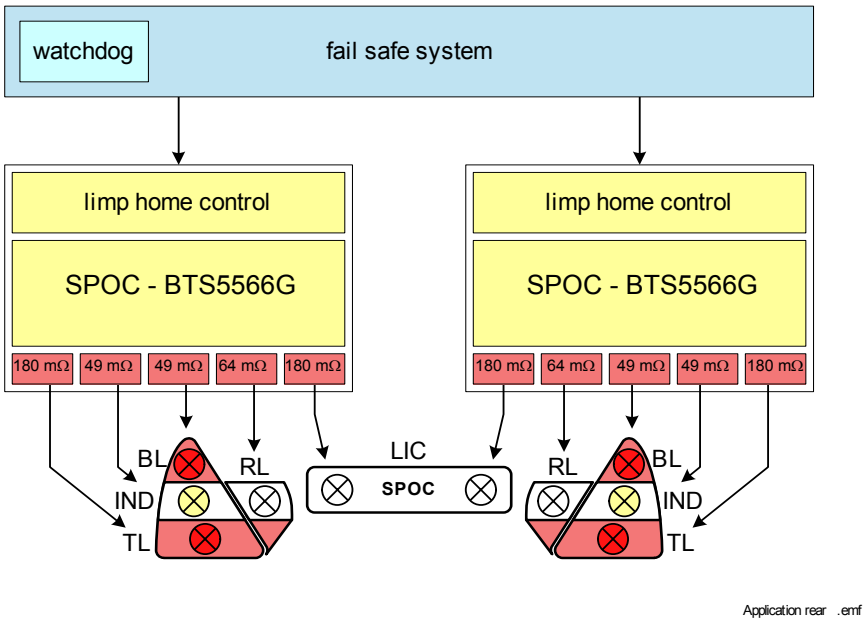


Figure 1 Application Example

Abbreviations:

BL	Brake Light (21 W, 27 W)
RL	Reverse Light (21 W, 27 W)
TL	Tail Light (5 W, 7 W, 10 W)
LIC	License plate lighting (5 W, 10 W)
IND	Indicator / Flasher (21 W, 27 W)

2 Block Diagram

The SPOC - BTS5566G is a five channel high-side power switch in PG-DSO-36-34 package providing embedded protective functions. An 8 bit serial peripheral interface (SPI) is used for configuration and diagnosis. The SPI can be used in daisy chain configuration.

The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over load and over temperature flag is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides diagnosis at short-circuit to V_{BB}.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART SIPMOS technology.

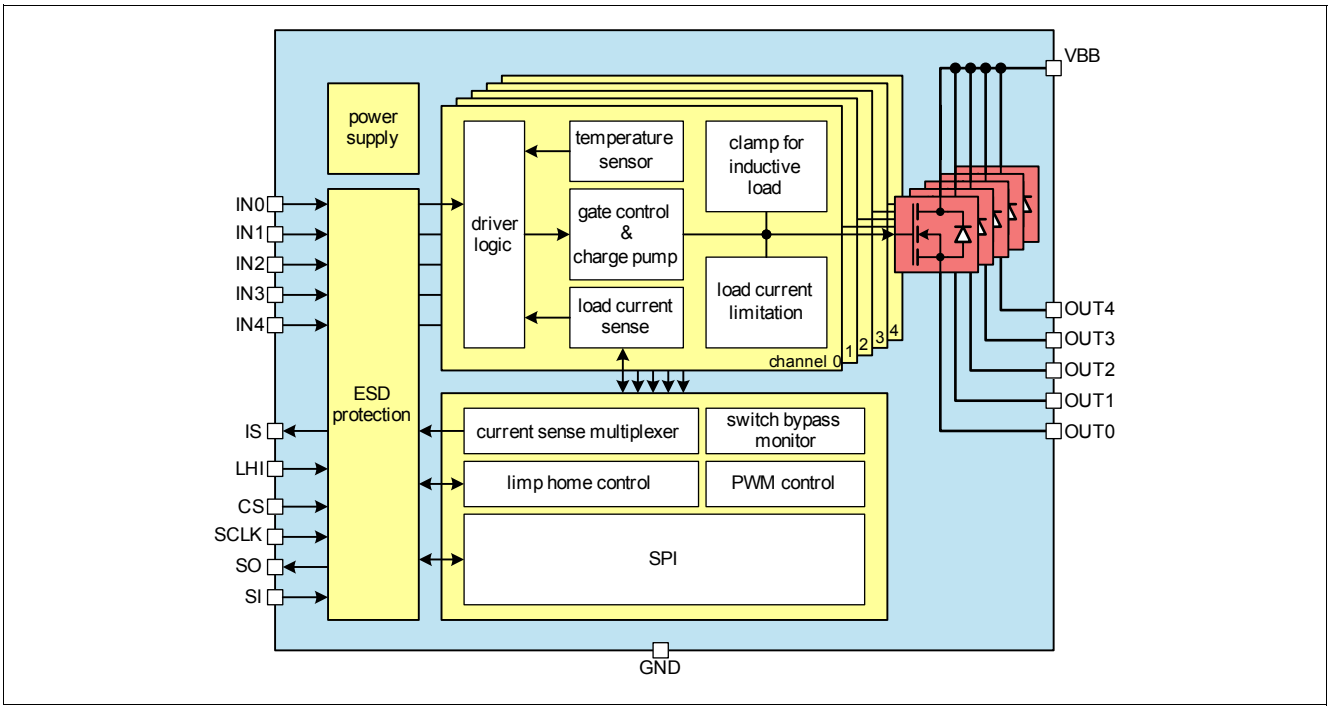


Figure 2 Block Diagram SPOC - BTS5566G

2.1 Terms

The following figure shows all terms used in this data sheet.

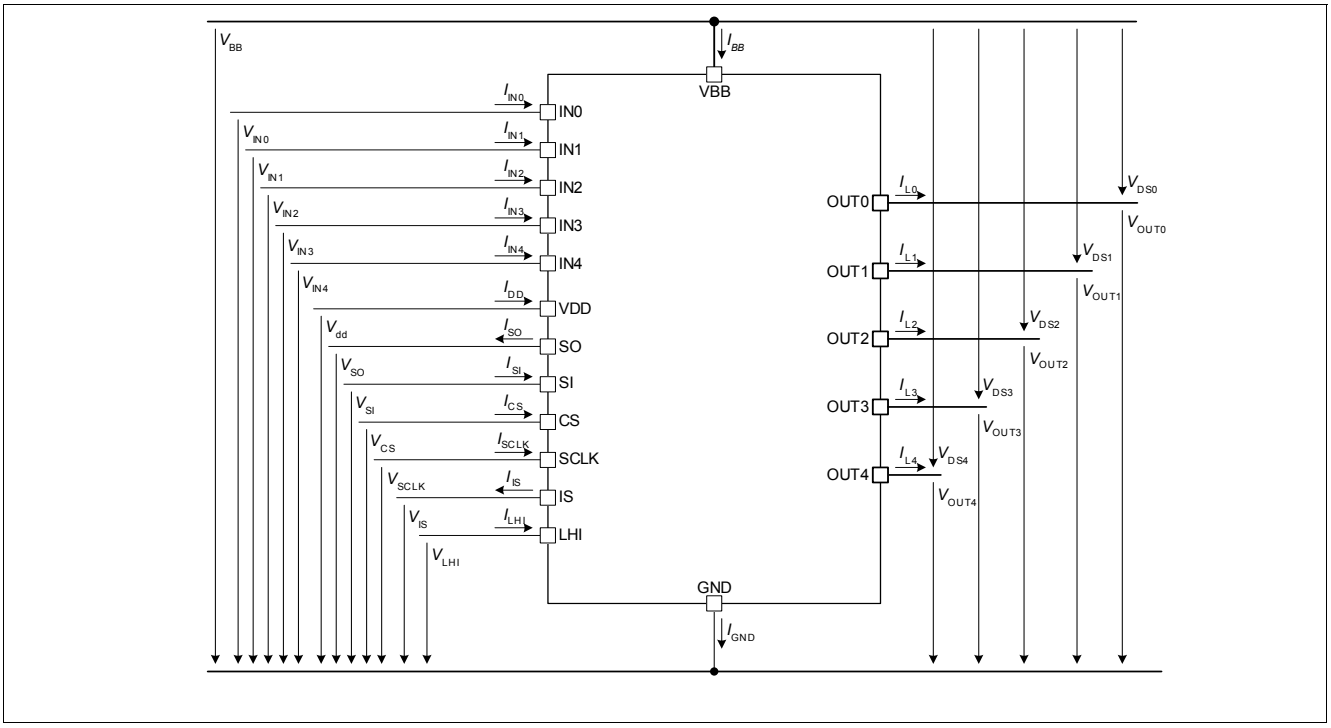


Figure 3 Terms

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} ... V_{DS4}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.CTL`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment SPOC - BTS5566G

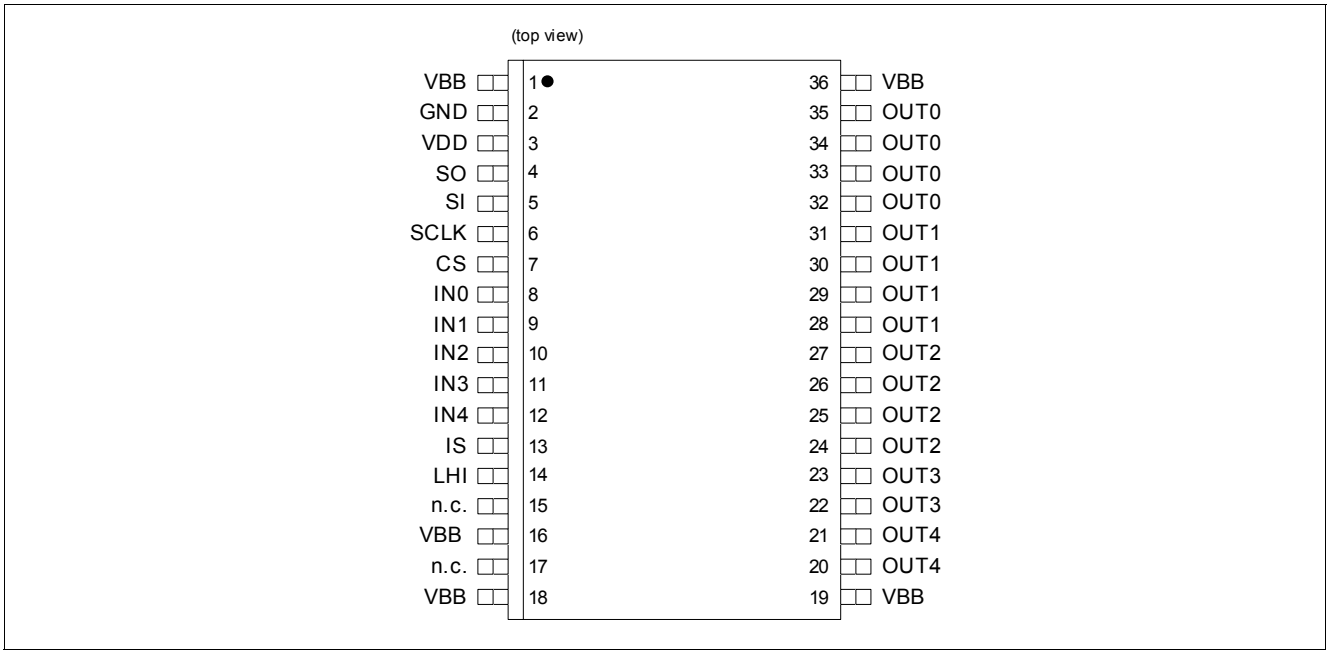


Figure 4 Pin Configuration PG-DSO-36-34

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
1, 16, 18, 19, 36 [1]	VBB	–	Positive power supply for high-side power switch and limp home block
3	VDD	–	Logic supply (5 V)
2	GND	–	Ground connection
Parallel Input Pins			
8	IN0	I	Input signal of channel 0
9	IN1	I	Input signal of channel 1
10	IN2	I	Input signal of channel 2
11	IN3	I	Input signal of channel 3
12	IN4	I	Input signal of channel 4
Power Output Pins			
32, 33, 34, 35 [2]	OUT0	O	Protected high-side power output of channel 0
28, 29,30, 31 [2]	OUT1	O	Protected high-side power output of channel 1
24, 25,26, 27 [2]	OUT2	O	Protected high-side power output of channel 2
22, 23 [2]	OUT3	O	Protected high-side power output of channel 3
20, 21 [2]	OUT4	O	Protected high-side power output of channel 4
SPI & Diagnosis Pins			
7	CS	I	Chip select of SPI interface (low active)
6	SCLK	I	Serial clock of SPI interface
5	SI	I	Serial input of SPI interface
4	SO	O	Serial output of SPI interface
13	IS	O	Diagnosis output signal
Limp Home Pins			
14	LHI	I	Limp home mode activation
Other Pins			
15, 17	n.c.	–	not connected, floating

1) All VBB pins have to be connected.

2) All output pins of each channel have to be connected.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]
T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin.
(unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
Supply Voltage						
4.1.1	Power supply voltage	V_{BB}	-0.3	28	V	–
4.1.2	Logic supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Reverse polarity voltage according **Figure 23**	$-V_{BAT(rev)}$	–	16	V	T_{jStart} = 25 °C $t \leq$ 2 min [2)]
4.1.4	Supply voltage for full short circuit protection (single pulse) ($T_{j(0)}$ = -40 °C … 150 °C)	$V_{BB(SC)}$	0	20	V	R_{ECU} = 20mΩ R_{Cable}= 16mΩ/m L_{Cable}= 1µH/m l = 0 or 5m [3)]
4.1.5	Voltage at power transistor	V_{DS}	–	54	V	–
4.1.6	Supply Voltage for Load Dump protection	$V_{BB(LD)}$	–	41	V	R_I = 2 Ω [4)] t = 400ms
4.1.7	Current through ground pin	I_{GND}	-100	25	mA	$t \leq$ 2 min
4.1.8	Current through VDD pin	I_{DD}	-25	12	mA	$t \leq$ 2 min
Power Stages						
4.1.9	Load current	I_L	$-I_{L(LIM)}$	$I_{L(LIM)}$	A	[5)]
Diagnosis Pin						
4.1.10	Current through sense pin IS	I_{IS}	-10	10	mA	$t \leq$ 2 min
Input Pins						
4.1.11	Voltage at input pins	V_{IN}	-0.3	8.0	V	–
4.1.12	Current through input pins	I_{IN}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min
SPI Pins						
4.1.13	Voltage at chip select pin	V_{CS}	-0.3	5.7	V	–
4.1.14	Current through chip select pin	I_{CS}	-2.0	2.0	mA	$t \leq$ 2 min
4.1.15	Voltage at serial input pin	V_{SI}	-0.3	5.7	V	–
4.1.16	Current through serial input pin	I_{SI}	-2.0	2.0	mA	$t \leq$ 2 min
4.1.17	Voltage at serial clock pin	V_{SCLK}	-0.3	5.7	V	–
4.1.18	Current through serial clock pin	I_{SCLK}	-2.0	2.0	mA	$t \leq$ 2 min
4.1.19	Current through serial output pin SO	I_{SO}	-2.0	2.0	mA	$t \leq$ 2 min
Limp Home Pins						
4.1.20	Voltage at limp home input pin	V_{LHI}	-0.3	8.0	V	–
4.1.21	Current through limp home input pin	I_{LHI}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min

Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin.
(unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
Temperatures						
4.1.22	Junction temperature	T_j	-40	150	°C	–
4.1.23	Dynamic temperature increase while switching	ΔT_j	–	60	K	–
4.1.24	Storage temperature	T_{STG}	-55	150	°C	–
ESD Susceptibility						
4.1.25	ESD resistivity HBM	V_{ESD}			kV	HBM[6)]
	OUT pins		-4	4		–
	other pins		-2	2		–

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).
3) In accordance to AEC Q100-012 and AEC Q101-006.
4) R_I is the internal resistance of the load dump pulse generator.
5) Current limitation is a protection feature. Operation in current limitation is considered as “outside” normal operating range. Protection features are not designed for continuous repetitive operation.
6) ESD resistivity, HBM according to EIA/JESD 22-A 114B (1.5kΩ, 100pF).

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

5 Power Supply

The SPOC - BTS5566G is supplied by two supply voltages V_{BB} and V_{DD}. The V_{BB} supply line is used by the power switches. The V_{DD} supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins VDD and GND is recommended.

There is a power-on reset function implemented for the V_{DD} logic supply voltage. After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as V_{DD} is provided in the specified range independent of V_{BB}.

5.1 Power Supply Modes

The following table shows all possible power supply modes for V_{BB}, V_{DD} and the pin LHI.

Power Supply Modes

VBB	0 V	0 V	0 V	0 V	13.5 V	13.5 V	13.5 V	13.5 V
VDD	0 V	0 V	5 V	5 V	0 V	0 V	5 V	5 V
LHI	0 V	5 V	0 V	5 V	0 V	5 V	0 V	5 V
PROFET operating	–	–	–	–	✓	✓	✓	✓
Limp home mode	–	–	–	–	–	✓	–	✓
SPI (logic)	reset	reset	✓	✓	reset	reset	✓	reset
Stand-by current	–	–	–	–	✓	–	–	–
Idle current	–	–	–	–	–	–	✓ 1)	–
Diagnosis	–	–	–	–	–	–	✓	✓ 2)

1) When all channels are in OFF-state and all SPI registers are at default values.

2) Current sense diagnosis not available in limp home mode.

To achieve stand-by mode, the limp home block must be disabled (LHI = 0 V), all channels must be switched off and the thermal latches have to be cleared. As a result the stand-by current $I_{BB(OFF)}$ is valid as listed. In case of active V_{DD} supply, the idle mode parameters are valid only, when additionally all SPI registers are at default values (see **Section 9.6**) e.g. after a reset command.

5.2 Reset

There are several reset trigger implemented in the device. They reset the SPI registers to their default values. The power stages as well as the analog watchdog block are not affected by the reset signals.

The first SPI transmission after any kind of reset contains at pin SO the read information from register `OUT`, and the transmission error bit `TER` is set.

Power-On Reset

The power-on reset is released, when V_{DD} voltage level is higher than $V_{DD(PO)}$. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `HWCR.RST` = 1, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time $t_{CS(td)}$.

Limp Home Mode

In limp home mode, the SPI write-registers are reset. The SPI interface is operating normally, so the limp home register bit LHI as well as the error flags can be read.

5.3 Electrical Characteristics

Electrical Characteristics Power Supply

Unless otherwise specified: V_{BB} = 9 V to 16 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C.
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
5.3.1	Operating voltage	V_{BB}	4.5	–	28	V	–
5.3.2	Stand-by current for whole device with loads	$I_{BB(OFF)}$				µA	V_{DD} = 0 V V_{LHI} = 0 V V_{IN} = 0 V
			–	1.2	3		T_j = 25 °C
			–	–	3		$T_j \leq$ 85 °C 1)
			–	–	50		T_j = 150 °C
	Idle current for whole device with loads	$I_{BB(idle)}$				µA	V_{DD} = 5 V V_{LHI} = 0 V V_{IN} = 0 V
			–	–	3		T_j = 25 °C
			–	–	3		$T_j \leq$ 85 °C 1)
			–	–	50		T_j = 150 °C
5.3.3	Logic supply voltage	V_{DD}	3.8	–	5.5	V	–
5.3.4	Logic supply current	I_{DD}	–	45	150	µA	V_{CS} = 0 V f_{SCLK} = 0 Hz
5.3.5	Logic idle current	$I_{DD(idle)}$	–	15	35	µA	$V_{CS} = V_{dd}$ f_{SCLK} = 0 Hz
5.3.6	Operating current for whole device	I_{GND}	–	10	20	mA	f_{SCLK} = 0 Hz
5.3.7	Power-On reset threshold voltage	$V_{DD(PO)}$	–	–	3.8	V	–
5.3.8	Power-On wake up time	$t_{WU(PO)}$	–	–	500	µs	–

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing at V_{BB} = 13.5 V, V_{DD} = 4.3 V and T_j = 25 °C.

5.4 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$	4	3	2	1	0
read	**RST**	**0**	**SBM**	**PWM**	**CTL**
write	**RST**	**0**	**0**	**PWM**	**CTL**

Field	Bits	Type	Description
RST	4	r	**Reset Command** **0** Normal operation 1 Device in reset due to limp home mode
RST	4	w	**Reset Command** **0** Normal operation 1 Execute reset command

6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs (DMOS) with charge pumps. There are five channels implemented in the device. Each channel can be switched on via an input pin or via SPI register `OUT`.

6.1 Output ON-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage V_{BB} as well as on the junction temperature T_j. **Figure 5** shows those dependencies. The behavior in reverse polarity mode is described in **Section 7.3**.

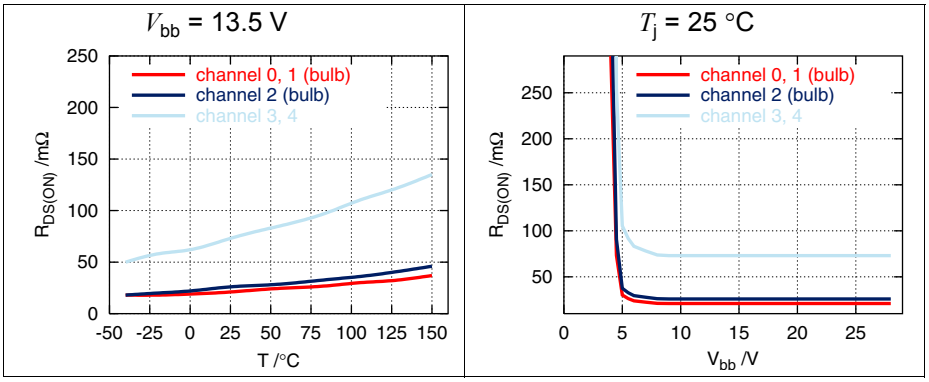


Figure 5 Typical On-State Resistance

6.2 Input Circuit

There are two ways of using the input pins in combination with the OUT SPI register by programming the `HWCR.PWM` parameter.

- `HWCR.PWM` = 0: A channel is switched on either by the according `OUT` register bit or the input pin.
- `HWCR.PWM` = 1: A channel is switched on by the according `OUT` register bit only, when the input pin is high. In this configuration, a PWM signal can be given to the input pin and the channel is activated by the SPI register `OUT`.

Figure 6 shows the complete input switch matrix.

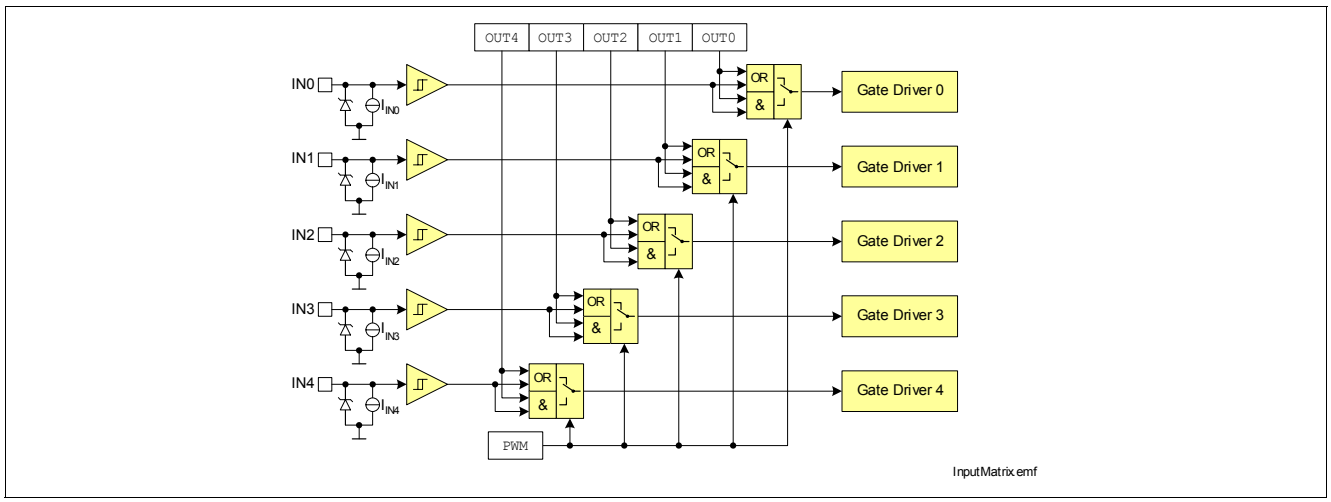


Figure 6 Input Switch Matrix

The current sink to ground at the input pins ensures that the input signal is low in case of an open input pin. The zener diode protects the input circuit against ESD pulses.

6.3 Power Stage Output

The power stages are built to be used in high side configuration (**Figure 7**).

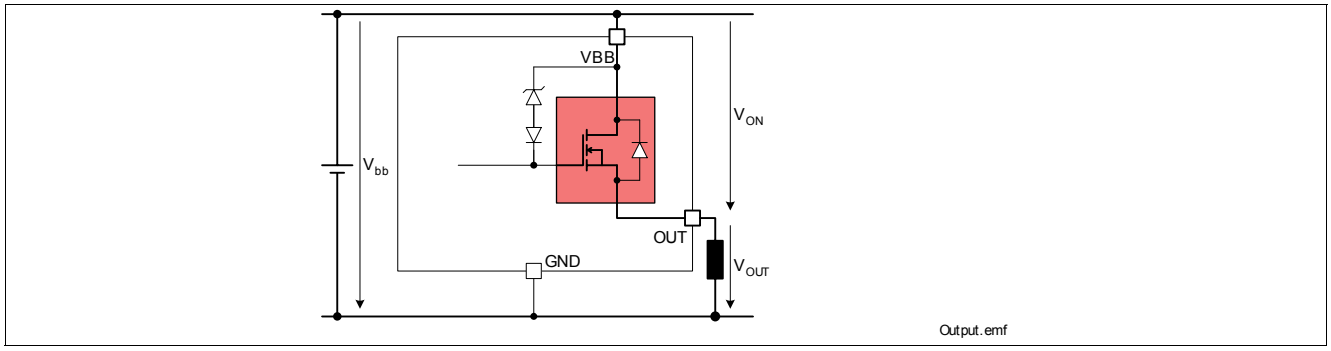


Figure 7 Power Stage Output

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission.

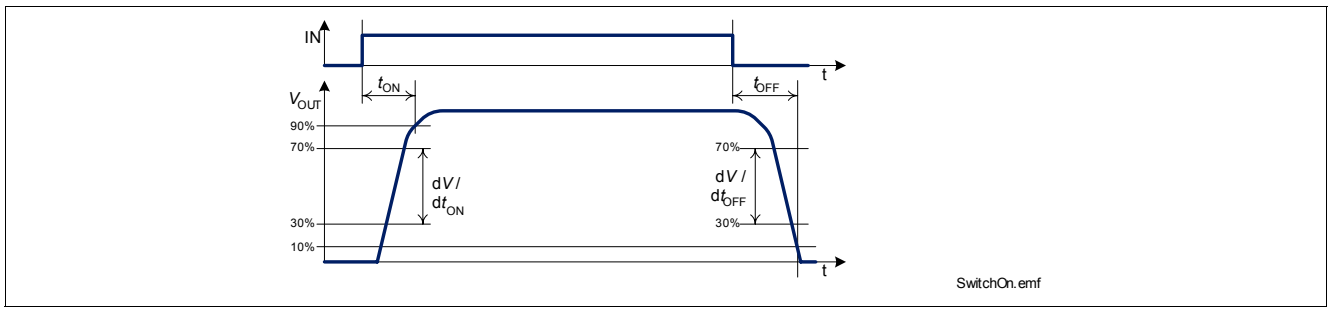


Figure 8 Switching a Load (resistive)

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent destruction of the device, there is a voltage clamp mechanism implemented that limits that negative output voltage to a certain level ($V_{ON(CL)}$ (**6.4.3**)). See **Figure 7** for details. The maximum allowed load inductance is limited.

6.4 Electrical Characteristics

Electrical Characteristic Power Stages

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C.
typical values: V_{BB} = 13.5 V, T_j = 25 °C.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output Characteristics							
6.4.1	On-State resistance	$R_{DS(ON)}$				mΩ	
	channel 0, 1		–	22.3	–		[1] T_j = 25 °, I_L = 2.6 A
			–	38	49		T_j = 150 °, I_L = 2.6 A
	channel 2		–	25.2	–		[1] T_j = 25 °C, I_L = 2.6 A
			–	49	64		T_j = 150 °C, I_L = 2.6 A
	channel 3, 4		–	72.9	–		[1] T_j = 25 °C, I_L = 1 A
			–	141	180		T_j = 150 °C,I_L = 1 A
6.4.2	Output voltage drop limitation at small load currents	$V_{DS(NL)}$				mV	
	channel 0, 1, 2		–	35	–		I_L = 35 mA
	channel 3, 4		–	35	–		I_L = 35 mA
6.4.3	Output clamp	$V_{ON(CL)}$	40	47	54	V	I_L = 20 mA
6.4.4	Output leakage current per channel	$I_{L(OFF)}$				µA	V_{IN} = 0 V `OUT.OUTn = 0`
	channel 0, 1		–	0.1	10		stand-by
			–	–	40		not stand-by
	channel 2		–	0.1	10		stand-by
			–	–	40		not stand-by
	channel 3, 4		–	0.1	8		stand-by
			–	–	40		not stand-by
6.4.5	Inverse current capability per channel	$-I_{L(IC)}$				A	No influence on functionality of unaffected channels [1]
	channel 0, 1, 2		–	2.5	–		–
	channel 3, 4		–	1.0	–		–
Thermal Resistance							
6.4.6	Junction to Case	R_{thJC}	–	–	20	K/W	[1]
6.4.7	Junction to Ambient, all channels active	R_{thJA}	–	40	–	K/W	[1] [2]
Input Characteristics							
6.4.8	L-input level	$V_{IN(L)}$	-0.3	–	1.0	V	–
6.4.9	H-input level	$V_{IN(H)}$	2.6	–	5.5	V	–
6.4.10	L-input current	$I_{IN(L)}$	3	25	75	µA	V_{IN} = 0.4 V
6.4.11	H-input current	$I_{IN(H)}$	10	40	75	µA	V_{IN} = 5 V

Electrical Characteristic Power Stages

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C.
typical values: V_{BB} = 13.5 V, T_j = 25 °C.

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Timings							
6.4.12	Turn-on time to 90% V_{BB}	t_{ON}				µs	V_{BB} = 13.5 V
	channel 0, 1, 2		–	–	250		R_L = 6.8 Ω
	channel 3, 4		–	–	250		R_L = 18 Ω
6.4.13	Turn-off time to 10% V_{BB}	t_{OFF}				µs	V_{BB} = 13.5 V
	channel 0, 1, 2		–	–	290		R_L = 6.8 Ω
	channel 3, 4		–	–	290		R_L = 18 Ω
6.4.14	Turn-on slew rate 30% to 70% V_{BB}	dV/dt_{ON}				V/µs	V_{BB} = 13.5 V
	channel 0, 1, 2		0.1	–	0.5		R_L = 6.8 Ω
	channel 3, 4		0.1	–	0.5		R_L = 18 Ω
6.4.15	Turn-off slew rate 70% to 30% V_{BB}	$-dV/dt_{OFF}$				V/µs	V_{BB} = 13.5 V
	channel 0, 1, 2		0.1	–	0.5		R_L = 6.8 Ω
	channel 3, 4		0.1	–	0.5		R_L = 18 Ω

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

6.5 Command Description

OUT
Output Configuration Registers

W/$\overline{R}$	RB	5	4	3	2	1	0
read/write	**0**	**0**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**

Field	Bits	Type	Description
OUTn n = 4 to 0	n	r/w	**Set Output Mode for Channel n** **0** Channel n is switched off 1 Channel n is switched on

HWCR
Hardware Configuration Register

W/$\overline{R}$	4	3	2	1	0
read	**RST**	**0**	**SBM**	**PWM**	**CTL**
write	**RST**	**0**	**0**	**PWM**	**CTL**

Field	Bits	Type	Description
PWM	1	rw	**PWM Configuration** **0** Input signal OR-combined with according `OUT` register bit 1 Input signal AND-combined with according `OUT` register bit

7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

7.1 Over Load Protection

The load current I_L is limited by the device itself in case of over load or short circuit to ground. There are multiple steps of current limitation which are selected automatically depending on the voltage V_{DS} across the power DMOS. Please note that the voltage at the OUT pin is V_{BB} - V_{DS}. Please refer to following figures for details.

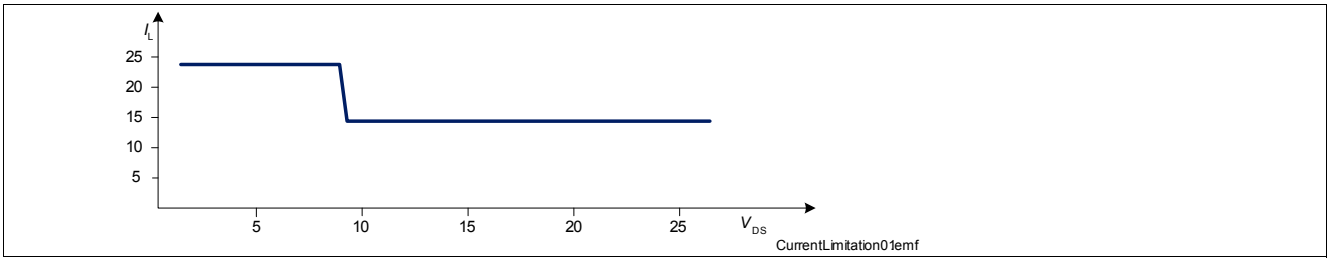


Figure 9 Current Limitation Channels 0, 1 (minimum values)

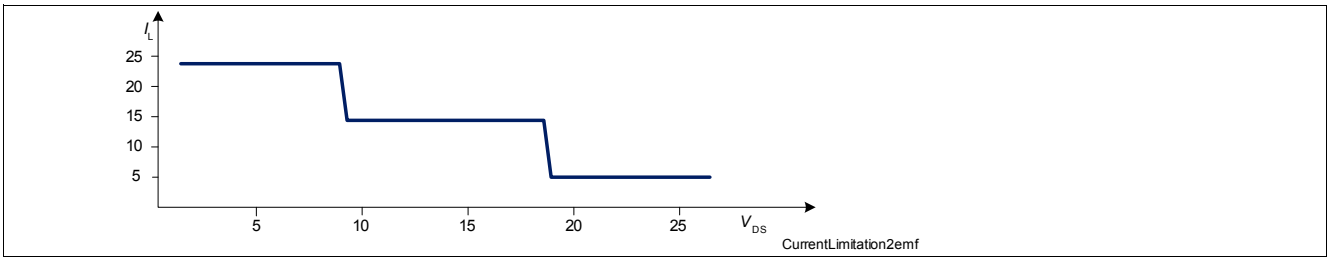


Figure 10 Current Limitation Channels 2 (minimum values)

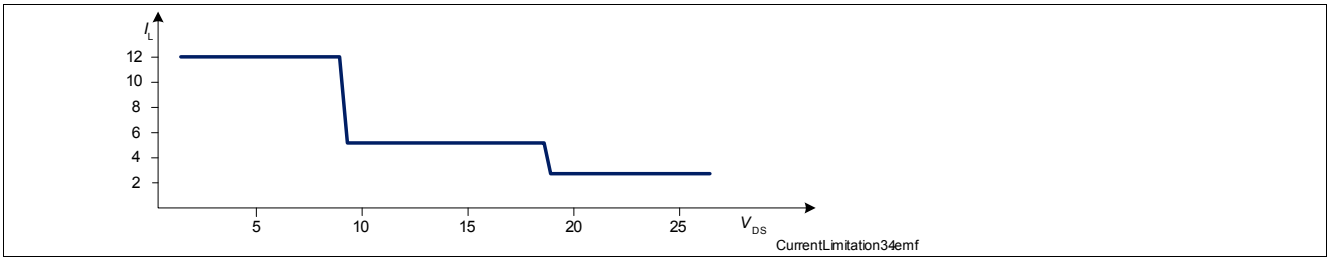


Figure 11 Current Limitation Channels 3, 4 (minimum values)

Current limitation to the value $I_{L(LIM)}$ is realized by increasing the resistance of the output channel, which leads to rapid temperature rise inside.

7.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel to switch off latched to prevent destruction (also even in case of V_{DD} = 0V). All over temperature latches are cleared by SPI command `HWCR.CTL` = 1.

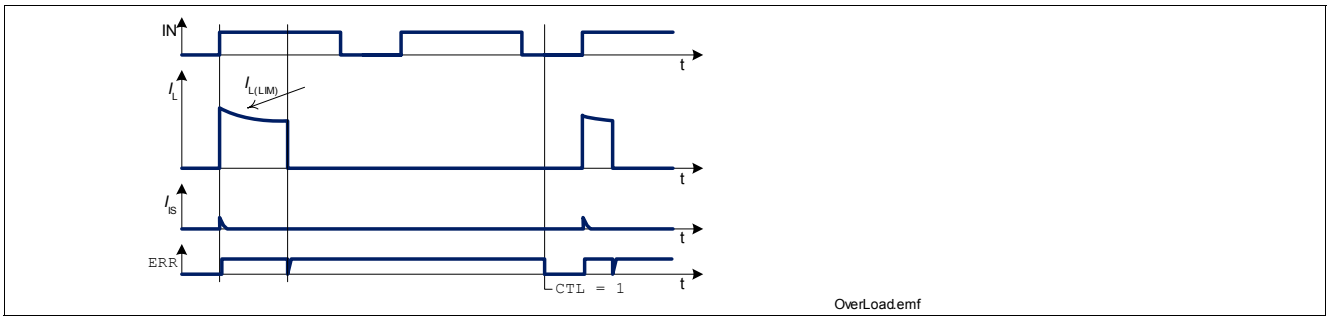


Figure 12 Shut Down by Over Temperature

7.3 Reverse Polarity Protection

In reverse polarity mode, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads. The current trough the ground pin, sense pin IS, the logic power supply pin VDD, the SPI pins and the watchdog pins has to be limited as well (please refer to the maximum ratings listed on **Page 10**).

Note: No other protection mechanism such as temperature protection or current limitation is active during reverse polarity.

7.4 Over Voltage Protection

In addition to the output clamp for inductive loads as described in **Section 6.3**, there is a clamp mechanism available for over voltage protection. The current through the ground connection has to be limited during over voltage. Please note that in case of over voltage the pin GND may have a high voltage offset to the module ground.

7.5 Loss of Ground

In case of complete loss of the device ground connections, but connected load ground, the SPOC - BTS5566G securely changes to or stays in off-state.

7.6 Loss of V_{bb}

In case of loss of V_{bb} connection in on-state, all inductance of the loads has to be demagnetized through the ground connection or through an additional path from VBB to ground. When a diode is used in the ground path for reverse polarity reasons, the ground connection is not available for demagnetization. Then for example, a resistor can be placed in parallel to the diode or a suppressor diode can be used between VBB and GND.

7.7 Electrical Characteristics

Electrical Characteristics Protection Functions
Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
7.7.1	Load current limitation	$I_{L(LIM)}$				A	V_{DS} = 7 V
	channel 0		24	–	48[1)]		–
	channel 1		24	–	48[1)]		–
	channel 2		24	–	48[1)]		–
	channel 3		12	–	27[1)]		–
	channel 4		12	–	27[1)]		–
7.7.2	Initial short circuit shut down time	$t_{OFF(SC)}$				µs	T_{jStart} = 25 °C [1)]
	channel 0, 1		–	550	–		–
	channel 2		–	400	–		–
	channel 3, 4		–	400	–		–
Over Temperature Protection							
7.7.3	Thermal shut down temperature	$T_{j(SC)}$	150	170[1)]	–	°C	–
7.7.4	Thermal hysteresis	ΔT_j	–	7	–	K	[1)]
Reverse Battery							
7.7.5	Drain-Source diode voltage (V_{OUT} > V_{bb})	$-V_{DS(rev)}$				mV	T_j = 150 °C
	channel 0, 1		–	600	–		I_L = -2.5 A
	channel 2		–	620	–		I_L = -2.5 A
	channel 3, 4		–	600	–		I_L = -1 A
Over Voltage							
7.7.6	Overvoltage protection	$V_{BB(AZ)}$	40	47	54	V	I_{BB} = 4 mA
Loss of GND protection							
7.7.7	Output current while GND disconnected	$I_{L(GND)}$	–	–	1	mA	[1)]

1) Not subject to production test, specified by design.

7.8 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$	4	3	2	1	0
read	**RST**	**0**	**SBM**	**PWM**	**CTL**
write	**RST**	**0**	**0**	**PWM**	**CTL**

Field	Bits	Type	Description
CTL	0	rw	**Clear Thermal Latch** **0** Thermal latches are untouched 1 Command: Clear all thermal latches

8 Diagnosis

For diagnosis purpose, the SPOC - BTS5566G provides a current sense signal and the diagnosis word at SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage.

Please refer to **Figure 13** for details.

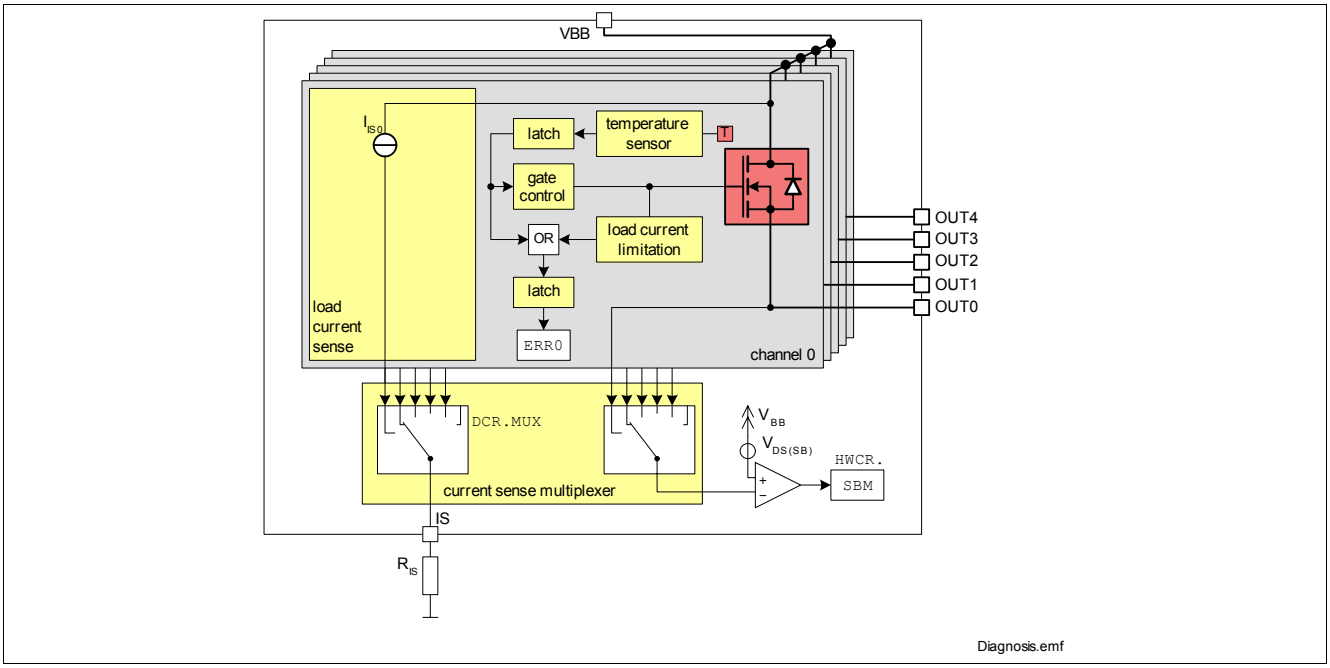


Figure 13 Block Diagram: Diagnosis

For diagnosis feedback at different operation modes, please see following table.

Table 1 Operation Modes [1)]

Operation Mode	Input Level OUT.OUTn	Output Level V_{OUT}	Current Sense I_{IS}	Error Flag ERRn[2)]	HWCR. SBM
Normal Operation (OFF)	L / 0 (OFF-state)	GND	Z	0	1
Short Circuit to GND		GND	Z	0	1
Over Temperature		Z	Z	0	x
Short Circuit to V_{BB}		V_{BB}	Z	0	0
Open Load		Z	Z	0	x
Normal Operation (ON)	H / 1 (ON-state)	~V_{BB}	I_L / k_{ILIS}	0	0
Current Limitation		< V_{BB}	Z	1	x
Short Circuit to GND		~GND	Z	1	1
Over Temperature		Z	Z	1[3)]	x
Short Circuit to V_{BB}		V_{BB}	< I_L / k_{ILIS}	0	0
Open Load		V_{BB}	Z	0	0

1) L = low level, H = high level, Z = high impedance, potential depends on leakage currents and external circuit x = undefined
2) The error flags are latched until they are transmitted in the standard diagnosis word via SPI
3) The over temperature flag is set latched and can be cleared by SPI command HWCR.CTL

8.1 Diagnosis Word at SPI

The standard diagnosis at the SPI interface provides information about each channel. The error flags, an OR combination of the over temperature flags and the over load monitoring signals are provided in the SPI standard diagnosis bits `ERRn`.

The over load monitoring signals are latched in the error flags and cleared each time the standard diagnosis is transmitted via SPI. In detail, they are cleared between the second and third raising edge of the SCLK signal.

The over temperature flags, which cause an overheated channel to stay switched off, are latched directly at the gate control block. The latches are cleared by SPI command `HWCR.CTL`.

Please note:

The over temperature information is latched twice. When transmitting a clear thermal latch command (`HWCR.CLT`), the error flag is cleared during command transmission of the next SPI frame and ready for latching after the third raising edge of the SCLK signal. As a result, the first standard diagnosis information after a `CTL` command will indicate a failure mode at the previously affected channels although the thermal latches have been cleared already. In case of continuous over load, the error flags are set again immediately because of the over load monitoring signal.

In case of high duty cyle (off state of output < $t_{off\text{-}state\_min}$) the V_{DS} might not be equal to V_{DD} during the off state of the power Mosfet. The over load monitoring signals might be set and latched in the error flags. See Application Note “Software Strategy for Diagnosis during PWM-Operation“ for more details.

8.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

The current sense signal (ratio $k_{ILIS} = I_L / I_S$) is provided as long as no failure mode occurs. Usually a resistor R_{IS} is connected from the current sense pin to GND. It is recommended to use resistors 2.5 kΩ <R_{IS} < 7 kΩ. A typical value is 3.3 kΩ.

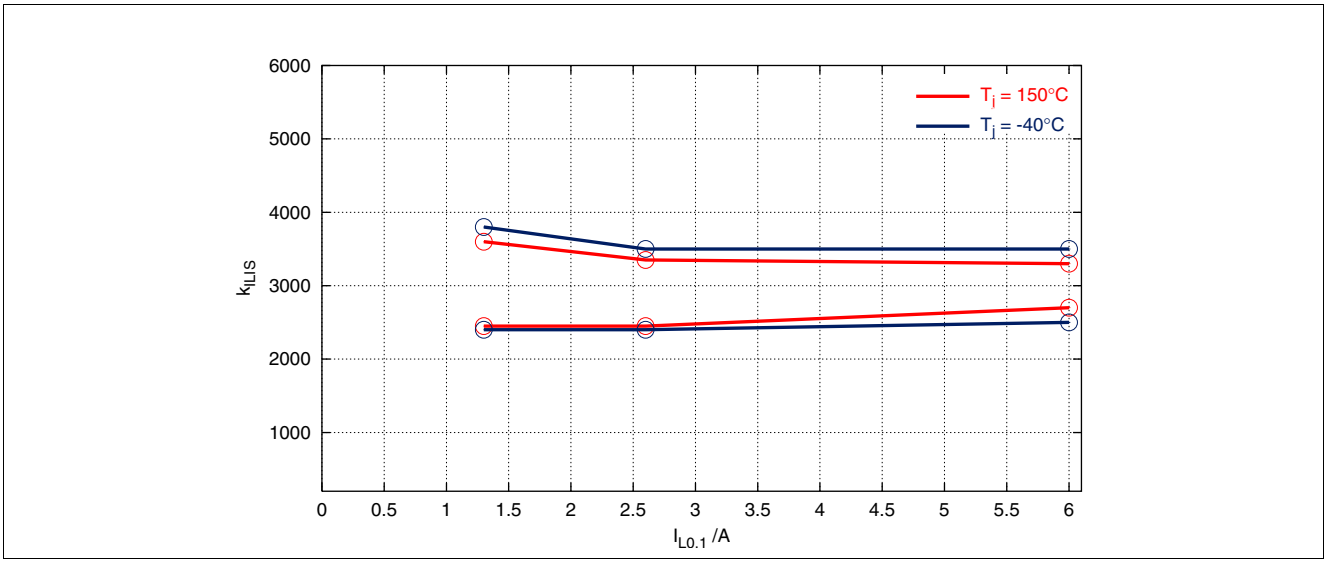


Figure 14 Current Sense Ratio k_{ILIS} Channel 0,1 [1)]

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 8.4** (Position **8.4.1**).

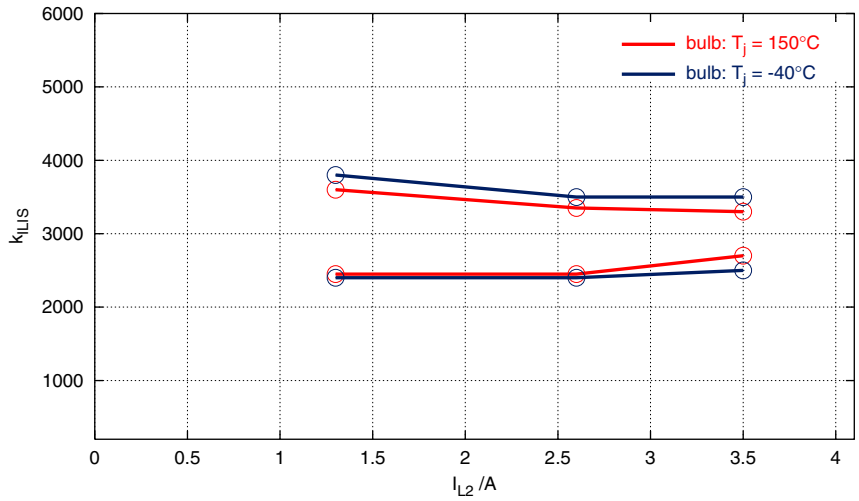
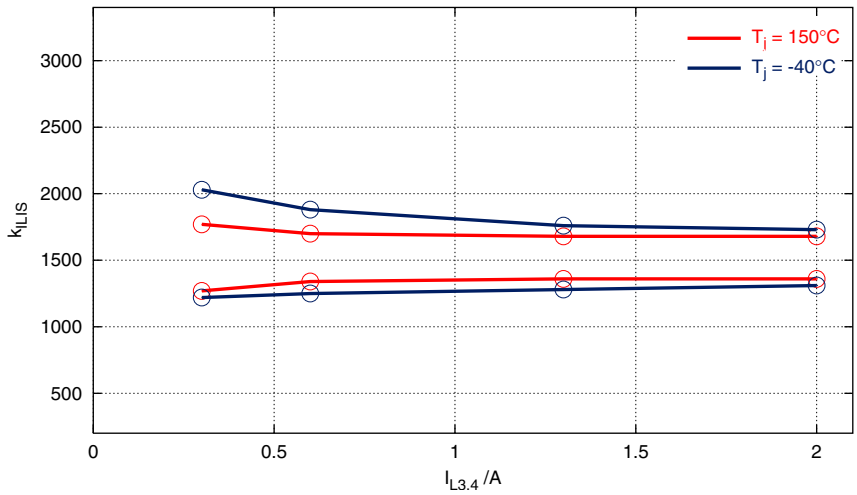


Figure 15 Current Sense Ratio k_{ILIS} Channel 2 [1)]

Figure 16



Current Sense Ratio k_{ILIS} Channel 3, 4 [1)]

In case of over current as well as over temperature, the current sense signal of the affected channel is switched off. To distinguish between over temperature and over load, the SPI diagnosis word can be used. Whereas the over load flag is cleared every time the diagnosis is transmitted, the over temperature flag is cleared by a dedicated SPI command (`HWCR.CTL`).

Details about timings between the current sense signal I_{IS} and the output voltage V_{OUT} and the load current I_L can be found in **Figure 17**.

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 8.4** (Position **8.4.1**).

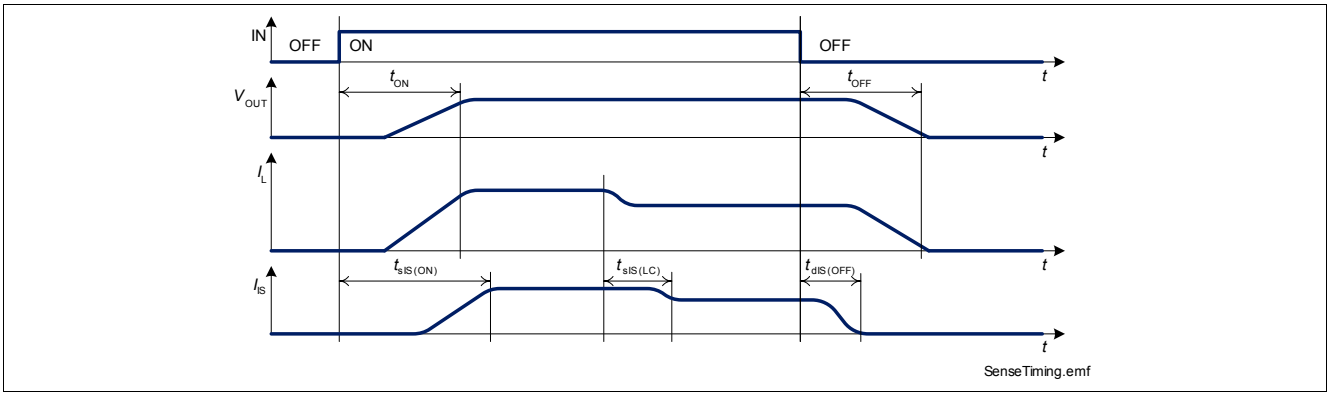


Figure 17 Timing of Current Sense Signal

Current Sense Multiplexer

There is a current sense multiplexer implemented in the SPOC - BTS5566G that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register `DCR.MUX`. The sense current also can be disabled by SPI register `DCR.MUX`. For details on timing of the current sense multiplexer, please refer to **Figure 18**.

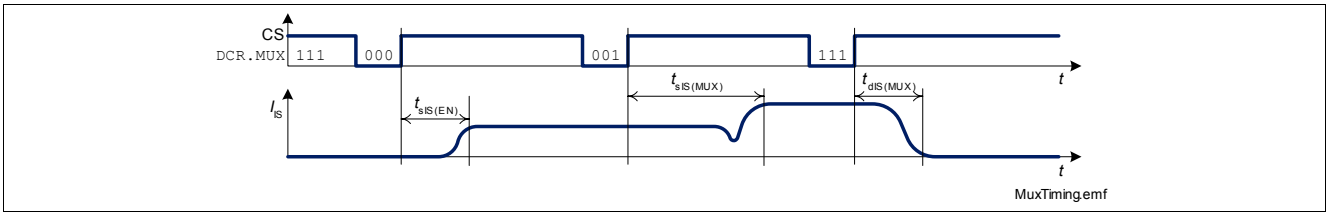


Figure 18 Timing of Current Sense Multiplexer

8.3 Switch Bypass Diagnosis

To detect short circuit to V_{DD}, there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and V_{BB} in ON-state, the current will flow through the power transistor as well as through the short circuit (bypass) with undefined ratio. As a result, the current sense signal will show lower values than expected by the load current. In OFF-state, the output voltage will stay close to V_{BB} potential which means a small V_{DS}.

The switch bypass monitor compares the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (`DCR.MUX`) with threshold $V_{DS(SB)}$. The result of comparison can be read in SPI register `HWCR.SBM`. The switch bypass monitor is active in ON- as well as in OFF-state.

8.4 Electrical Characteristics

Electrical Characteristics Diagnosis

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Load Current Sense							
8.4.1	Current sense ratio channel 0, 1:	k_{ILIS}					
	I_L = 1.3 A		2400	3100	3800		T_j = -40 °C
	I_L = 2.6 A		2400	3000	3500		–
	I_L = 6.0 A		2500	3000	3500		–
	I_L = 1.3 A		2450	3030	3600		T_j = 150 °C
	I_L = 2.6 A		2450	3000	3350		–
	I_L = 6.0 A		2700	3000	3300		–
	channel 2:						
	I_L = 1.3 A		2400	3100	3800		T_j = -40 °C
	I_L = 2.6 A		2400	3000	3500		–
	I_L = 3.5 A		2500	3000	3500		–
	I_L = 1.3 A		2450	3000	3600		T_j = 150 °C
	I_L = 2.6 A		2450	3000	3350		–
	I_L = 3.5 A		2700	3000	3300		–
	channel 3, 4:						
	I_L = 0.3 A		1220	1625	2030		T_j = -40 °C
	I_L = 0.6 A		1250	1565	1880		–
	I_L = 1.3 A		1280	1520	1760		–
	I_L = 2.0 A		1310	1520	1730		–
	I_L = 0.3 A		1270	1520	1770		T_j = 150 °C
	I_L = 0.6 A		1340	1520	1700		–
	I_L = 1.3 A		1360	1520	1680		–
	I_L = 2.0 A		1360	1520	1680		–
8.4.2	Current sense voltage limitation	$V_{IS(LIM)}$	-8%	V_{dd}	8%	V	I_{IS} = 1 mA
8.4.3	Current sense leakage / offset current	$I_{IS(en)}$	–	–	2	µA	I_L = 0 DCR.MUX = 000_B
8.4.4	Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	–	1	µA	$I_L = I_{L(nom)}$ DCR.MUX = 111_B
8.4.5	Current sense settling time after channel activation	$t_{sIS(ON)}$	–	–	300	µs	V_{BB} = 13.5 V $I_L = I_{L(nom)}$ R_{IS} = 4.7 kΩ
8.4.6	Current sense desettling time after channel deactivation	$t_{dIS(OFF)}$	–	–	25	µs	V_{BB} = 13.5 V [1)] $I_L = I_{L(nom)}$ R_{IS} = 4.7 kΩ

Electrical Characteristics Diagnosis

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
8.4.7	Current sense settling time after change of load current	$t_{sIS(LC)}$				µs	V_{BB} = 13.5 V [1] R_{IS} = 4.7 kΩ
	channel 0, 1, 2		–	–	30		I_L = 1.3 A to 2.6 A
	channel 3, 4		–	–	30		I_L = 0.6 A to 1.3 A
8.4.8	Current sense settling time after current sense activation	$t_{sIS(EN)}$	–	–	25	µs	R_{IS} = 4.7 kΩ DCR.MUX:111_B -> 000_B
8.4.9	Current sense settling time after multiplexer channel change	$t_{sIS(MUX)}$	–	–	30	µs	R_{IS} = 4.7 kΩ DCR.MUX:000_B -> 001_B
8.4.10	Current sense deactivation time	$t_{dIS(MUX)}$	–	–	25	µs	[1] R_{IS} = 4.7 kΩ DCR.MUX: 001_B -> 111_B
8.4.11	Off state time during PWM operation	$t_{off\ state\_min}$	350	–	–	µs	–
Switch Bypass Monitor							
8.4.12	Switch bypass monitor threshold	$V_{DS(SB)}$	0.7	–	2.5	V	–

1) Not subject to production test, specified by design.

8.5 Command Description

DCR
Diagnosis Control Registers

4	3	2	1	0
0	**0**		**MUX**	

Field	Bits	Type	Description
MUX	2:0	rw	**Set Current Sense Multiplexer Configuration** 000 current sense of channel 0 is routed to IS pin 001 current sense of channel 1 is routed to IS pin 010 current sense of channel 2 is routed to IS pin 011 current sense of channel 3 is routed to IS pin 100 current sense of channel 4 is routed to IS pin 101 IS pin is high impedance 110 IS pin is high impedance **111** IS pin is high impedance

HWCR
Hardware Configuration Register

W/$\overline{R}$	4	3	2	1	0
read	**RST**	**0**	SBM	**PWM**	**CTL**
write	**RST**	**0**	0	**PWM**	**CTL**

Field	Bits	Type	Description
SBM	2	r	**Switch Bypass Monitor**[1)] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$

1) Invalid in stand-by mode

Standard Diagnosis

CS	7	6	5	4	3	2	1	0
TER	**0**	**LHI**	**0**	**ERR4**	**ERR3**	**ERR2**	**ERR1**	**ERR0**

Field	Bits	Type	Description
ERRn n = 4 to 0	n	r	**Error flag Channel n** 0 normal operation 1 failure mode occurred

9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

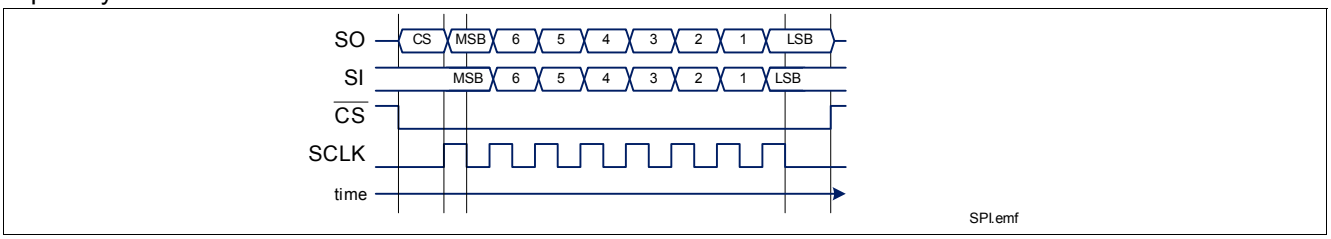


Figure 19 Serial Peripheral Interface

9.1 SPI Signal Description

$\overline{CS}$ - Chip Select:

The system micro controller selects the SPOC - BTS5566G by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition:

- The requested information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. This information stays available to the first rising edge of SCLK.

$\overline{CS}$ Low to High transition:

- Command decoding is only done, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input:

Serial input data bits are shifted-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Section 9.5** for further information.

SO Serial Output:

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 9.5** for further information.

9.2 Daisy Chain Capability

The SPI of SPOC - BTS5566G provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 20**), in order to build a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

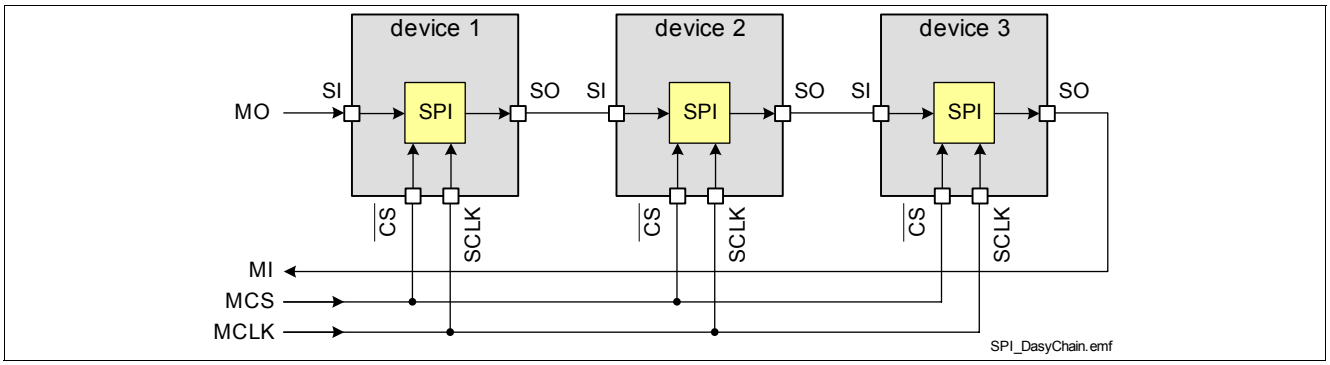


Figure 20 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out occures at the SO pin. After eight SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must turn high to make the device accept the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times eight bits have to be shifted through the devices. After that, the $\overline{MCS}$ line must turn high (see **Figure 21**).

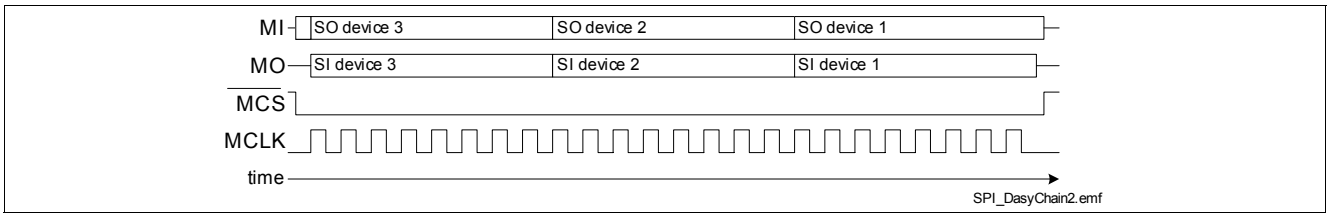


Figure 21 Data Transfer in Daisy Chain Configuration

9.3 Timing Diagrams

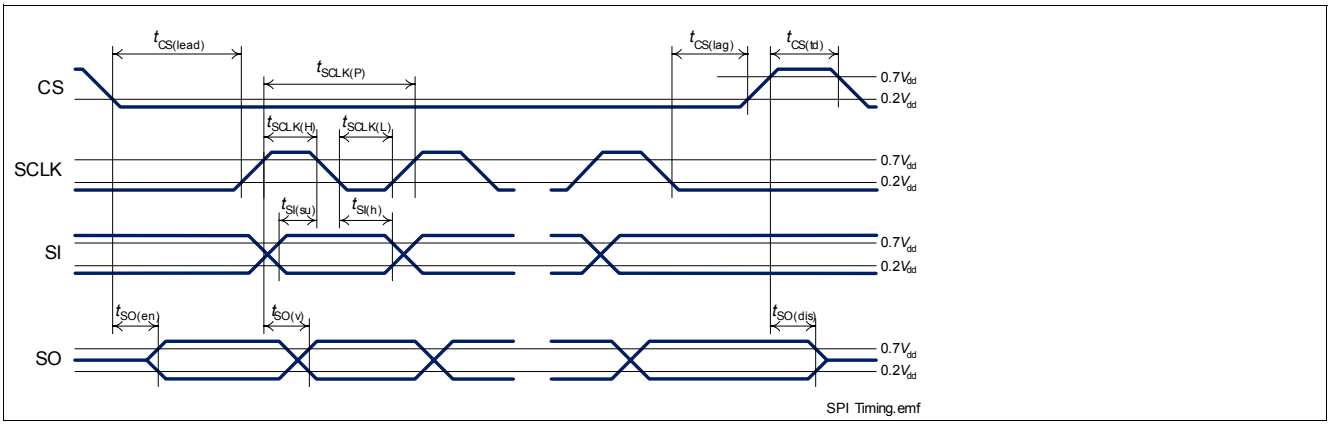


Figure 22 Timing Diagram SPI Access

9.4 Electrical Characteristics

Electrical Characteristics SPI

Unless otherwise specified: V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C, V_{dd} = 3.8 V to 5.5 V
typical values: V_{bb} = 13.5 V, T_j = 25 °C, V_{dd} = 4.3 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
9.4.1	L level of pin					V	V_{DD} = 4.3 V
	$\overline{CS}$	$V_{CS(L)}$	-0.3	–	1.0		–
	SCLK	$V_{SCLK(L)}$	-0.3	–	1.0		–
	SI	$V_{SI(L)}$	-0.3	–	1.0		–
9.4.2	H level of pin					V	V_{DD} = 4.3 V
	$\overline{CS}$	$V_{CS(H)}$	2.6	–	5.5		–
	SCLK	$V_{SCLK(H)}$	2.6	–	5.5		–
	SI	$V_{SI(H)}$	2.6	–	5.5		–
9.4.3	L-input pull-up current at $\overline{CS}$ pin	$I_{CS(L)}$	10	30	85	µA	V_{DD} = 4.3 V, V_{CS} = 0 V
9.4.4	H-input pull-up current at $\overline{CS}$ pin	$I_{CS(H)}$	3	–	85	µA	V_{DD} = 4.3 V, V_{CS} = 2.6 V
9.4.5	L-input pull-down current at pin					µA	V_{DD} = 4.3 V
	SCLK	$I_{SCLK(L)}$	3	–	75		V_{SCLK} = 0.4 V
	SI	$I_{SI(L)}$	3	–	75		V_{SI} = 0.4 V
9.4.6	H-input pull-down current at pin					µA	V_{DD} = 4.3 V
	SCLK	$I_{SCLK(H)}$	10	30	75		V_{SCLK} = 4.3 V
	SI	$I_{SI(H)}$	10	30	75		V_{SI} = 4.3 V
Output Characteristics (SO)							
9.4.7	L level output voltage	$V_{SO(L)}$	0	–	0.5	V	I_{SO} = -0.5 mA
9.4.8	H level output voltage	$V_{SO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{SO} = 0.5 mA, V_{DD} = 4.3 V
9.4.9	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} = V_{DD}
Timings							
9.4.10	Serial clock freqency	f_{SCLK}	0	–	2	MHz	–
9.4.11	Serial clock period	$t_{SCLK(P)}$	500	–	–	ns	–
9.4.12	Serial clock high time	$t_{SCLK(H)}$	250	–	–	ns	–
9.4.13	Serial clock low time	$t_{SCLK(L)}$	250	–	–	ns	–
9.4.14	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	1	–	–	µs	–
9.4.15	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	1	–	–	µs	–
9.4.16	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	1	–	–	µs	–
9.4.17	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	100	–	–	ns	–
9.4.18	Data hold time (falling SCLK to SI)	$t_{SI(h)}$	100	–	–	ns	–
9.4.19	Output enable time (falling $\overline{CS}$ to SO valid)	$t_{SO(en)}$	–	–	1	µs	C_L = 20 pF [1)]

Electrical Characteristics SPI

Unless otherwise specified: V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C, V_{dd} = 3.8 V to 5.5 V
typical values: V_{bb} = 13.5 V, T_j = 25 °C, V_{dd} = 4.3 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
9.4.20	Output disable time (rising $\overline{CS}$ to SO tri-state)	$t_{SO(dis)}$	–	–	1	µs	C_L = 20 pF [1]
9.4.21	Output data valid time with capacitive load	$t_{SO(v)}$	–	–	250	ns	C_L = 20 pF [1]

1) Not subject to production test, specified by design.

9.5 SPI Protocol

	CS[1]	7	6	5	4	3	2	1	0
		Write Register							
SI		1	ADDR		DATA				
		Read Register							
SI		0	ADDR		x	x	x	x	0
		Read Standard Diagnosis							
SI		0	x	x	x	x	x	x	1
		Standard Diagnosis							
SO	TER	0	LHI	X	ERR4	ERR3	ERR2	ERR1	ERR0
		Second Frame of Read Command							
SO	TER	1	ADDR		DATA				

1) The SO pin shows this information between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame.

Field	Bits	Type	Description
TER	CS	r	**Transmission Error** 0 Previous transmission was successful (modulo 8 clocks received) **1** Previous transmission failed or first transmission after reset
ADDR	6:5	rw	**Address** Pointer to register for read and write command
DATA	4:0	rw	**Data** Data written to or read from register selected by address ADDR
LHI	6	r	**Limp Home Input Pin** 0 L-input signal at pin LHI 1 H-input signal at pin LHI
ERRx x = 4 to 0	x	r	**Diagnosis of Channel x** **0** No failure 1 Over temperature, over load or short circuit

9.6 Register Overview

Name	W/$\overline{R}$	Addr	4	3	2	1	0	default[1]
OUT	W/R	00_B	OUT4	OUT3	OUT2	OUT1	OUT0	00_H
HWCR	R	10_B	RST	X	SBM	PWM	CTL	00_H
	W	10_B	RST	0	0	PWM	CTL	00_H
DCR	W/R	11_B	0	0	MUX			07_H

1) The default values are set after reset.

10 Application Description

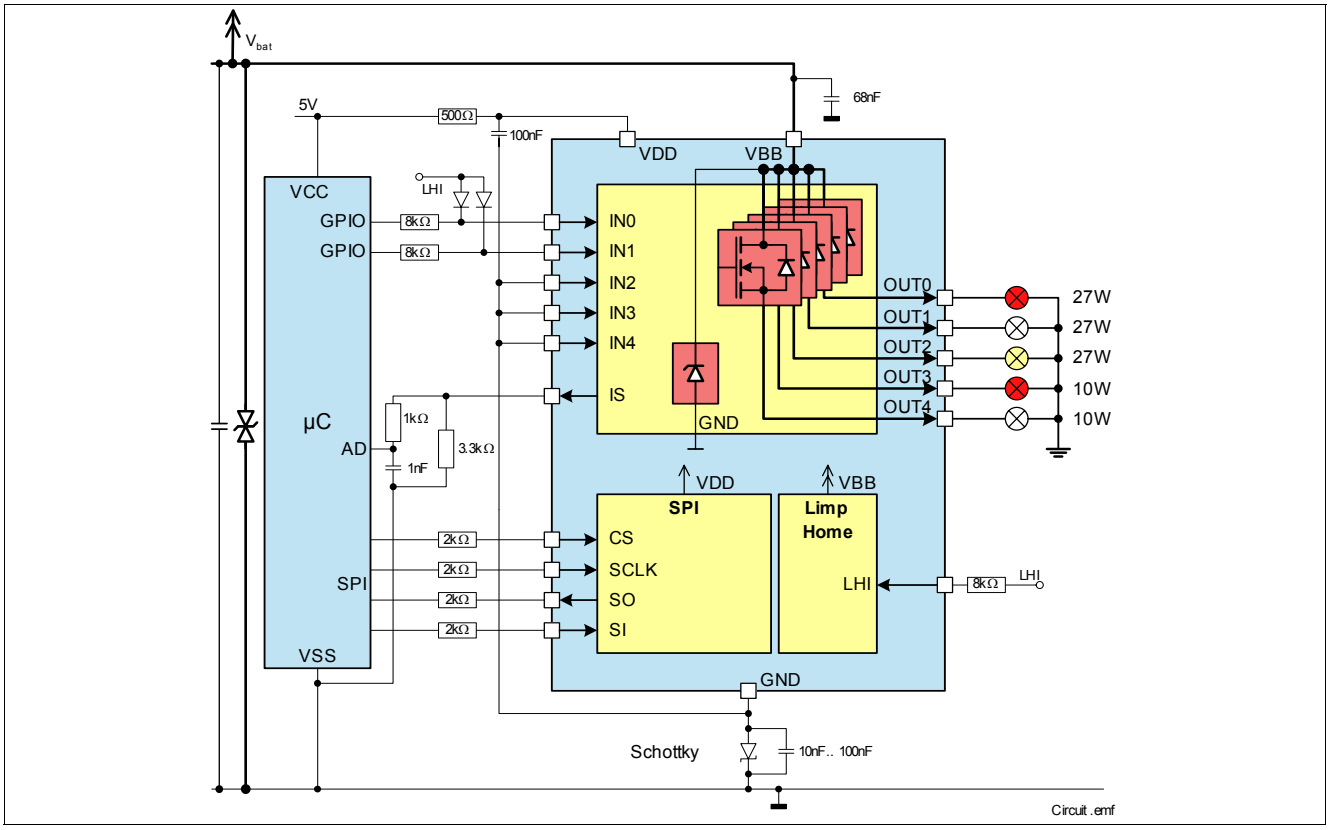


Figure 23 Application Circuit Example

11 Package Outlines SPOC - BTS5566G

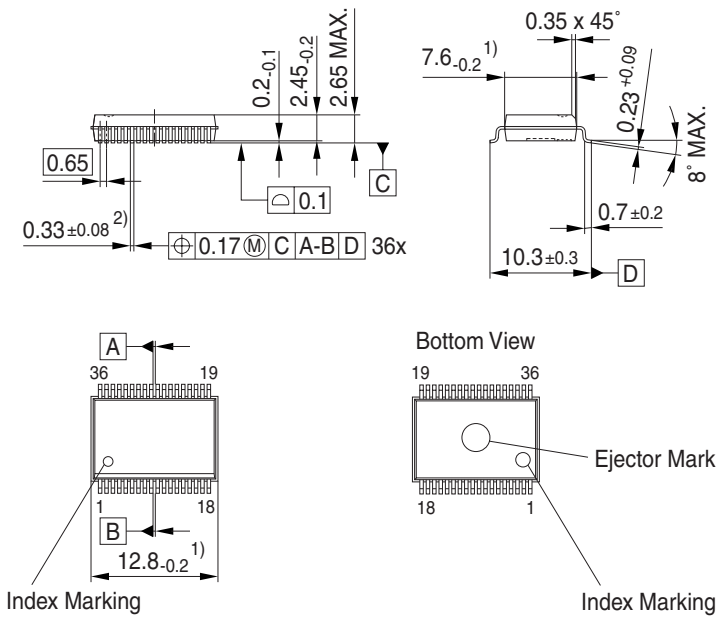


Figure 24 PG-DSO-36-34 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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Dimensions in mm

12 Revision History

Revision	Date	Changes
1.3	07-10-30	• Chapter 11 Package outline drawing changed
1.2	07-08-28	• 4.1 Conditions updated • 4.1 and 6.4 : footnote change to : Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). • 4.1.4 Conditions updated • 4.1.28 Definition change • 5.2 Reset Command : $t_{CS(td)}$ change to : $t_{CS(td)}$. • 8.4.1 Kilis : updated values for Channel 2-3 • 8.4.3 New parameter : Current sense leakage / offset current • Max Input Voltage value change to 40 Volts
1.1	07-03-05	• Product summary Green Product (ROHS compliant) and AEC Qualified added • 4.1.12 Current through input pins min value change to -0.75mA • 4.1.21 Current through limp home input pin min value change to -0.75mA • Chapter 2 Test pin change to Vbb • Chapter 6 R_{on} definition changed • Chapter 7.2 (also even in case of V_{dd} = 0V) added. • Basic Feature : Green Logo added • Chapter 8.1 In case of high duty cyle (off state of output < $t_{off\ state\_min}$) the V_{DS} might not be equal to V_{BB} during the off state of the power Mosfet. The over load monitoring signals might be set and latched in the error flags. See Application Note “ Software Strategy for Diagnosis during PWM-Operation“ for more details • Table 8.4.10 Off stateTime during PWM operation definition • Chapter 11 68nF added between V_{BB} and Gnd • page 18: register read value added • New template DIN A4 V1.2

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