

Smart Two Channel Highside Power Switch

Features

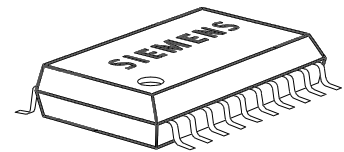
- Overload protection
- Current limitation
- Short-circuit protection
- Thermal shutdown
- Overvoltage protection (including load dump)
- Reverse battery protection¹⁾
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Open drain diagnostic output
- Open load detection in ON-state
- CMOS compatible input
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge (ESD) protection

Product Summary

Overvoltage Protection	$V_{bb(AZ)}$	43	V
Operating voltage	$V_{bb(on)}$	5.0 ... 24	V
active channels:		one	two parallel
On-state resistance	R_{ON}	40	20
Nominal load current	$I_{L(NOM)}$	4.8	7.3
Current limitation	$I_{L(SCr)}$	21	21

Application

- μ C compatible power switch with diagnostic feedback for 12 V DC grounded loads
- Most suitable for resistive and lamp loads
- Replaces electromechanical relays, fuses and discrete circuits



General Description

N channel vertical power FET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology. Fully protected by embedded protection functions.

Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12, 15,16, 19,20	V_{bb}	Positive power supply voltage. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
3	IN1	Input 1,2 , activates channel 1,2 in case of
7	IN2	logic high signal
17,18	OUT1	Output 1,2 , protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current
13,14	OUT2	
4	ST1	Diagnostic feedback 1,2 of channel 1,2, open drain, low on failure
8	ST2	
2	GND1	Ground 1 of chip 1 (channel 1)
6	GND2	Ground 2 of chip 2 (channel 2)
5,9	N.C.	Not Connected

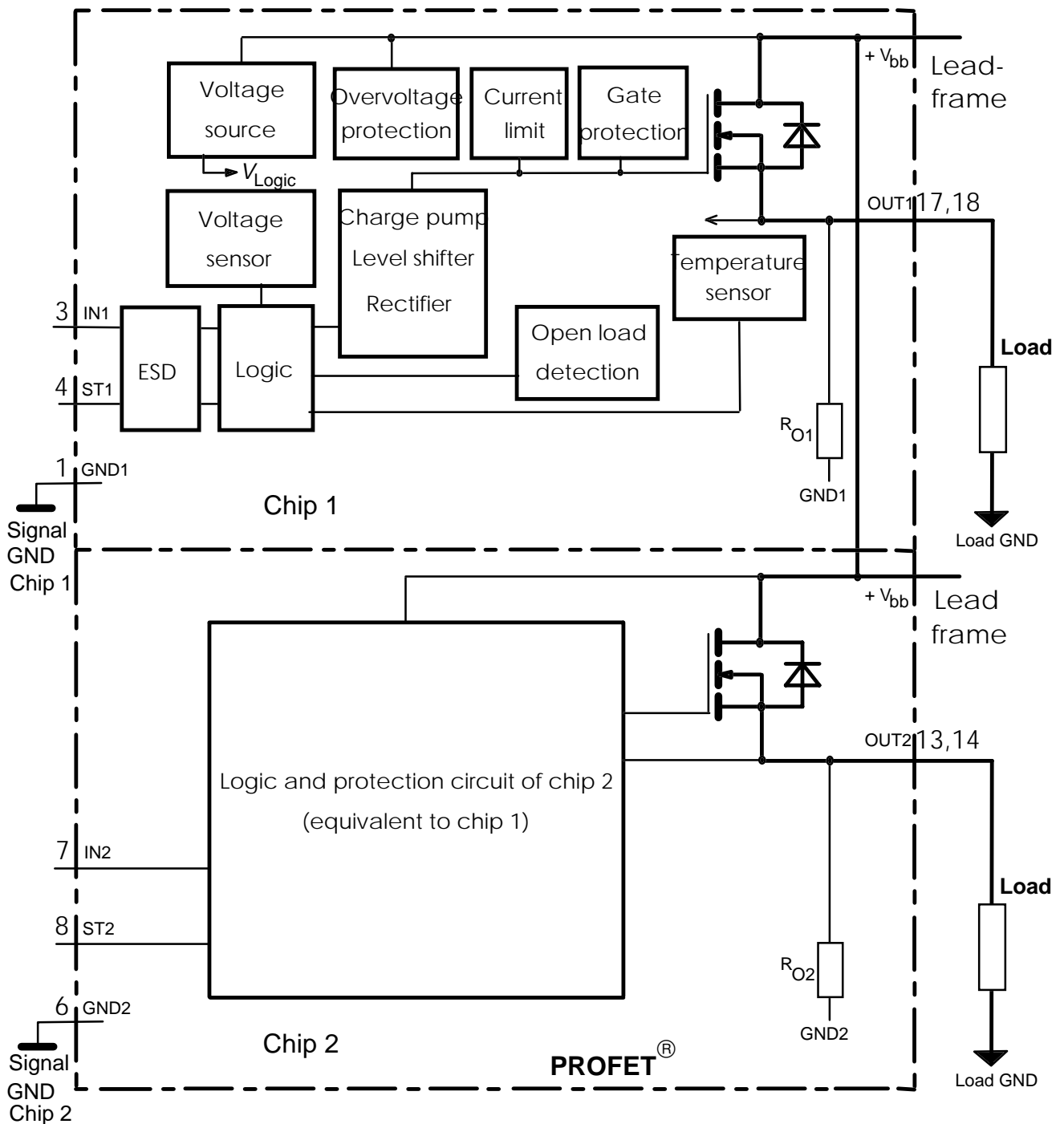
Pin configuration (top view)

V_{bb}	1	20	V_{bb}
GND1	2	19	V_{bb}
IN1	3	18	OUT1
ST1	4	17	OUT1
N.C.	5	16	V_{bb}
GND2	6	15	V_{bb}
IN2	7	14	OUT2
ST2	8	13	OUT2
N.C.	9	12	V_{bb}
V_{bb}	10	11	V_{bb}

¹⁾ With external current limit (e.g. resistor $R_{GND}=150 \Omega$) in GND connection, resistor in series with ST connection, reverse load current limited by connected load.

Block diagram

Two Channels; Open Load detection in on state;



Leadframe connected to pin 1, 10, 11, 12, 15, 16, 19, 20

Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 4)	V_{bb}	43	V
Supply voltage for full short circuit protection $T_{j,start} = -40 \dots +150^\circ\text{C}$	V_{bb}	24	V

Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Values	Unit
Load current (Short-circuit current, see page 5)	I_L	self-limited	A
Load dump protection ²⁾ $V_{\text{LoadDump}} = U_A + V_s$, $U_A = 13.5\text{ V}$ $R_l^3) = 2\ \Omega$, $t_d = 200\text{ ms}$; IN = low or high, each channel loaded with $R_L = 2.8\ \Omega$,	$V_{\text{LoadDump}}^4)$	60	V
Operating temperature range	T_j	-40 ... +150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 ... +150	
Power dissipation (DC) ⁵⁾ (all channels active)	$T_a = 25^\circ\text{C}$: $T_a = 85^\circ\text{C}$: P_{tot}	3.8 2.0	W
Electrostatic discharge capability (ESD) (Human Body Model)	V_{ESD}	1.0	kV
Input voltage (DC)	V_{IN}	-10 ... +16	V
Current through input pin (DC)	I_{IN}	± 2.0	mA
Current through status pin (DC) see internal circuit diagram page 8	I_{ST}	± 5.0	

Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit
		min	typ	max	
Thermal resistance junction - soldering point ^{5),6)} each channel:	R_{thjs}	--	--	11	K/W
junction - ambient ⁵⁾ one channel active:	R_{thja}	--	40	--	
all channels active:		--	33	--	

Electrical Characteristics

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$, $V_{\text{bb}} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

Load Switching Capabilities and Characteristics

On-state resistance (V_{bb} to OUT) $I_L = 2\text{ A}$ each channel, $T_j = 25^\circ\text{C}$: $T_j = 150^\circ\text{C}$: two parallel channels, $T_j = 25^\circ\text{C}$:	R_{ON}	--	36 67 18	40 75 20	m Ω
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2) Supply voltages higher than $V_{\text{bb(AZ)}}$ require an external current limit for the GND and status pins, e.g. with a $150\ \Omega$ resistor in the GND connection and a $15\text{ k}\Omega$ resistor in series with the status pin. A resistor for input protection is integrated.

3) R_l = internal resistance of the load dump test pulse generator

4) $V_{\text{Load dump}}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

5) Device on $50\text{mm} \times 50\text{mm} \times 1.5\text{mm}$ epoxy PCB FR4 with 6cm^2 (one layer, $70\ \mu\text{m}$ thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 14

6) Soldering point: upper side of solder edge of device pin 15. See page 14

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	
Nominal load current one channel active: two parallel channels active: Device on PCB ⁵⁾ , $T_a = 85^\circ\text{C}$, $T_j \leq 150^\circ\text{C}$	$I_{L(\text{NOM})}$	4.4 6.7	4.8 7.3	--	A
Output current while GND disconnected or pulled up; $V_{bb} = 30\text{ V}$, $V_{\text{IN}} = 0$, see diagram page 9	$I_{L(\text{GNDhigh})}$	--	--	10	mA
Turn-on time ⁷⁾ IN  to 90% V_{OUT} :	t_{on}	80	180	350	μs
Turn-off time IN  to 10% V_{OUT} : $R_L = 12\ \Omega$, $T_j = -40\dots+150^\circ\text{C}$	t_{off}	80	250	450	μs
Slew rate on ⁷⁾ 10 to 30% V_{OUT} , $R_L = 12\ \Omega$, $T_j = -40\dots+150^\circ\text{C}$:	dV/dt_{on}	0.1	--	1	$\text{V}/\mu\text{s}$
Slew rate off ⁷⁾ 70 to 40% V_{OUT} , $R_L = 12\ \Omega$, $T_j = -40\dots+150^\circ\text{C}$:	$-dV/dt_{\text{off}}$	0.1	--	1	$\text{V}/\mu\text{s}$

Operating Parameters

Operating voltage ⁸⁾ $T_j = -40\dots+150^\circ\text{C}$:	$V_{bb(\text{on})}$	5.0	--	24	V
Undervoltage shutdown $T_j = -40\dots+150^\circ\text{C}$:	$V_{bb(\text{under})}$	3.5	--	5.0	V
Undervoltage restart $T_j = -40\dots+25^\circ\text{C}$: $T_j = +150^\circ\text{C}$:	$V_{bb(\text{u rst})}$	--	--	5.0 7.0	V
Undervoltage restart of charge pump see diagram page 13 $T_j = -40\dots+150^\circ\text{C}$:	$V_{bb(\text{ucp})}$	--	5.6	7.0	V
Undervoltage hysteresis $\Delta V_{bb(\text{under})} = V_{bb(\text{u rst})} - V_{bb(\text{under})}$	$\Delta V_{bb(\text{under})}$	--	0.2	--	V
Overvoltage shutdown $T_j = -40\dots+150^\circ\text{C}$:	$V_{bb(\text{over})}$	24	--	34	V
Overvoltage restart $T_j = -40\dots+150^\circ\text{C}$:	$V_{bb(\text{o rst})}$	23	--	--	V
Overvoltage hysteresis $T_j = -40\dots+150^\circ\text{C}$:	$\Delta V_{bb(\text{over})}$	--	0.5	--	V
Overvoltage protection ⁹⁾ $T_j = -40\dots+150^\circ\text{C}$: $I_{bb} = 40\text{ mA}$	$V_{bb(\text{AZ})}$	42	47	--	V
Standby current, all channels off $T_j = 25^\circ\text{C}$: $V_{\text{IN}} = 0$ $T_j = 150^\circ\text{C}$:	$I_{bb(\text{off})}$	--	16 24	40 50	μA
Leakage output current (included in $I_{bb(\text{off})}$) $V_{\text{IN}} = 0$	$I_{L(\text{off})}$	--	--	20	μA
Operating current ¹⁰⁾ , $V_{\text{IN}} = 5\text{ V}$, $T_j = -40\dots+150^\circ\text{C}$ $I_{\text{GND}} = I_{\text{GND1}} + I_{\text{GND2}}$, one channel on: two channels on:	I_{GND}	--	1.8 3.6	4 8	mA

7) See timing diagram on page 11.

8) At supply voltage increase up to $V_{bb} = 5.6\text{ V}$ typ without charge pump, $V_{\text{OUT}} \approx V_{bb} - 2\text{ V}$

9) see also $V_{\text{ON(CL)}}$ in circuit diagram on page 8.

10) Add I_{ST} , if $I_{\text{ST}} > 0$

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	
Protection Functions					
Initial peak short circuit current limit, (see timing diagrams, page 11) each channel, $T_j = -40^\circ\text{C}$: $T_j = 25^\circ\text{C}$: $T_j = +150^\circ\text{C}$: two parallel channels	$I_{L(SCp)}$	52 42 23	65 53 31	75 63 43	A
		twice the current of one channel			
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two parallel channels (see timing diagrams, page 11)	$I_{L(SCr)}$	-- --	21 21	-- --	A
Initial short circuit shutdown time $T_{j,start} = -40^\circ\text{C}$: $T_{j,start} = 25^\circ\text{C}$: (see page 10 and timing diagrams on page 11)	$t_{off(SC)}$	-- --	3 2.5	-- --	ms
Thermal overload trip temperature	T_{jt}	150	--	--	$^\circ\text{C}$
Thermal hysteresis	ΔT_{jt}	--	10	--	K

Reverse Battery



Reverse battery voltage ¹¹⁾	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ($V_{out} > V_{bb}$) $I_L = -4.8\text{ A}$, $T_j = +150^\circ\text{C}$	$-V_{ON}$	--	600	--	mV

Diagnostic Characteristics

Open load detection current, (on-condition) each channel, $T_j = -40^\circ\text{C}$: $T_j = 25^\circ\text{C}$: $T_j = +150^\circ\text{C}$: two parallel channels	$I_{L(OL)}$	100 100 100	-- -- --	1200 1000 1000	mA
		twice the current of one channel			
Open load detection voltage ¹²⁾ $T_j = -40..+150^\circ\text{C}$:	$V_{OUT(OL)}$	2	3	4	V
Internal output pull down (OUT to GND), $V_{OUT} = 5\text{ V}$ $T_j = -40..+150^\circ\text{C}$:	R_O	4	10	30	k Ω

¹¹⁾ Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 8).

¹²⁾ External pull up resistor required for open load detection in off state.

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	
Input and Status Feedback¹³⁾					
Input resistance (see circuit page 8)	R_I	2.5	3.5	6	$\text{k}\Omega$
Input turn-on threshold voltage  $T_j = -40..+150^\circ\text{C}$:	$V_{IN(T+)}$	1.7	--	3.3	V
Input turn-off threshold voltage  $T_j = -40..+150^\circ\text{C}$:	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current $T_j = -40..+150^\circ\text{C}$: $V_{IN} = 0.4\text{ V}$:	$I_{IN(off)}$	1	--	50	μA
On state input current $T_j = -40..+150^\circ\text{C}$: $V_{IN} = 5\text{ V}$:	$I_{IN(on)}$	20	50	90	μA
Delay time for status with open load after switch off (see timing diagrams, page 12), $T_j = -40..+150^\circ\text{C}$:	$t_{d(ST\ OL4)}$	100	520	1000	μs
Status invalid after positive input slope (open load) $T_j = -40..+150^\circ\text{C}$:	$t_{d(ST)}$	--	250	600	μs
Status output (open drain)					
Zener limit voltage $T_j = -40...+150^\circ\text{C}$, $I_{ST} = +1.6\text{ mA}$:	$V_{ST(high)}$	5.4	6.1	--	V
ST low voltage $T_j = -40...+25^\circ\text{C}$, $I_{ST} = +1.6\text{ mA}$:	$V_{ST(low)}$	--	--	0.4	
$T_j = +150^\circ\text{C}$, $I_{ST} = +1.6\text{ mA}$:		--	--	0.6	

¹³⁾ If ground resistors R_{GND} are used, add the voltage drop across these resistors.

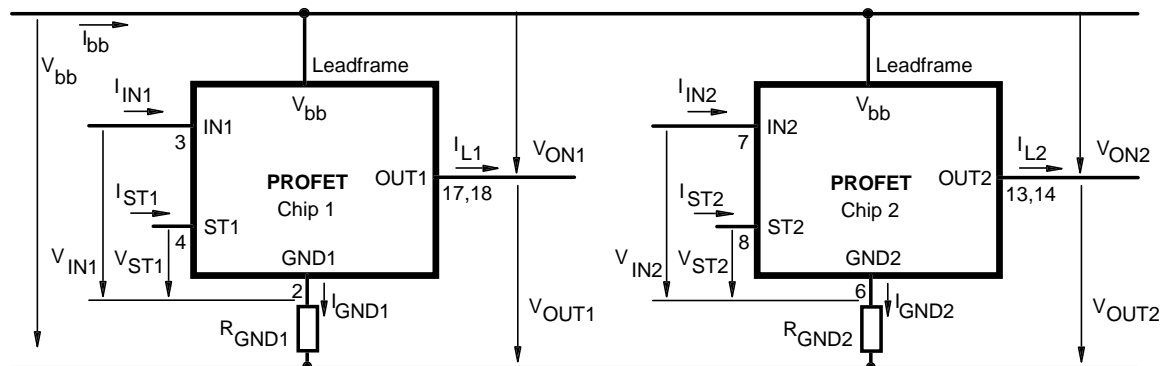
Truth Table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	BTS 733L1
Normal operation	L	L	H
	H	H	H
Open load	L	Z	H (L ¹⁴)
	H	H	L
Short circuit to V _{bb}	L	H	L ¹⁵
	H	H	H (L ¹⁶)
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	H
	H	L	H
Overvoltage	L	L	H
	H	L	H

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit
H = "High" Level Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

Terms

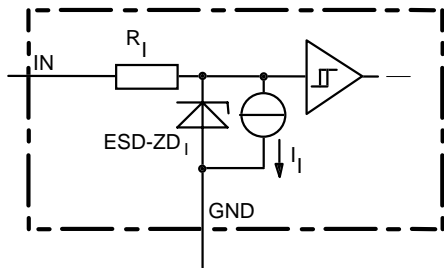


Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20

External R_{GND} optional; two resistors R_{GND1} , $R_{GND2} = 150 \Omega$ or a single resistor $R_{GND} = 75 \Omega$ for reverse battery protection up to the max. operating voltage.

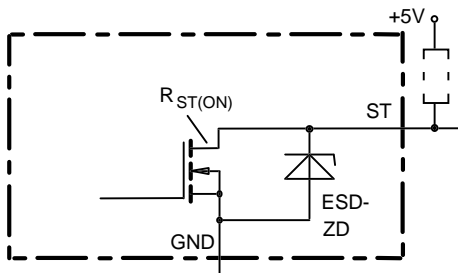
- 14) With external resistor between output and V_{bb}
- 15) An external short of output to V_{bb} in the off state causes an internal current from output to ground. If R_{GND} is used, an offset voltage at the GND and ST pins will occur and the $V_{ST\ low}$ signal may be erroneous.
- 16) Low resistance to V_{bb} may be detected by no-load-detection

Input circuit (ESD protection), IN1 or IN2



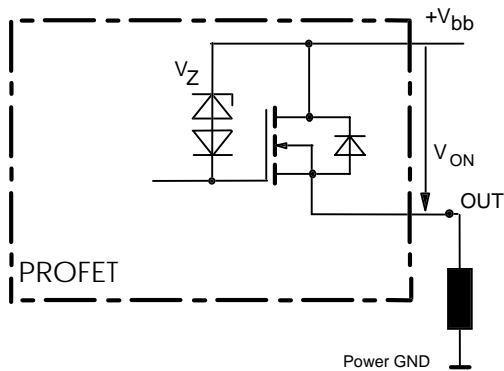
ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

Status output, ST1 or ST2



ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)} < 375 \Omega$ at 1.6 mA, ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

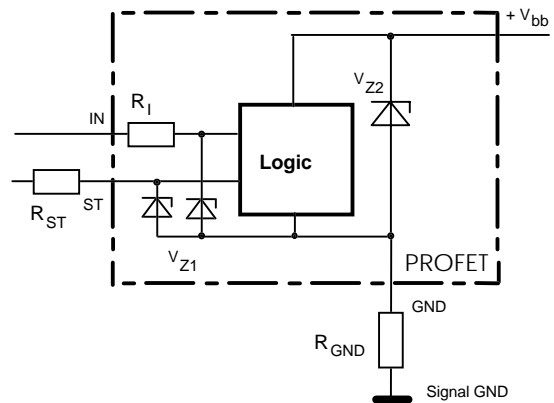
overvoltage output clamp, OUT1 or OUT2



V_{ON} clamped to $V_{ON(CL)} = 47 \text{ V typ.}$

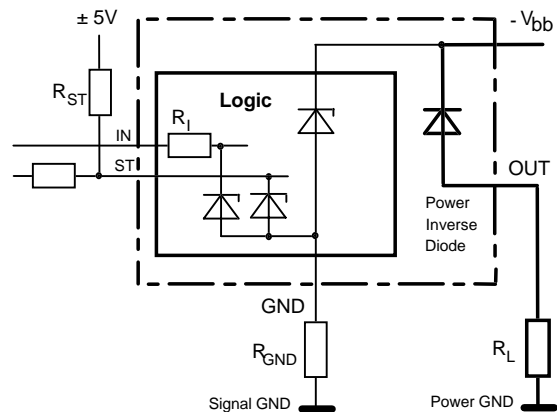
Overvoltage protection of logic part

GND1 or GND2



$V_{Z1} = 6.1 \text{ V typ.}$, $V_{Z2} = 47 \text{ V typ.}$, $R_I = 3.5 \text{ k}\Omega \text{ typ.}$, $R_{GND} = 150 \Omega$, $R_{ST} = 15 \text{ k}\Omega \text{ nominal.}$

Reverse battery protection



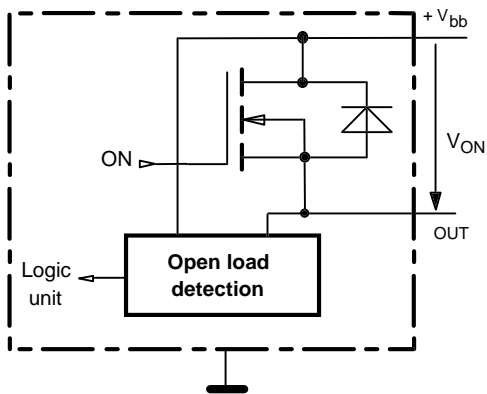
$R_{GND} = 150 \Omega$, $R_I = 3.5 \text{ k}\Omega \text{ typ.}$

Temperature protection is not active during inverse current operation.

Open-load detection, OUT1 or OUT2

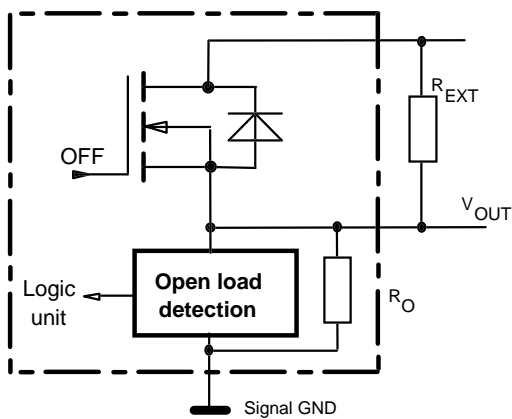
ON-state diagnostic condition:

$$V_{ON} < R_{ON} \cdot I_{L(OL)}; \text{IN high}$$

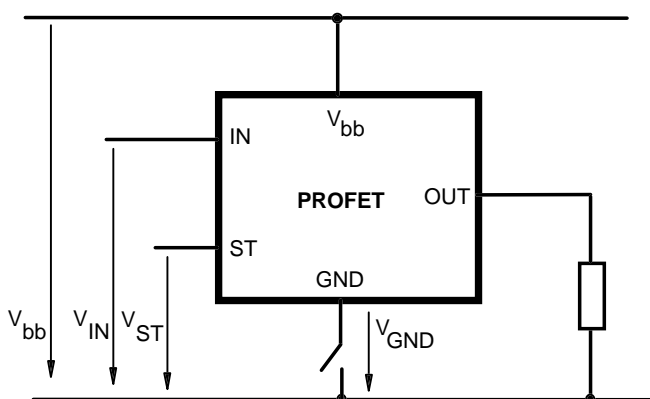


OFF-state diagnostic condition:

$$V_{OUT} > 3 \text{ V typ.}; \text{IN low}$$

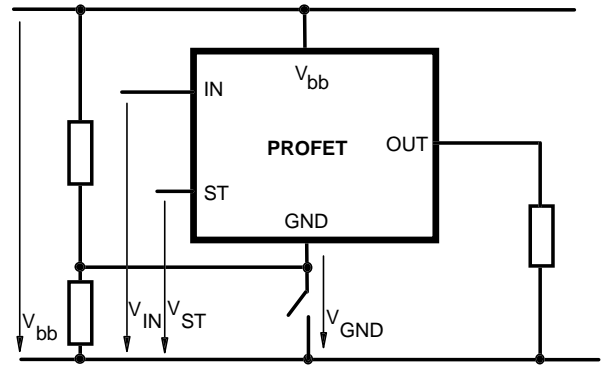


GND disconnect



In case of IN=high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$. Due to $V_{GND} > 0$, no $V_{ST} = \text{low}$ signal available.

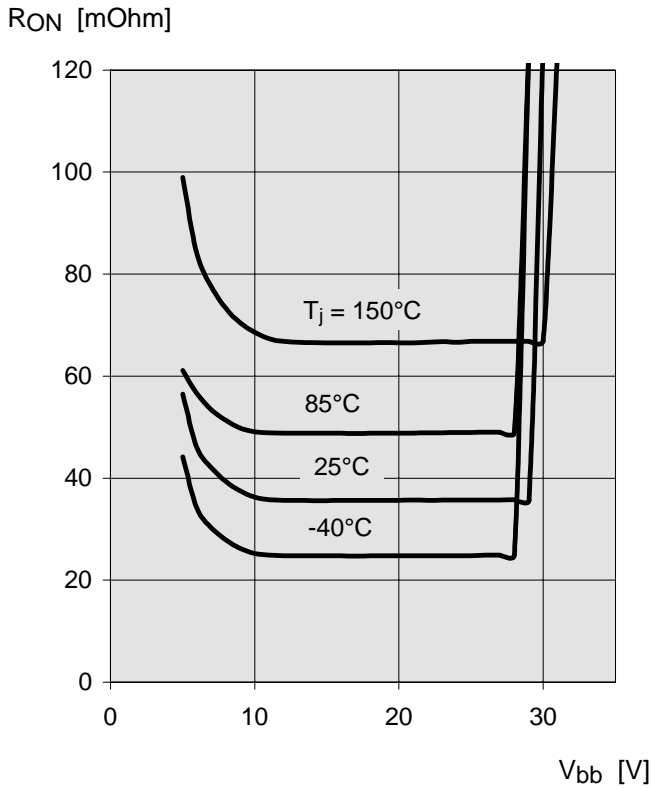
GND disconnect with GND pull up



If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off
Due to $V_{GND} > 0$, no $V_{ST} = \text{low}$ signal available.

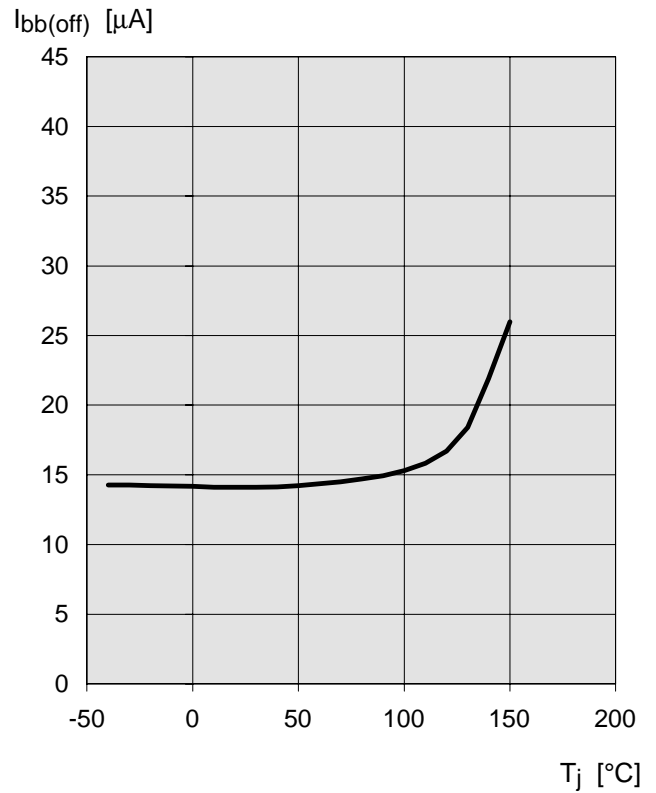
Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$; $I_L = 2\text{ A}$, $I_N = \text{high}$



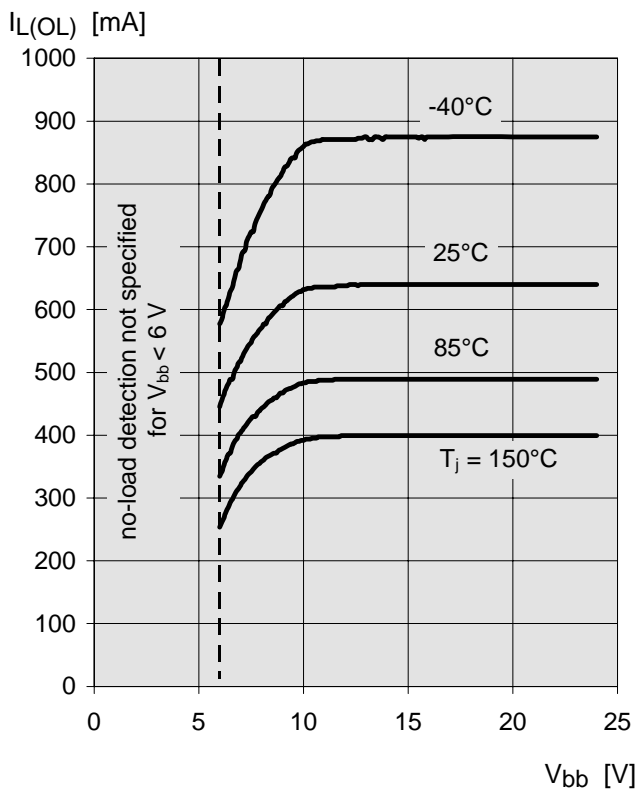
Typ. standby current

$I_{bb(off)} = f(T_j)$; $V_{bb} = 9 \dots 24\text{ V}$, $I_{N1,2} = \text{low}$



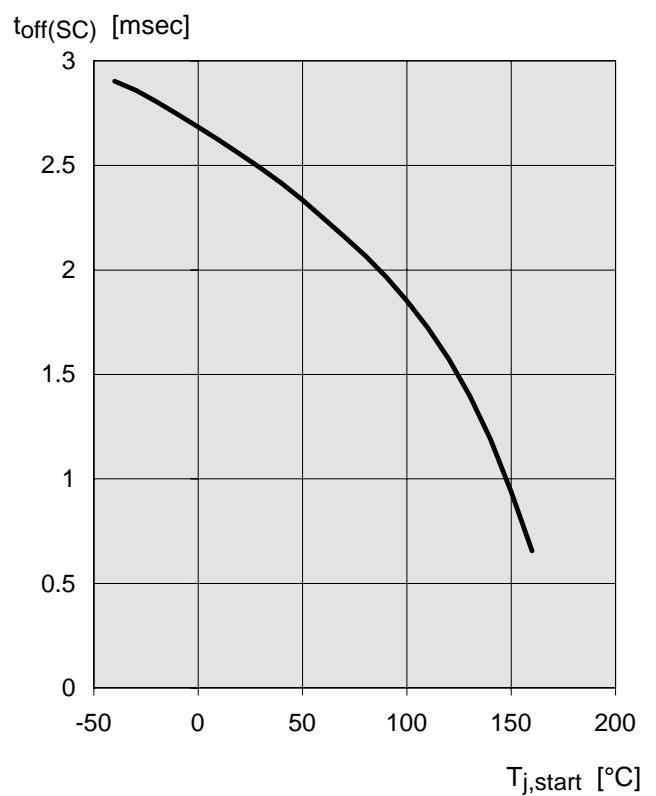
Typ. open load detection current

$I_{L(OL)} = f(V_{bb}, T_j)$; $I_N = \text{high}$



Typ. initial short circuit shutdown time

$t_{off(SC)} = f(T_{j,start})$; $V_{bb} = 12\text{ V}$



Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: V_{bb} turn on:

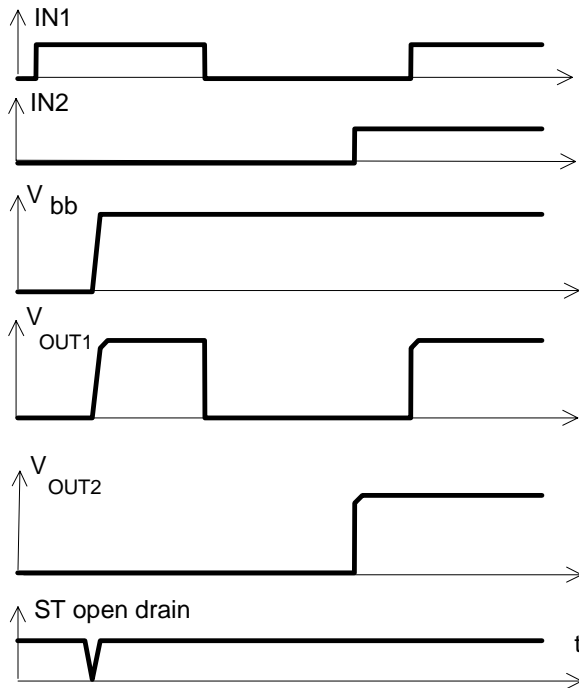
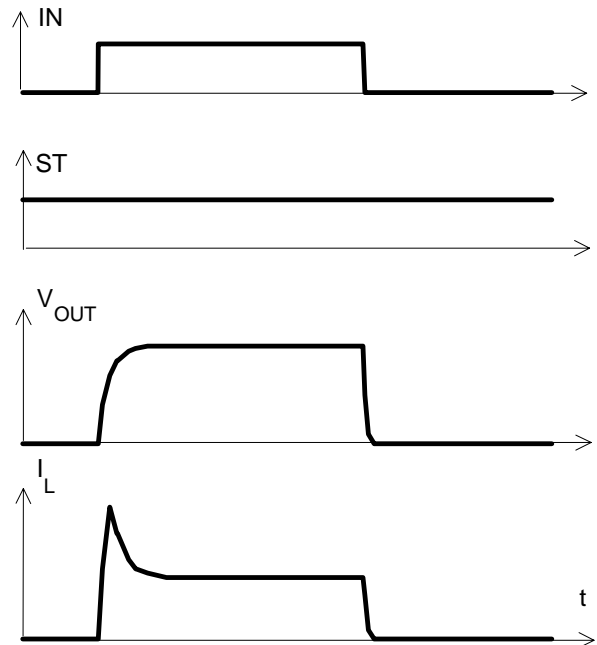


Figure 2b: Switching a lamp:



The initial peak current should be limited by the lamp and not by the initial short circuit current $I_{L(SCp)} = 53 \text{ A typ.}$ of the device.

Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

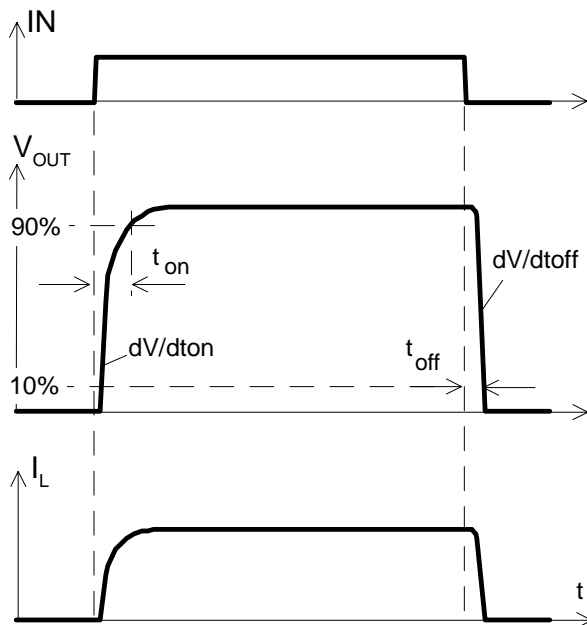
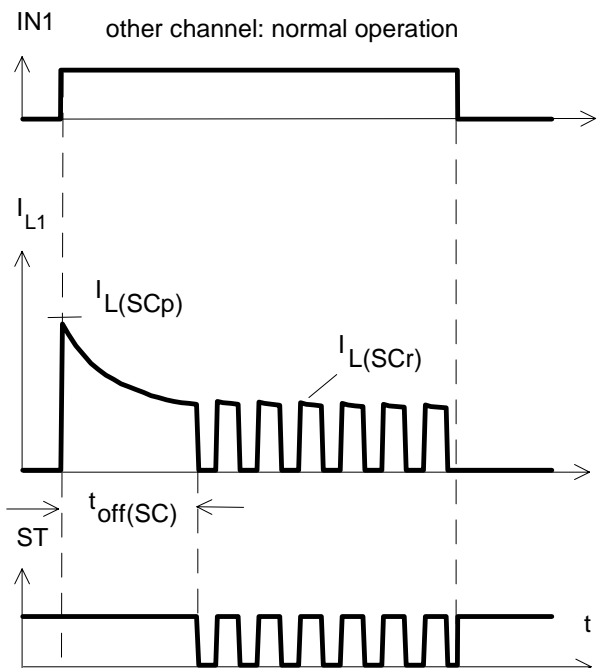


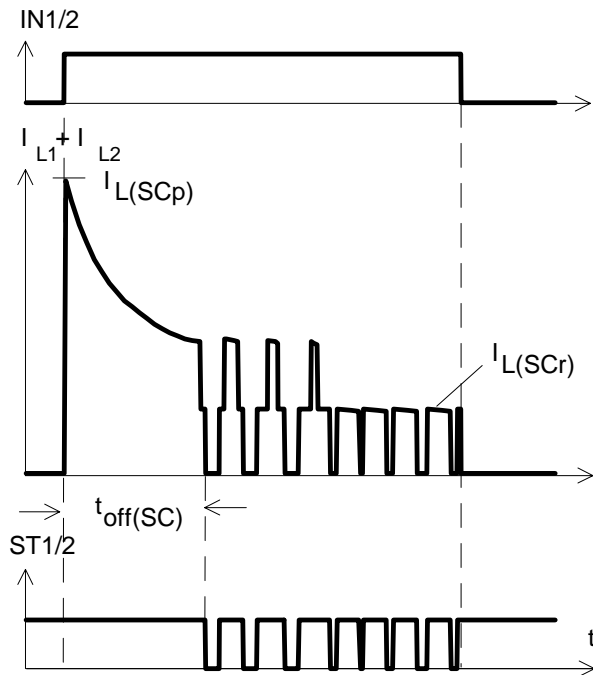
Figure 3a: Turn on into short circuit:

shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions ($t_{off(SC)}$ vs. $T_{j,start}$ see page 10)

Figure 3b: Turn on into short circuit: shut down by overtemperature, restart by cooling (two parallel switched channels 1 and 2)



ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

Figure 4a: Overtemperature: Reset if $T_j < T_{jt}$

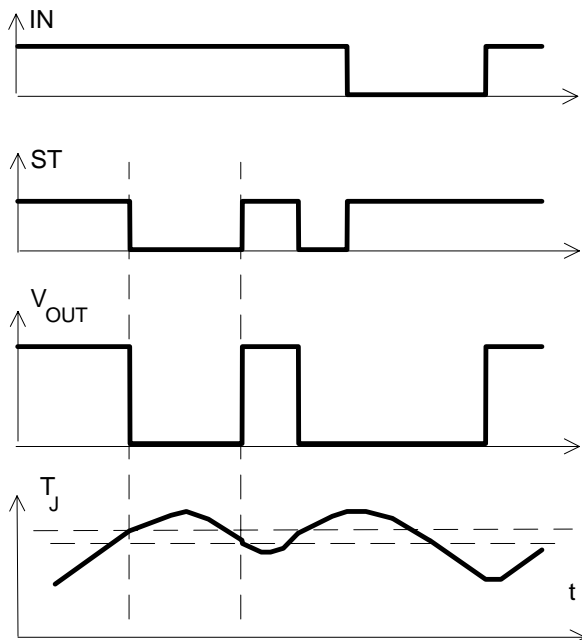
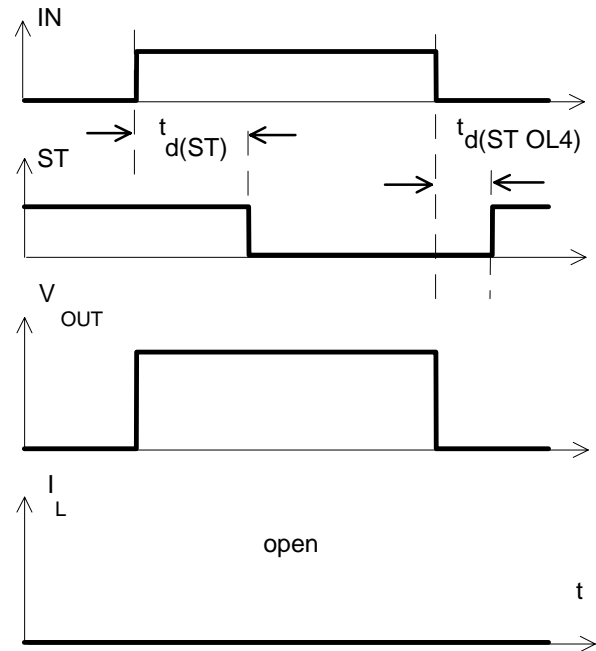
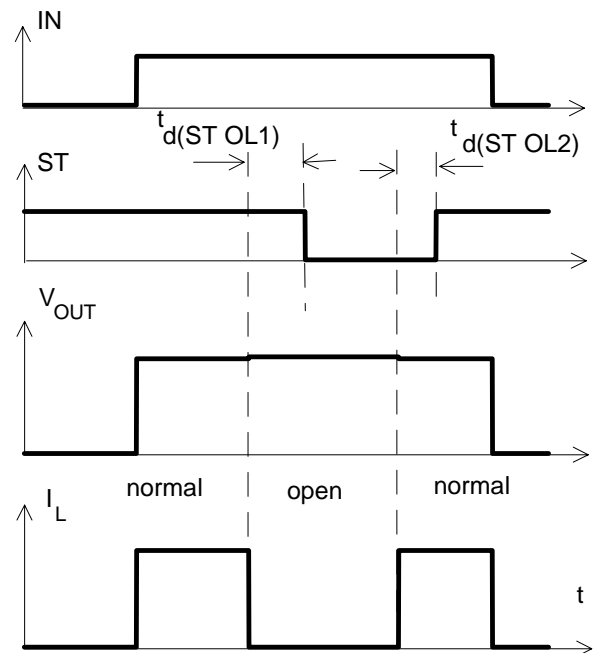


Figure 5a: Open load: detection in ON-state, turn on/off to open load



The status delay t_{d(ST OL4)} is for differentiation between the failure modes "open load in ON-state" and "overtemperature"; t_{d(ST OL4)} only appears after turn off to open load.

Figure 5b: Open load: detection in ON-state, open load occurs in on-state



t_{d(ST OL1)} = 20 μs typ., t_{d(ST OL2)} = 10 μs typ

Figure 5c: Open load: detection in ON- and OFF-state (with R_{EXT}), turn on/off to open load

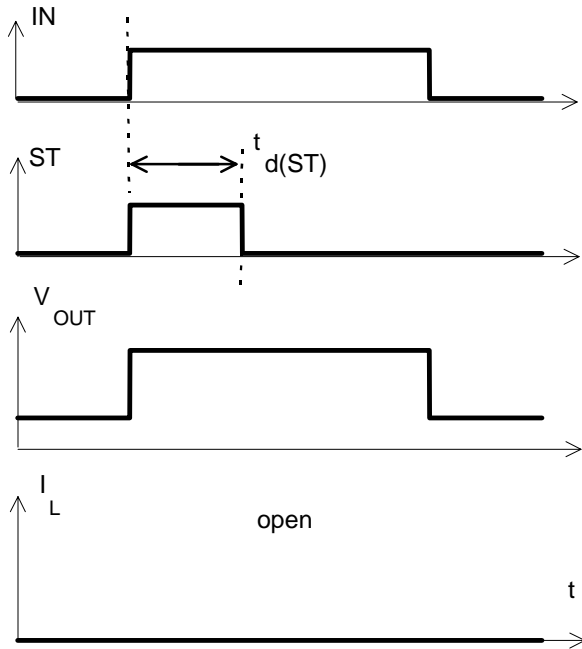


Figure 6a: Undervoltage:

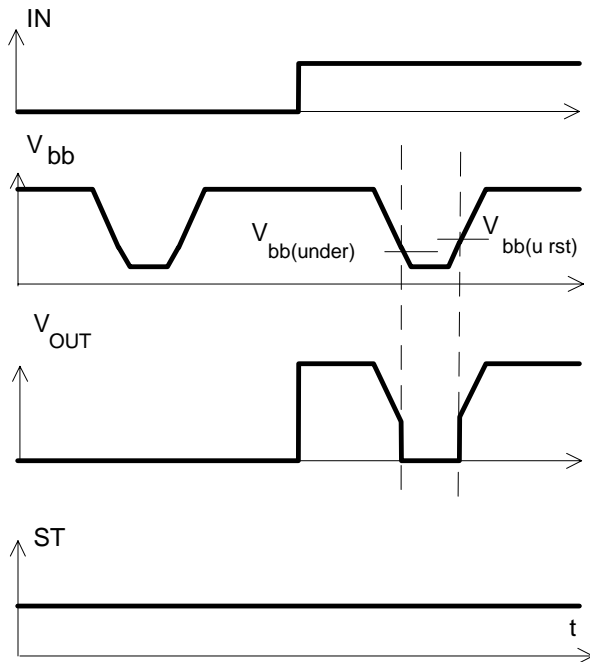
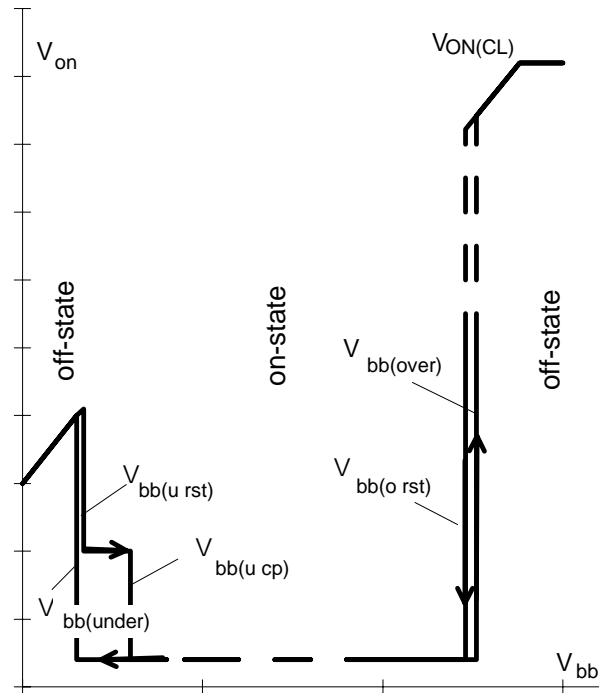
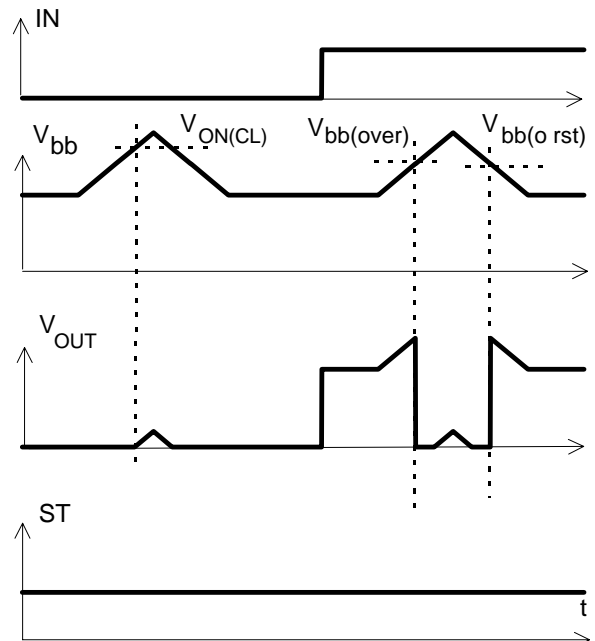


Figure 6b: Undervoltage restart of charge pump



IN = high, normal load conditions.
Charge pump starts at $V_{bb(ucp)} = 5.6V$ typ.

Figure 7a: Overvoltage:

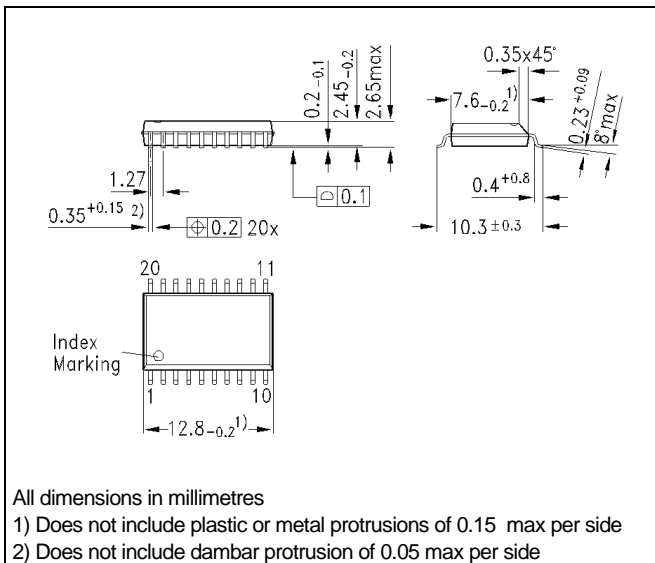


Package and Ordering Code

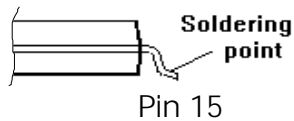
Standard P-DSO-20-9

Ordering Code

BTS733L1	Q67060-S7008-A2
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Definition of soldering point with temperature T_s :
 upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer 70 μ m, 6cm² active heatsink area) as a reference for max. power dissipation P_{tot} , nominal load current $I_{L(NOM)}$ and thermal resistance R_{thja}

