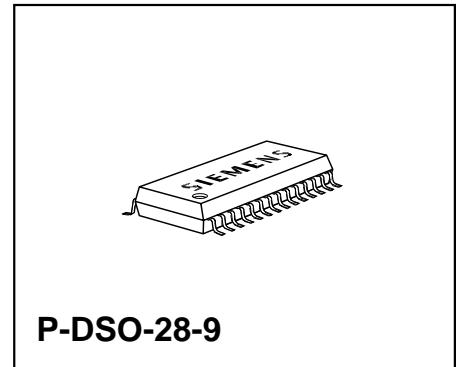


Overview

Features

- Quad switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Ultra low $R_{DS\ ON}$ @ 25 °C:
 - High-side switch: typ.85 m Ω ,
 - Low-side switch: typ. 45 m Ω
- Very high peak current capability
- Very low quiescent current
- Space- and thermal optimized power P-DSO-Package
- Full short-circuit-protection
- Operates up to 40 V
- Status flag diagnosis
- Overtemperature shut down with hysteresis
- Short-circuit detection and diagnosis
- Open-load detection and diagnosis
- C-MOS compatible inputs
- Internal clamp diodes
- Isolated sources for external current sensing
- Over- and under-voltage detection with hysteresis



| Type | Ordering Code | Package |
|-----------|---------------|------------|
| BTS 775 G | Q67007-A9350 | P-DSO-28-9 |

Description

The **BTS 775 G** is a **TrilithIC** contains one double high-side switch and two low-side switches in **one P-DSO-28-9** -Package.

**“Silicon instead of heatsink”
becomes true**

The ultra low $R_{DS\ ON}$ of this device avoids powerdissipation. It saves costs in mechanical construction and mounting and increases the efficiency.

The high-side switches are produced in the **SIEMENS SMART SIPMOS®** technology. It is fully protected and contains the signal conditioning circuitry for diagnosis. (The comparable standard high-side product is the **BTS 621L1**.)

For minimized $R_{DS\ ON}$ the two low-side switches are N channel vertical power FETs in the **SIEMENS SMART SIPMOS®** technology. Fully protected by embedded protection functions. (The comparable standard product is the **BSP 78**).

Each drain of these three chips is mounted on separated leadframes (see **P-DSO-28-9** pin configuration). The sources of all four power transistors are connected to separate pins.

So the **BTS 775 G** can be used in H-Bridge configuration as well as in any other switch configuration.

Moreover, it is possible to add current sense resistors.

All these features open a broad range of automotive and industrial applications.

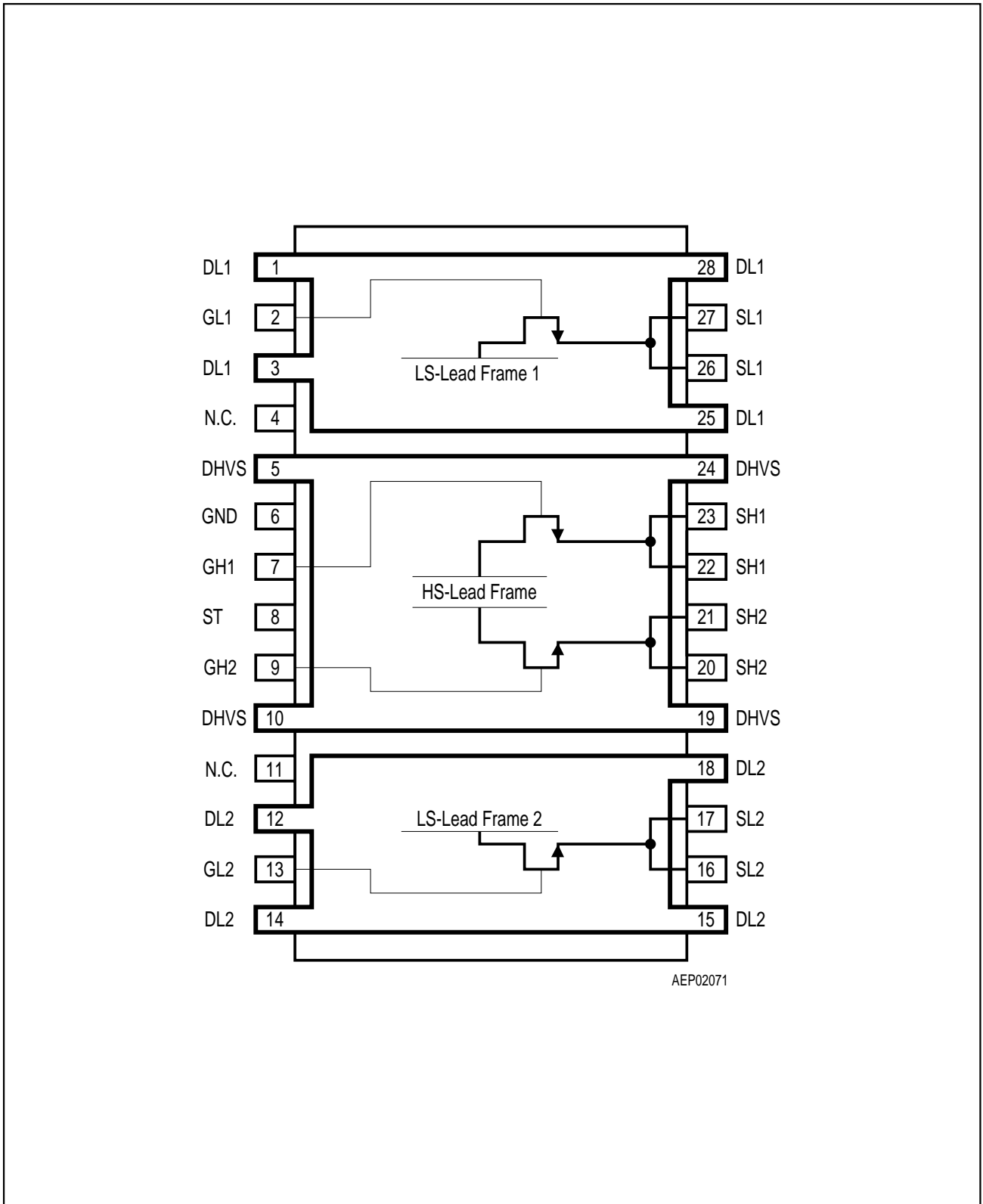


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

| Pin No. | Symbol | Function |
|-----------------------|-------------|---|
| 1, 3, 25, 28 | DL1 | Drain of low-side switch1 Leadframe 1 ¹⁾ |
| 2 | GL1 | Gate of low-side switch1 |
| 4 | N.C. | not connected |
| 5, 10, 19, 24 | DHVS | Drain of high-side switches and power supply voltage Leadframe 2 ¹⁾ |
| 6 | GND | Ground |
| 7 | GH1 | Gate of high-side switch1 |
| 8 | ST | Status of high-side switches; open Drain output |
| 9 | GH2 | Gate of high-side switch2 |
| 11 | N.C. | not connected |
| 12, 14, 15, 18 | DL2 | Drain of low-side switch2 Leadframe 3 ¹⁾ |
| 13 | GL2 | Gate of low-side switch2 |
| 16, 17 | SL2 | Source of low-side switch2 |
| 20, 21 | SH2 | Source of high-side switch2 |
| 22, 23 | SH1 | Source of high-side switch1 |
| 26, 27 | SL1 | Source of low-side switch1 |

¹⁾ To reduce the thermal resistance these pins are direct connected via metal bridges to the leadframe.

Bold type: Pin needs power wiring

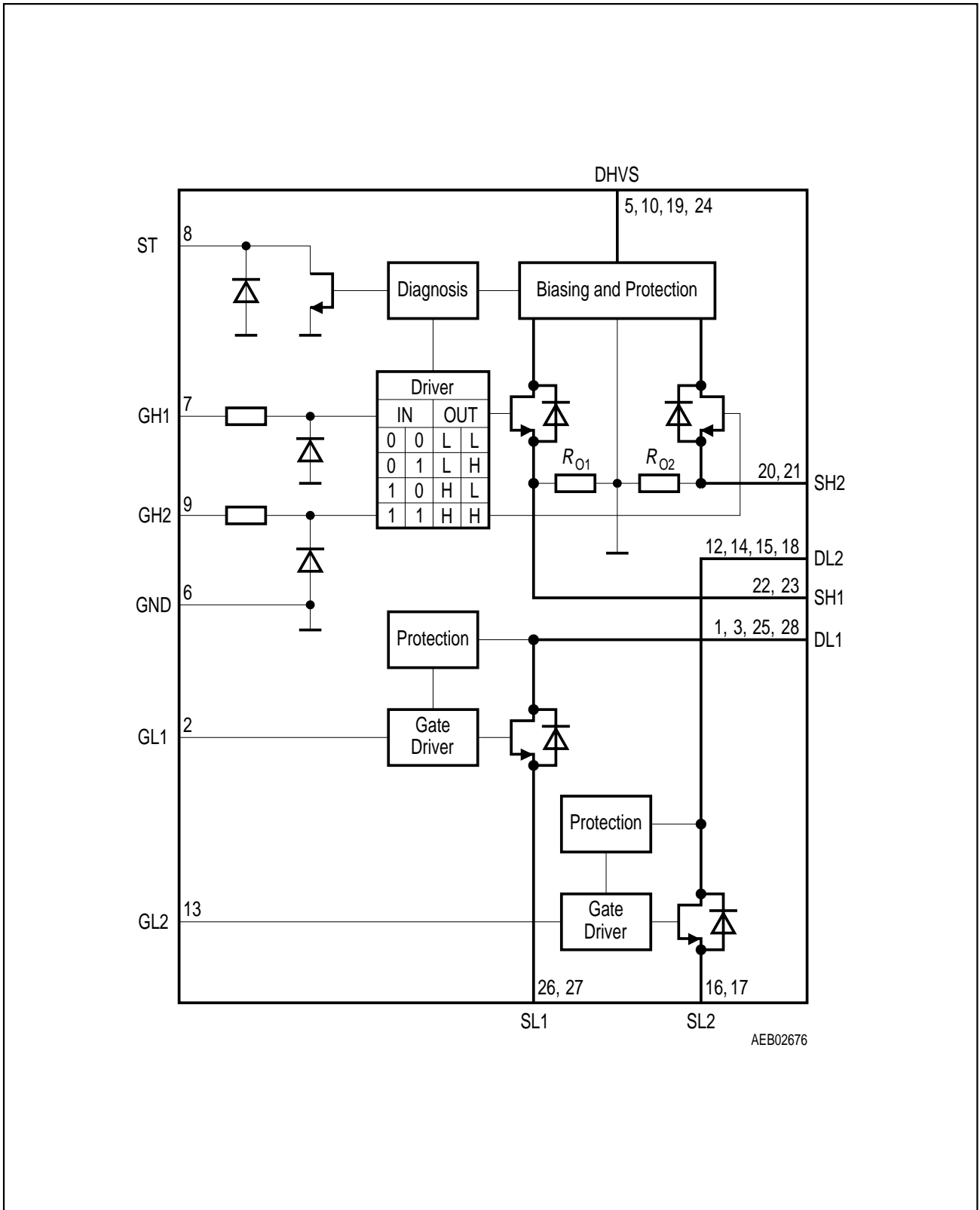


Figure 2 Block Diagram

Circuit Description

Input Circuit

The control inputs GH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages.

The inputs GL1 and GL2 are connected to the internal gate-driving units of the fully protected N-channel vertical power-MOS-FETs.

Output Stages

The output stages consist of an ultra low $R_{DS\ ON}$ Power-MOS H-Bridge. Embedded protective circuits make the outputs short circuit proof to ground, to the supply voltage and load short circuit proof. Positive and negative voltage spikes, which occur when driving inductive loads, are limited by integrated power clamp diodes.

Short Circuit Protection

The outputs are protected against

- output short circuit to ground
- output short circuit to the supply voltage, and
- overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

In the case of overloaded high-side switches the status output is set to low.

If the HS-Switches are in OFF-state-Condition internal resistors $R_{O1,2}$ from SH1,2 to GND pull the voltage at SH1,2 to low values. On each output pin SH1 and SH2 an output examiner circuit compares the output voltages with the internal reference voltage VEO. This results in switching the status output to low. The fully protected low-side switches have no status output.

Overtemperature Protection

The highside and the lowside switch also incorporates an overtemperature protection circuit with hysteresis which switches off the output transistors and sets the status output to low.

Undervoltage-Lockout (UVLO)

When V_S reaches the switch-on voltage V_{UVON} the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage V_S drops below the switch off value V_{UVOFF} .

Overvoltage-Lockout (OVLO)

When V_S reaches the switch-off voltage $V_{OV\text{OFF}}$ the High-Side output transistors are switched off with a hysteresis. The IC becomes active if the supply voltage V_S drops below the switch-on value $V_{OV\text{ON}}$.

Open Load Detection

Open load is detected by current measurement. If the output current drops below an internal fixed level the error flag is set with a delay.

Status Flag

Various errors as listed in the table "Diagnosis" are detected by switching the open drain output ST to low.

Truthtable and Diagnosis (valid only for the High-Side-Switches)

| Flag | GH1 | GH2 | SH1 | SH2 | ST | Remarks | |
|--|--------|-----|---------|-----|----|--|----------|
| | Inputs | | Outputs | | | | |
| Normal operation; identical with functional truth table | 0 | 0 | L | L | 1 | stand-by mode switch2 active switch1 active both switches active | |
| | 0 | 1 | L | H | 1 | | |
| | 1 | 0 | H | L | 1 | | |
| | 1 | 1 | H | H | 1 | | |
| Open load at high-side switch1 | 0 | 0 | Z | L | 1 | | |
| | 0 | 1 | Z | H | 1 | | |
| | 1 | X | H | X | 0 | | detected |
| Open load at high-side switch2 | 0 | 0 | L | Z | 1 | | |
| | 1 | 0 | H | Z | 1 | | |
| | X | 1 | X | H | 0 | | detected |
| Short circuit to DHVS at high-side switch1 | 0 | 0 | H | L | 0 | detected | |
| | 0 | 1 | H | H | 1 | | |
| | 1 | X | H | X | 1 | | |
| Short circuit to DHVS at high-side switch2 | 0 | 0 | L | H | 0 | detected | |
| | 1 | 0 | H | H | 1 | | |
| | X | 1 | X | H | 1 | | |
| Overtemperature high-side switch1 | 0 | X | L | X | 1 | | |
| | 1 | X | L | X | 0 | | detected |
| Overtemperature high-side switch2 | X | 0 | X | L | 1 | | |
| | X | 1 | X | L | 0 | | detected |
| Overtemperature both high-side switch | 0 | 0 | L | L | 1 | | |
| | X | 1 | L | L | 0 | | detected |
| | 1 | X | L | L | 0 | | detected |
| Over- and Under-Voltage | X | X | L | L | 1 | not detected | |

Inputs:

0 = Logic LOW
 1 = Logic HIGH
 X = don't care

Outputs:

Z = Output in tristate condition
 L = Output in sink condition
 H = Output in source condition
 X = Voltage level undefined

Status:

1 = No error
 0 = Error

Electrical Characteristics

Absolute Maximum Ratings

$-40\text{ °C} < T_j < 150\text{ °C}$

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|-----------|--------|--------------|------|------|---------|
| | | min. | max. | | |

High-Side-Switches (Pins DHVS, GH1,2 and SH1,2)

| | | | | | |
|------------------|-----------|-------|----|----|----------------------|
| Supply voltage | V_S | - 0.3 | 43 | V | – |
| HS-drain current | I_{DHS} | - 10 | * | A | * internally limited |
| HS-input current | I_{GH} | - 2 | 2 | mA | Pin GH1 and GH2 |
| HS-input voltage | V_{GH} | - 10 | 16 | V | Pin GH1 and GH2 |

Status Output ST

| | | | | | |
|-----------------------|----------|-----|---|----|--------|
| Status Output current | I_{ST} | - 5 | 5 | mA | Pin ST |
|-----------------------|----------|-----|---|----|--------|

Low-Side-Switches (Pins DL1,2, GL1,2 and SL1,2)

| | | | | | |
|--------------------|---------------|-------|----|---|---|
| Break-down voltage | $V_{(BR)DSS}$ | 40 | – | V | $V_{GS} = 0\text{ V}; I_D \leq 1\text{ mA}$ |
| LS-drain current | I_{DLS} | 16 | * | A | * internally limited |
| LS-input voltage | V_{GL} | - 0.3 | 10 | V | Pin GL1 and GL2 |

Temperatures

| | | | | | |
|----------------------|-----------|------|-----|----|---|
| Junction temperature | T_j | - 40 | 150 | °C | – |
| Storage temperature | T_{stg} | - 50 | 150 | °C | – |

Thermal Resistances (one HS-LS-Path active)

| | | | | | |
|------------------|--------------|---|----|-----|------------------------|
| LS-junction case | R_{thjCLS} | – | 20 | K/W | measured to pin3 or 12 |
| HS-junction case | R_{thjCHS} | – | 20 | K/W | measured to pin19 |
| Junction ambient | R_{thja} | – | 60 | K/W | – |

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|-------------------------|-----------|--------------|------|------|-------------------------------------|
| | | min. | max. | | |
| Supply voltage | V_S | V_{UVOFF} | 36 | V | After V_S rising above V_{UVON} |
| Input voltages | V_{GH} | - 0.3 | 15 | V | - |
| Input voltages | V_{GL} | - 0.3 | 10 | V | - |
| Output current | I_{ST} | 0 | 2 | mA | - |
| HS-junction temperature | T_{jHS} | - 40 | 150 | °C | - |
| LS-junction temperature | T_{jLS} | - 40 | 150 | °C | - |

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ °C} < T_j < 150 \text{ °C}$; $8 \text{ V} > V_S > 18 \text{ V}$
 unless otherwise specified

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Current Consumption

| | | | | | | |
|-------------------|-------|---|----|-----|---------------|--|
| Quiescent current | I_S | – | 16 | 30 | μA | GH1 = GH2 = L $V_S = 13.2 \text{ V}$ $T_j = 25 \text{ °C}$ |
| Quiescent current | I_S | – | – | 35 | μA | GH1 = GH2 = L $V_S = 13.2 \text{ V}$ |
| Supply current | I_S | – | 2 | 3.5 | mA | GH1 or GH2 = H |
| Supply current | I_S | – | 4 | 7 | mA | GH1 and GH2 = H |

Under Voltage Lockout (UVLO)

| | | | | | | |
|--------------------------|-------------|-----|-----|---|---|------------------------|
| Switch-ON voltage | V_{UVON} | – | 5.4 | 7 | V | V_S increasing |
| Switch-OFF voltage | V_{UVOFF} | 3.5 | 4.2 | – | V | V_S decreasing |
| Switch ON/OFF hysteresis | V_{UVHY} | – | 1.2 | – | V | $V_{UVON} - V_{UVOFF}$ |

Over Voltage Lockout (OVLO)

| | | | | | | |
|--------------------------|-------------|----|------|----|---|------------------------|
| Switch-OFF voltage | V_{OVOFF} | 36 | 37.8 | 43 | V | V_S increasing |
| Switch-ON voltage | V_{OVON} | 35 | 37.1 | – | V | V_S decreasing |
| Switch OFF/ON hysteresis | V_{OVHY} | – | 0.7 | – | V | $V_{OVOFF} - V_{OVON}$ |

Short Circuit of Highside Switch to GND

| | | | | | | |
|-------------------------|-----------|----|----|----|---|------------------------|
| Initial peak SC current | I_{SCP} | 11 | 18 | 25 | A | $T_j = -40 \text{ °C}$ |
| Initial peak SC current | I_{SCP} | 9 | 14 | 22 | A | $T_j = 25 \text{ °C}$ |
| Initial peak SC current | I_{SCP} | 5 | 8 | 14 | A | $T_j = 150 \text{ °C}$ |

Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} > V_S > 18 \text{ V}$
 unless otherwise specified

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Short Circuit of Highside Switch to V_S

| | | | | | | |
|-------------------------------|----------|---|----|----|------------|------------------------|
| OFF-state examiner-voltage | V_{EO} | 2 | 3 | 4 | V | $V_{GH} = 0 \text{ V}$ |
| Output pull-down-resistor | R_O | 4 | 10 | 30 | k Ω | – |

Open Circuit Detection of Highside Switch

| | | | | | | |
|-------------------|-----------|----|-----|-----|----|---|
| Detection current | I_{OCD} | 10 | 130 | 400 | mA | – |
|-------------------|-----------|----|-----|-----|----|---|

Switching Times of Highside Switch

| | | | | | | |
|-------------------------------------|-----------|---|-----|-----|----|---|
| Switch-ON-time; to 90% V_{SH} | t_{ON} | – | 0.2 | 0.4 | ms | resistive load $I_{SH} = 1 \text{ A}$; $V_S = 12 \text{ V}$ |
| Switch-OFF-time; to 10% V_{SH} | t_{OFF} | – | 0.2 | 0.4 | ms | resistive load $I_{SH} = 1 \text{ A}$; $V_S = 12 \text{ V}$ |

Note: switching times are guaranteed by design

Control Inputs of Highside Switches GH 1, 2

| | | | | | | |
|--------------------------|------------|-----|-----|-----|---------------|---------------------------|
| H-input voltage | V_{GHH} | – | 2.8 | 3.5 | V | – |
| L-input voltage | V_{GHL} | 1.5 | 2.3 | – | V | – |
| Input voltage hysteresis | V_{GHHY} | – | 0.5 | – | V | – |
| H-input current | I_{GHH} | 20 | 60 | 90 | μA | $V_{GH} = 5 \text{ V}$ |
| L-input current | I_{GHL} | 1 | 25 | 50 | μA | $V_{GH} = 0.4 \text{ V}$ |
| Input series resistance | R_i | 2.5 | 3.5 | 6 | k Ω | – |
| Zener limit voltage | V_{GHZ} | 5.4 | – | – | V | $I_{GH} = 1.6 \text{ mA}$ |

Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} > V_S > 18 \text{ V}$
 unless otherwise specified

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Control Inputs GL1, 2

| | | | | | | |
|------------------------|--------------|-----|-----|-----|---------------|--|
| Gate-threshold-voltage | $V_{GL(th)}$ | 0.9 | 1.7 | 2.2 | V | $I_{DL} = 2 \text{ mA}$ |
| Input current | I_{GLN} | – | 10 | 30 | μA | $V_{GL} = 5 \text{ V}$; normal operation |
| Input current | I_{GLF} | – | 150 | 300 | μA | $V_{GL} = 5 \text{ V}$; failure mode |

Short Circuit of Lowside Switch to V_S

| | | | | | | |
|-------------------------|-----------|----|----|----|---|------------------------------------|
| Initial peak SC current | I_{SCP} | 18 | 26 | 34 | A | $T_j = -40 \text{ }^\circ\text{C}$ |
| | | 15 | 21 | 27 | A | $T_j = 25 \text{ }^\circ\text{C}$ |
| | | 10 | 14 | 18 | A | $T_j = 150 \text{ }^\circ\text{C}$ |

Switching Times of Lowside Switch

| | | | | | | |
|-------------------------------------|-----------|---|-----|-----|---------------|---|
| Switch-ON-time; to 90% V_{SL} | t_{ON} | – | 100 | 200 | μs | resistive load $I_{SH} = 1 \text{ A}$; $V_S = 12 \text{ V}$ |
| Switch-OFF-time; to 10% V_{SL} | t_{OFF} | – | 50 | 200 | μs | resistive load $I_{SH} = 1 \text{ A}$; $V_S = 12 \text{ V}$ |

Note: Switching times are guaranteed by design.

Status Flag Output ST of Highside Switch

| | | | | | | |
|---------------------|------------|-----|------|-----|---------------|---------------------------|
| Low output voltage | V_{STL} | – | 0.25 | 0.6 | V | $I_{ST} = 1.6 \text{ mA}$ |
| Leakage current | I_{STLK} | – | 0.5 | 10 | μA | $V_{ST} = 5 \text{ V}$ |
| Zener-limit-voltage | V_{STZ} | 5.4 | – | – | V | $I_{ST} = 1.6 \text{ mA}$ |

Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C}$; $8 \text{ V} > V_s > 18 \text{ V}$
 unless otherwise specified

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|--------------|------|------|------|----------------|
| | | min. | typ. | max. | | |

Thermal Shutdown

| | | | | | | |
|--|------------|-----|----|-----|------------------|--------------------------------|
| Thermal shutdown junction temperature | T_{jSD} | 155 | – | 190 | $^\circ\text{C}$ | – |
| Thermal switch-on junction temperature | T_{jSO} | 150 | – | 180 | $^\circ\text{C}$ | – |
| Temperature hysteresis | ΔT | – | 10 | – | $^\circ\text{C}$ | $\Delta T = T_{jSD} - T_{jSO}$ |

Output Stages

| | | | | | | |
|--|-----------------|---|-----|-----|------------------|---|
| Leakage current of highside switch | I_{HLK} | – | 5 | 12 | μA | $V_{GH} = V_{SH} = 0 \text{ V}$ |
| Leakage current of lowside switch | I_{LKL} | – | 1.3 | 10 | μA | $V_{GL} = 0 \text{ V}$ $V_{DS} = 13 \text{ V}$ |
| Clamp-diode of highside switch; forward-voltage | V_{FH} | – | 0.8 | 1.5 | V | $I_{FH} = 3 \text{ A}$ |
| Clamp-diode leakage-current of highside switch | I_{LKCL} | – | 2 | 10 | mA | $I_{FH} = 3 \text{ A}$ |
| Clamp-diode of lowside switch; forward-voltage | V_{FL} | – | 0.8 | 1.2 | V | $I_{FL} = 3 \text{ A}$ |
| Static drain-source on-resistance of highside switch | $R_{DS\ ON\ H}$ | – | 85 | 110 | $\text{m}\Omega$ | $I_{SH} = 1 \text{ A}$ $T_j = 25 \text{ }^\circ\text{C}$ |
| Static drain-source on-resistance of lowside switch | $R_{DS\ ON\ L}$ | – | 45 | 60 | $\text{m}\Omega$ | $I_{SL} = 1 \text{ A}$; $V_{GL} = 5 \text{ V}$ $T_j = 25 \text{ }^\circ\text{C}$ |
| Static path on-resistance | $R_{DS\ ON}$ | – | – | 320 | $\text{m}\Omega$ | $R_{DS\ ON\ H} + R_{DS\ ON\ L}$ $I_{SH} = 1 \text{ A}$; |

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25^\circ\text{C}$ and the given supply voltage.

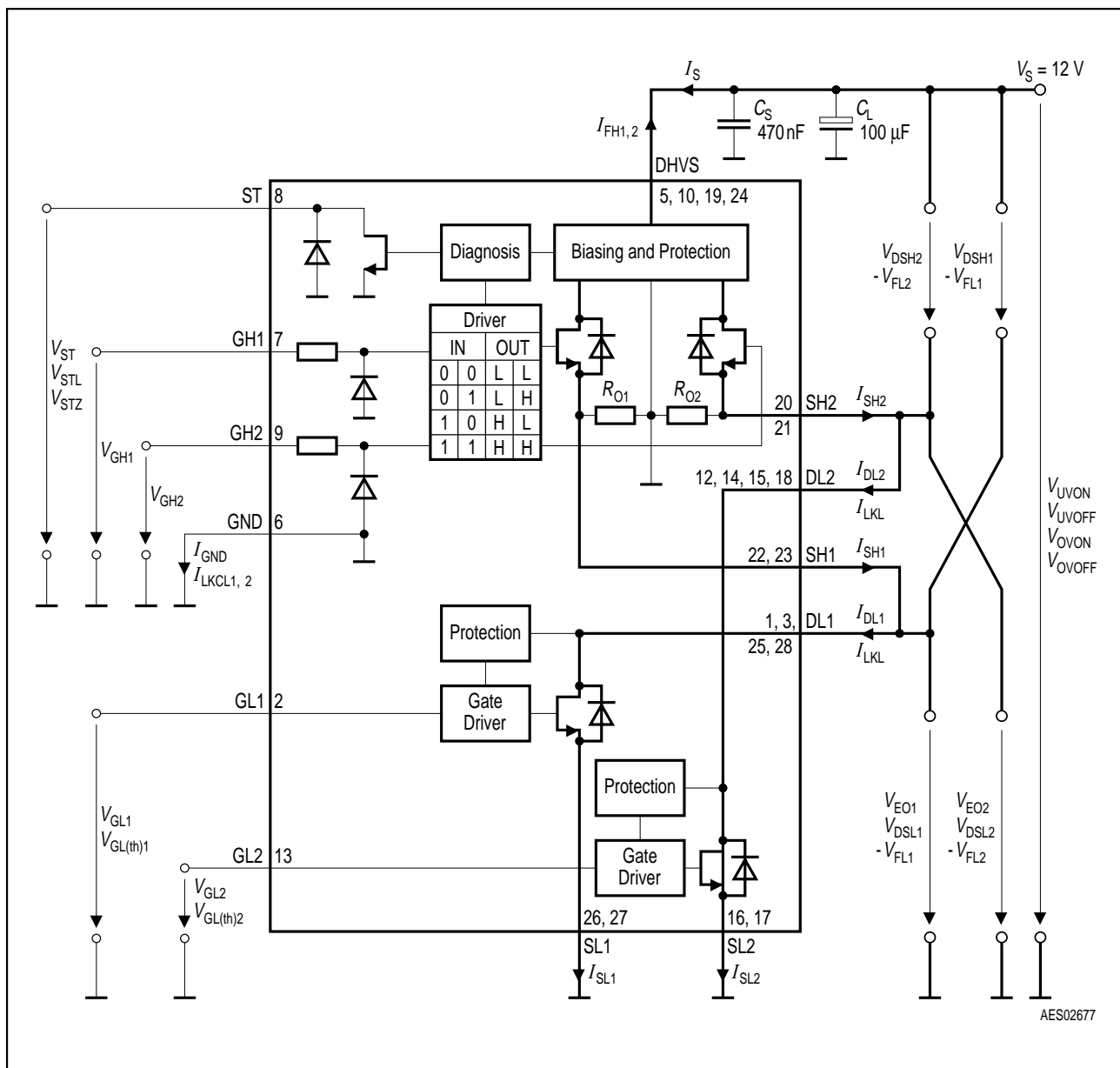
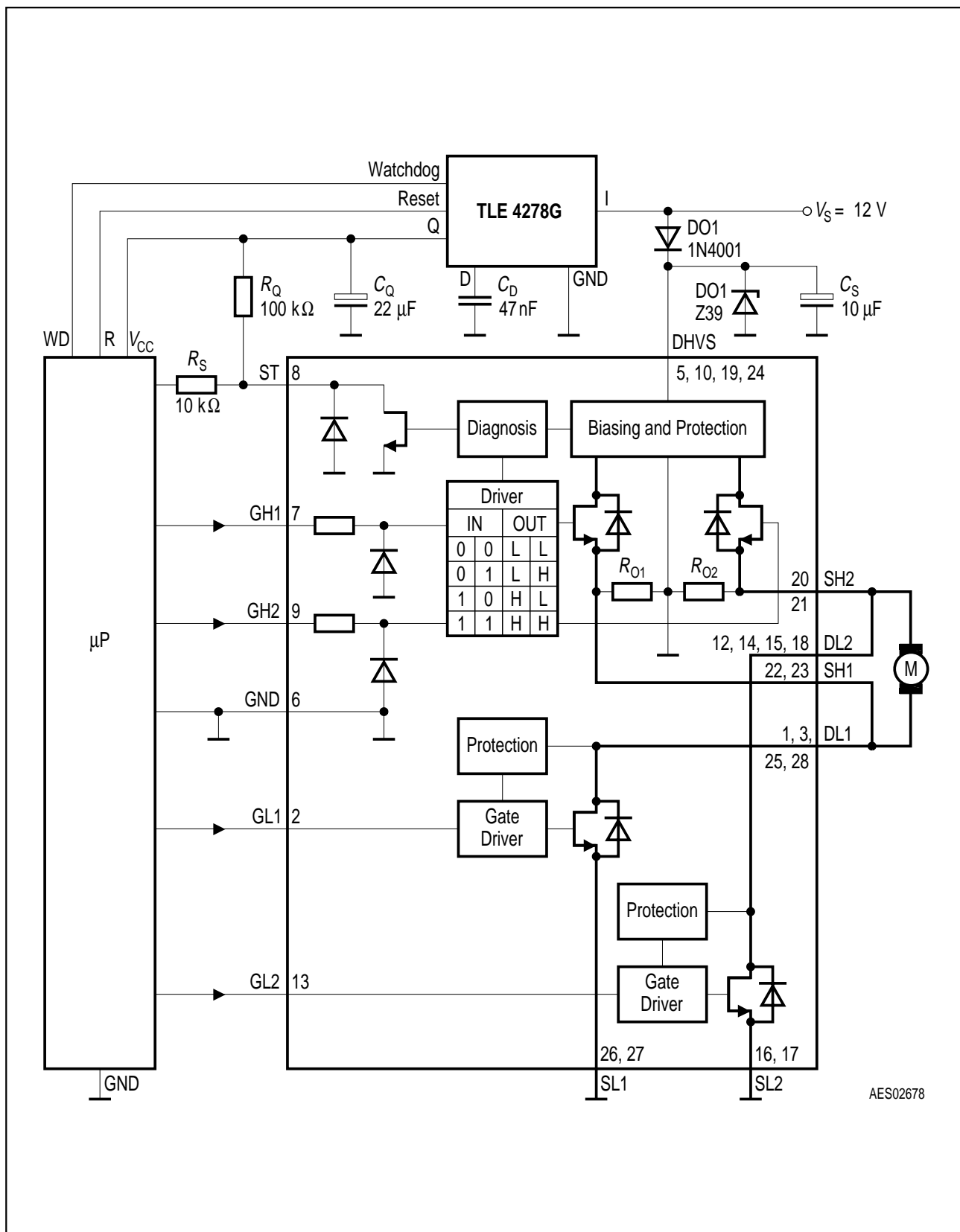


Figure 3 Test Circuit

| HS-Source-Current | Named during Short Circuit | Named during Open Circuit | Named during Leakage-Cond. |
|-------------------|----------------------------|---------------------------|----------------------------|
| $I_{SH1,2}$ | I_{SCP} | I_{OCD} | I_{HSLK} |

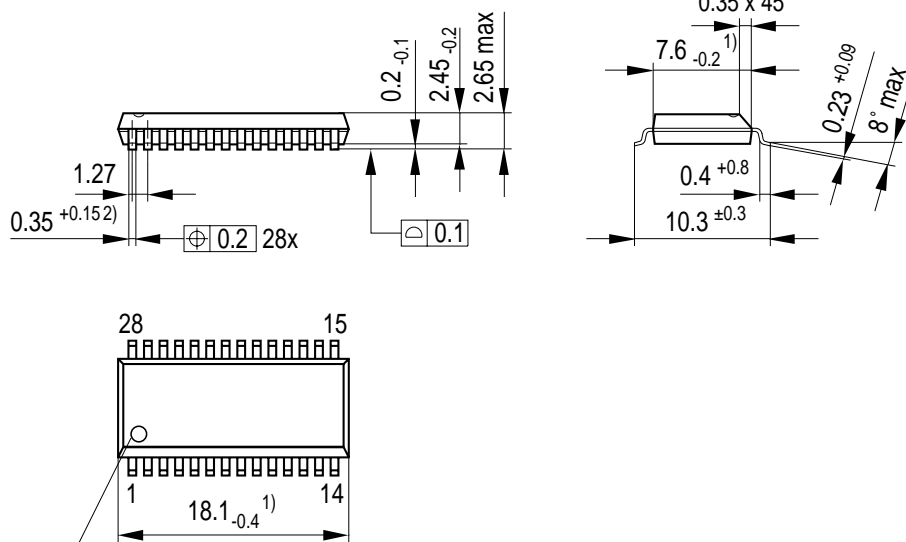


AES02678

Figure 4 Application Circuit

Package Outlines

P-DSO-28-9
(Plastic Dual Small Outline Package)



Index Marking

- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

GPS05123

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm