# THYRISTORS

Silicon thyristors in metal envelopes, intended for general purpose single-phase or three-phase mains operation.
The series consists of reverse polarity types (anode to stud) identified by a suffix R:
BTW24-600R to 1600R.

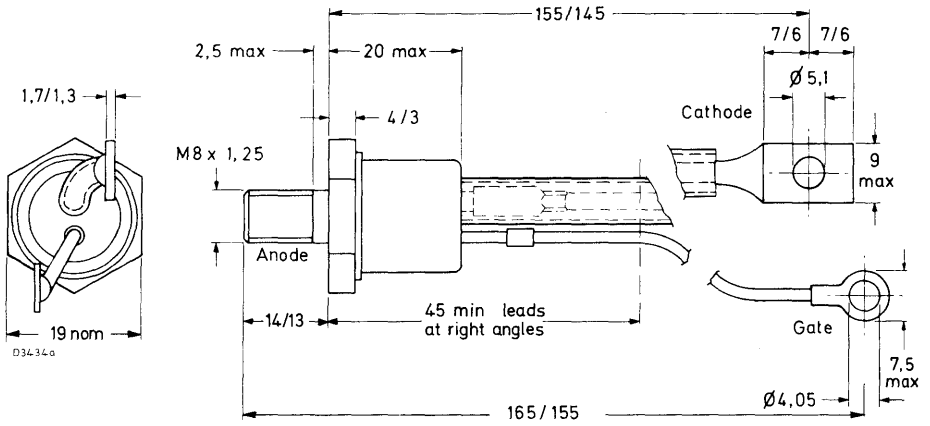
## QUICK REFERENCE DATA

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Repetitive peak voltages | BTW24- | 600R | 800R | 1000R | 1200R | 1400R | 1600R | |
| $V_{DRM} = V_{RRM}$ | max. | 600 | 800 | 1000 | 1200 | 1400 | 1600 | V |
| Average on-state current | | | | | $I_{T(AV)}$ | max. | 35 | A |
| R.M.S. on-state current | | | | | $I_{T(RMS)}$ | max. | 55 | A |
| Non-repetitive peak on-state current | | | | | $I_{TSM}$ | max. | 800 | A |
| Rate of rise of off-state voltage that will not trigger any device | | | | | $dV_D/dt$ | < | 200 | V/μs |
| On request (see ordering note on page 4) | | | | | $dV_D/dt$ | < | 1000 | V/μs |

## MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-103.




Net mass: 46 g
Diameter of clearance hole: 8,5 mm
Torque on nut: min. 4 Nm (40 kg cm)
max. 6 Nm (60 kg cm)

Supplied with device: 1 nut, 1 lock washer
Nut dimensions across the flats: 13 mm

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

### Anode to cathode

| | | | BTW24-600R | 800R | 1000R | 1200R | 1400R | 1600R | |
|---|---|---|---|---|---|---|---|---|---|
| Non-repetitive peak voltages ($t \leqslant 10$ ms) | $V_{DSM}/V_{RSM}$ | max. | 600 | 800 | 1000 | 1200 | 1400 | 1600 | V |
| Repetitive peak voltages | $V_{DRM}/V_{RRM}$ | max. | 600 | 800 | 1000 | 1200 | 1400 | 1600 | V |
| Crest working voltages | $V_{DWM}/V_{RWM}$ | max. | 400 | 600 | 700 | 800 | 800 | 800 | V * |

| | | | | |
|---|---|---|---|---|
| Average on-state current (averaged over any 20 ms period) up to $T_{mb} = 85$ °C | $I_{T(AV)}$ | max. | 35 | A |
| R.M.S. on-state current | $I_{T(RMS)}$ | max. | 55 | A |
| Repetitive peak on-state current | $I_{TRM}$ | max. | 450 | A |
| Non-repetitive peak on-state current; t = 10 ms; half sine-wave; $T_j = 125$ °C prior to surge; with reapplied $V_{RWMmax}$ | $I_{TSM}$ | max. | 800 | A |
| $I^2t$ for fusing (t = 10 ms) | $I^2t$ | max. | 3200 | $A^2s$ |
| Rate of rise of on-state current after triggering with $I_G = 500$ mA to $I_T = 100$ A; $dI_G/dt = 1$ A/µs | $dI_T/dt$ | max. | 300 | A/µs |
| Rate of change of commutation current | see Fig. 14 | | | |

### Gate to cathode

| | | | | |
|---|---|---|---|---|
| Reverse peak voltage | $V_{RGM}$ | max. | 10 | V |
| Average power dissipation (averaged over any 20 ms period) | $P_{G(AV)}$ | max. | 1 | W |
| Peak power dissipation | $P_{GM}$ | max. | 5 | W |

### Temperatures

| | | | | |
|---|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −55 to + 125 | °C |
| Junction temperature | $T_j$ | max. | 125 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | = | 0,6 | °C/W |
| From mounting base to heatsink | $R_{th\ mb\text{-}h}$ | = | 0,2 | °C/W |
| Transient thermal impedance (t = 1 ms) | $Z_{th\ j\text{-}mb}$ | = | 0,04 | °C/W |

* To ensure thermal stability: $R_{th\ j\text{-}a} < 1$ °C/W (d.c. blocking) or $< 2$ °C/W (a.c.). For smaller heatsinks $T_{j\ max}$ should be derated. For a.c. see Fig. 4.

## CHARACTERISTICS

### Anode to cathode

| | | | |
|---|---|---|---|
| On-state voltage<br>$I_T$ = 100 A; $T_j$ = 25 °C | $V_T$ | < | 1,9 V * |
| Rate of rise of off-state voltage that will not trigger any device; exponential method; $V_D$ = 2/3 $V_{DRMmax}$;<br>$T_j$ = 125 °C | $dV_D/dt$ | < | 200 V/μs |
| Reverse current<br>$V_R$ = $V_{RWMmax}$; $T_j$ = 125 °C | $I_R$ | < | 10 mA |
| Off-state current<br>$V_D$ = $V_{DWMmax}$; $T_j$ = 125 °C | $I_D$ | < | 10 mA |
| Latching current; $T_j$ = 25 °C | $I_L$ | < | 300 mA |
| Holding current; $T_j$ = 25 °C | $I_H$ | < | 200 mA |

### Gate to cathode

| | | | |
|---|---|---|---|
| Voltage that will trigger all devices<br>$V_D$ = 6 V; $T_j$ = 25 °C | $V_{GT}$ | > | 2,5 V |
| Voltage that will not trigger any device<br>$V_D$ = $V_{DRMmax}$; $T_j$ = 125 °C | $V_{GD}$ | < | 200 mV |
| Current that will trigger all devices<br>$V_D$ = 6 V; $T_j$ = 25 °C | $I_{GT}$ | > | 100 mA |

### Switching characteristics

| | | | |
|---|---|---|---|
| Gate-controlled turn-on time ($t_{gt}$ = $t_d$ + $t_r$) when switched from $V_D$ = $V_{DWMmax}$ to $I_T$ = 100 A; $I_{GT}$ = 150 mA; $dI_G/dt$ = 1 A/μs; $T_j$ = 25 °C | $t_{gt}$ | typ. | 2 μs |
| | $t_r$ | typ. | 1 μs |

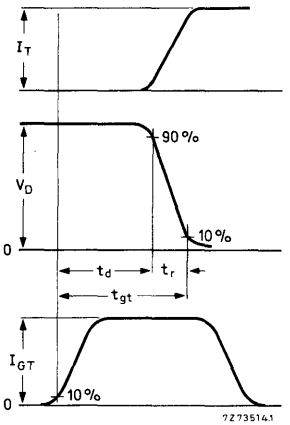



Fig. 2 Gate-controlled turn-on time definitions.

* Measured under pulse conditions to avoid excessive dissipation.

**CHARACTERISTICS** (continued)

Circuit-commutated turn-off time when switched
from $I_T$ = 30 A to $V_R \geqslant$ 50 V with $-dI_T/dt$ = 30 A/$\mu$s;
$dV_D/dt$ = 100 V/$\mu$s;

| | | | |
|---|---|---|---|
| $T_j$ = 125 °C | $t_q$ | typ. | 140 $\mu$s |
| | | < | 200 $\mu$s |
| $T_j$ = 25 °C | $t_q$ | < | 100 $\mu$s |

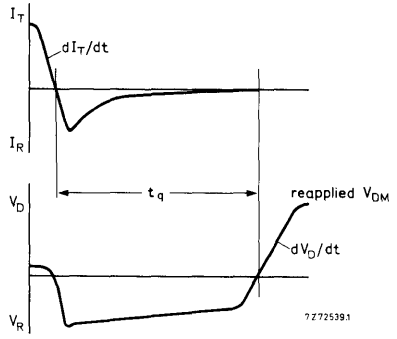



Fig. 3 Circuit-commutated turn-off time definition.

**OPERATING NOTE**

Switching losses in commutation

For applications in which the thyristor is forced to switch from an on-state current $I_{TRM}$ to a high reverse voltage at a high commutation rate ($-dI_T/dt$), consult Fig. 14 (nomogram) to find the increase in total average power. This increase must be added to the loss from the curves in Fig. 4.

**ORDERING NOTE**

Types with $dV_D/dt$ of 1000 V/$\mu$s are available on request. Add suffix C to the type number when ordering; e.g. BTW24-600RC.

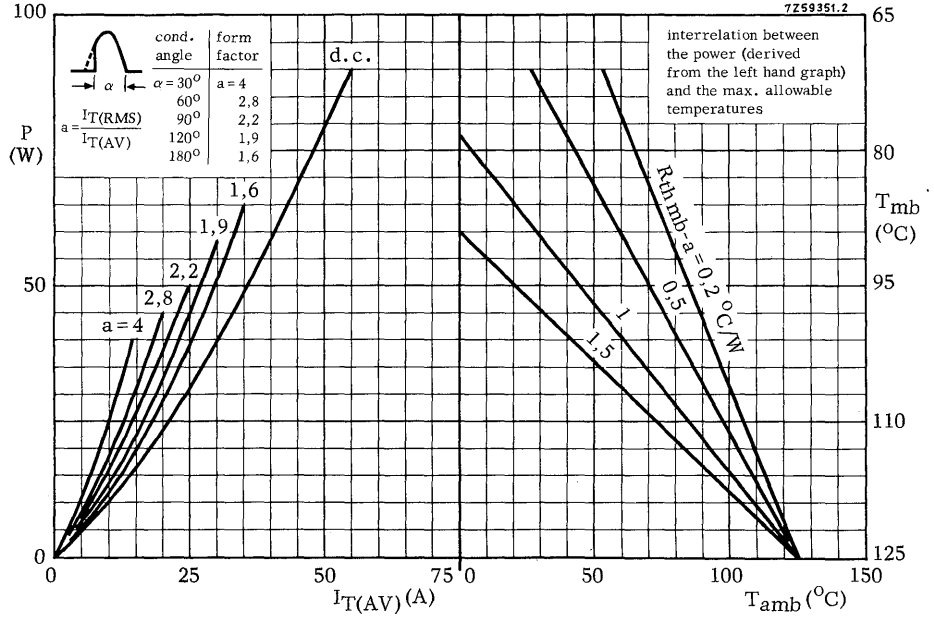

7Z59351.2
cond. angle
form factor
α = 30° a = 4
60° 2,8
90° 2,2
120° 1,9
180° 1,6
a = I T(RMS) / I T(AV)
d.c.
1,6
1,9
2,2
2,8
a = 4
P (W)
100
50
0
0
25
50
75
I T(AV) (A)
interrelation between the power (derived from the left hand graph) and the max. allowable temperatures
Rth mb-a = 0,2 °C/W
0,5
1
1,5
65
80
95
110
125
T mb (°C)
0
50
100
150
T amb (°C)

Fig. 4.

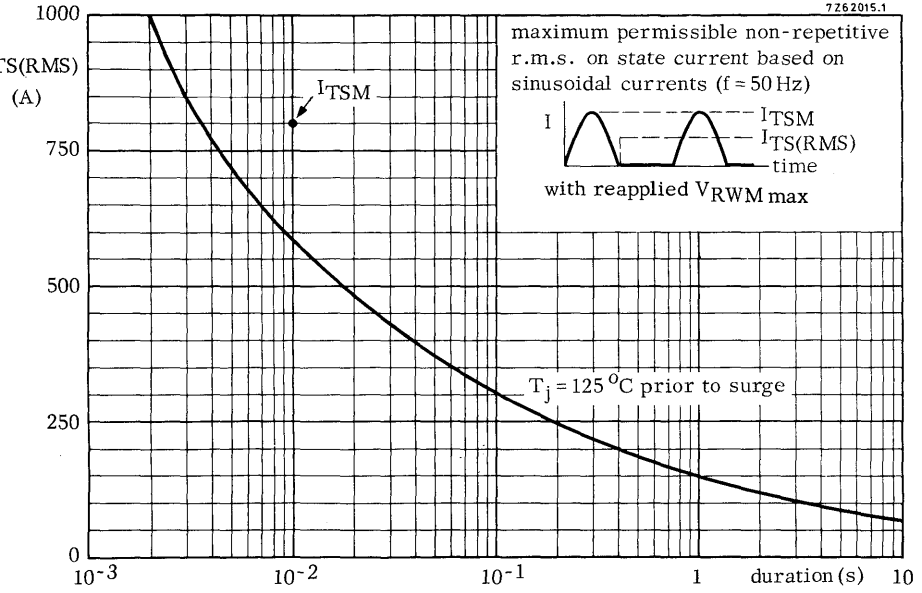

7Z62015.1
1000
750
500
250
0
TS(RMS) (A)
maximum permissible non-repetitive r.m.s. on state current based on sinusoidal currents (f = 50 Hz)
I
I TSM
I TS(RMS)
time
with reapplied V RWM max
I TSM
T j = 125 °C prior to surge
10-3
10-2
10-1
1
10
duration (s)

Fig. 5.

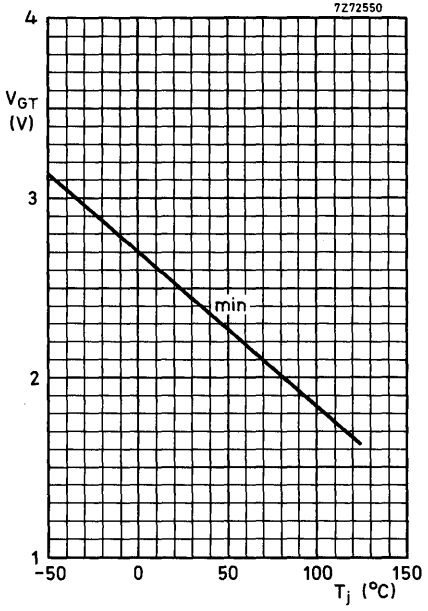



Fig. 6 Minimum gate voltage that will trigger all devices plotted against junction temperature.

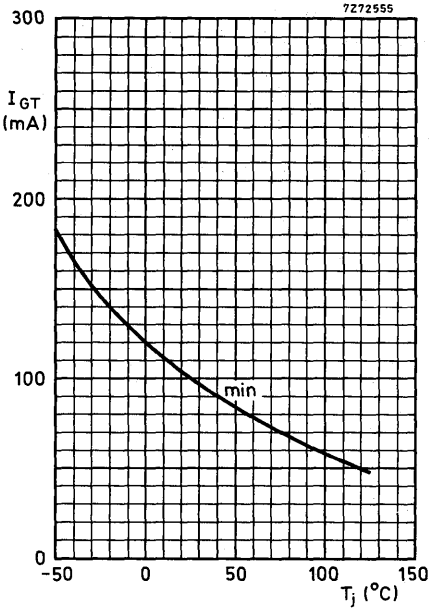



Fig. 7 Minimum gate current that will trigger all devices plotted against junction temperature.

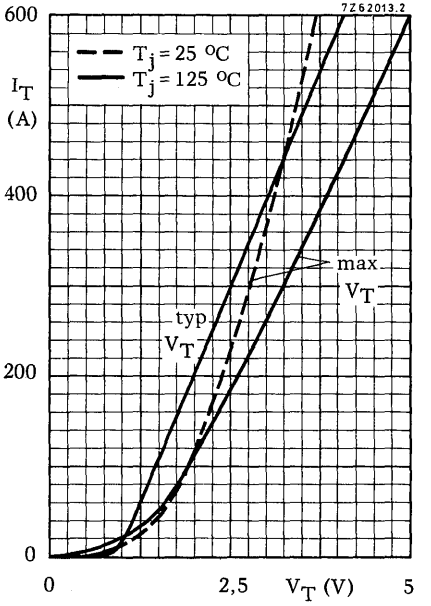



Fig. 8.

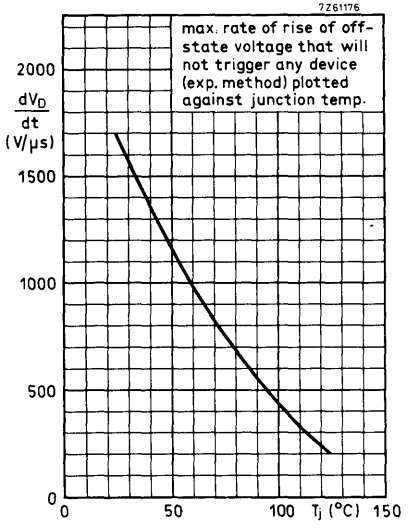



Fig. 9.

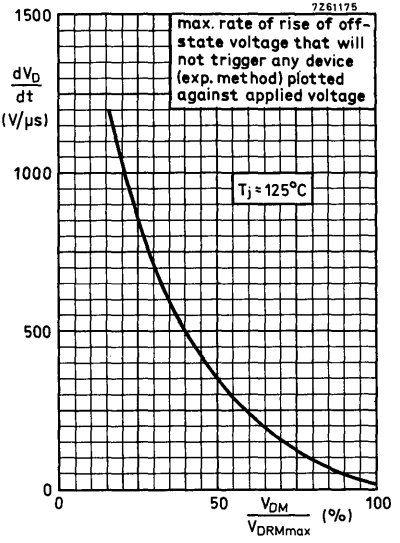



Fig. 10.

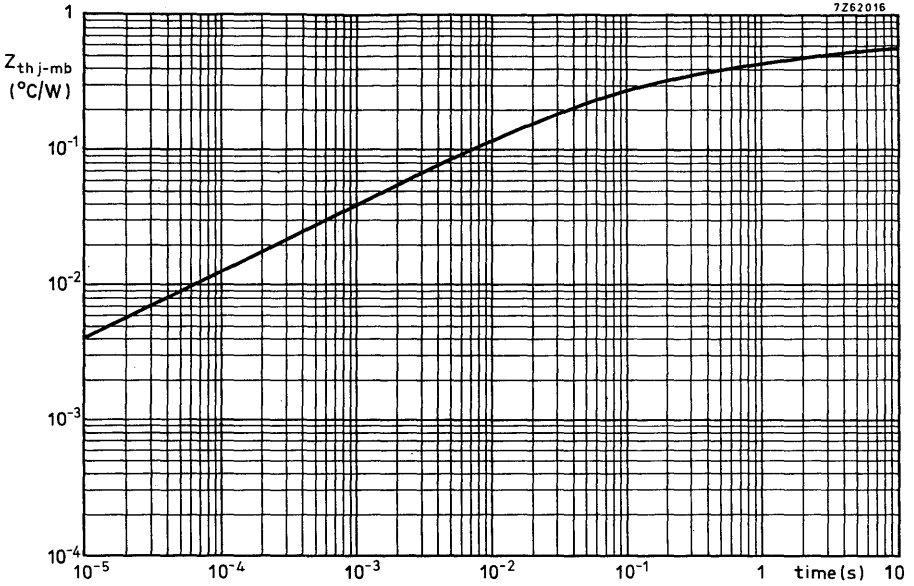
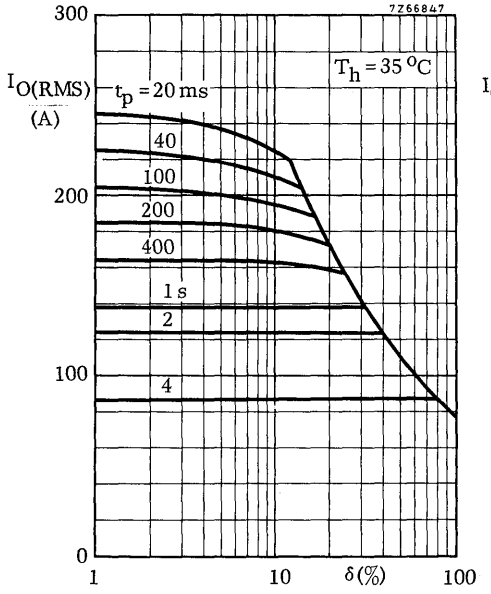
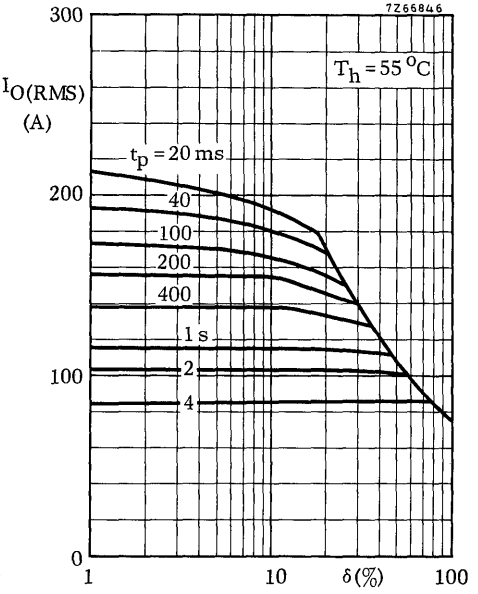
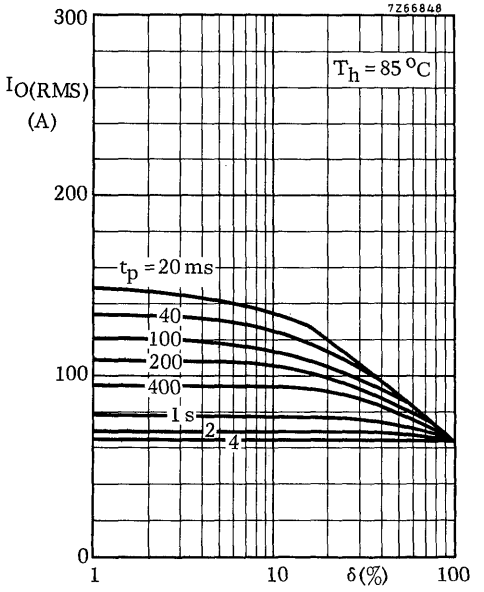



Fig. 11.



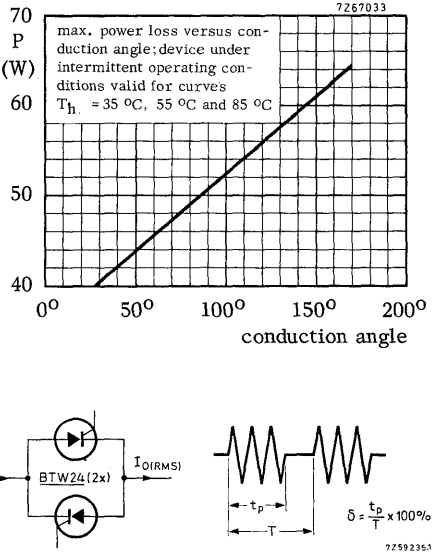




Fig. 12 Intermittent overload capability of two BTW24 thyristors in anti-parallel connection in a single phase a.c. control circuit (e.g. welding); conduction angle: 360°.

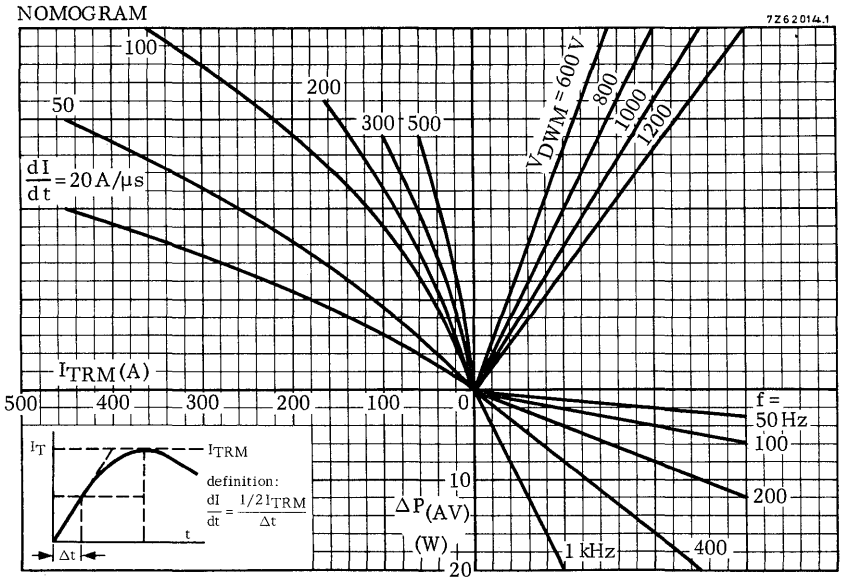



Fig. 13 Power loss $\Delta P_{(AV)}$ due to switching-on; $T_j$ = 125 °C; $I_G$ = 500 mA; $dI_G/dt$ = 1 A/μs.

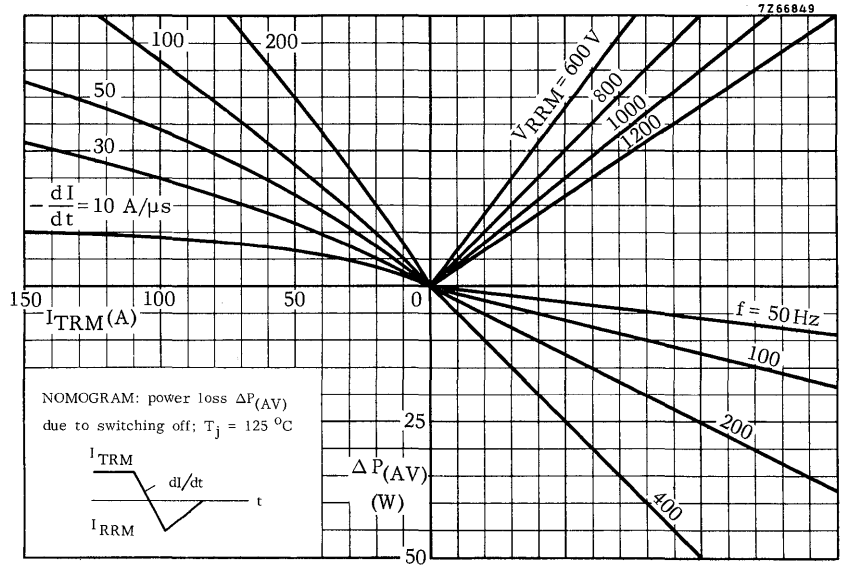
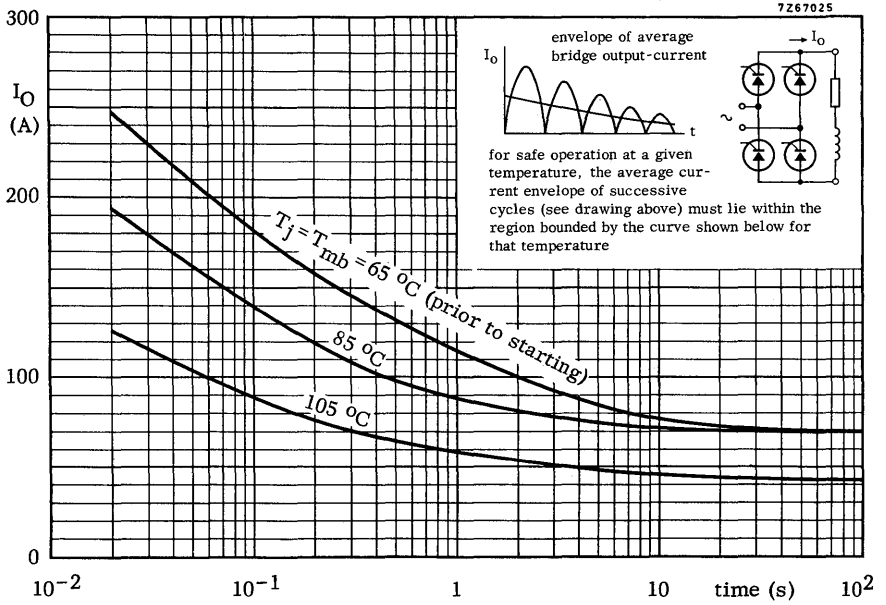



Fig. 14.



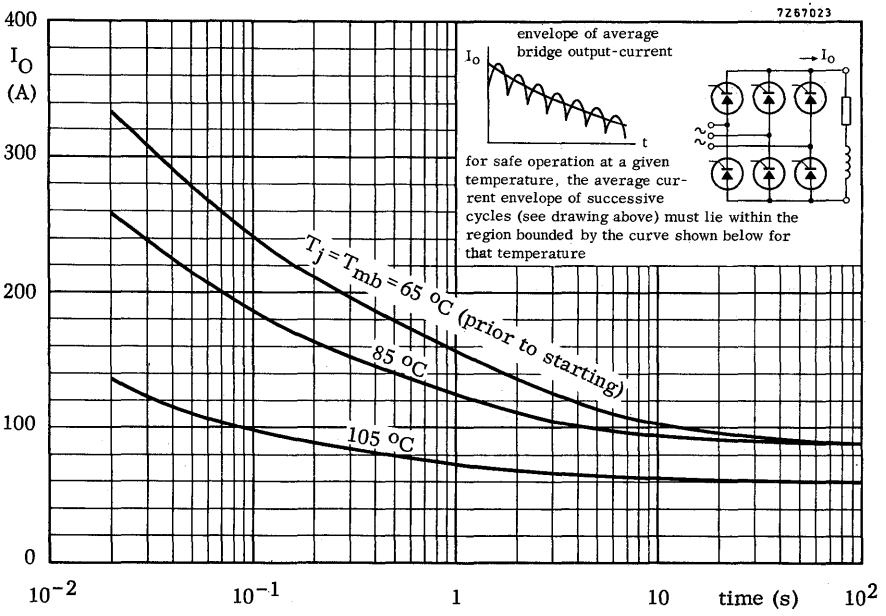




Fig. 15 Limits for starting or inrush currents.