

FAST TURN-OFF THYRISTORS

A range of medium current fast turn-off thyristors in metal envelopes, intended for use in inverter applications.

The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTW30-800RS to 1200RS.

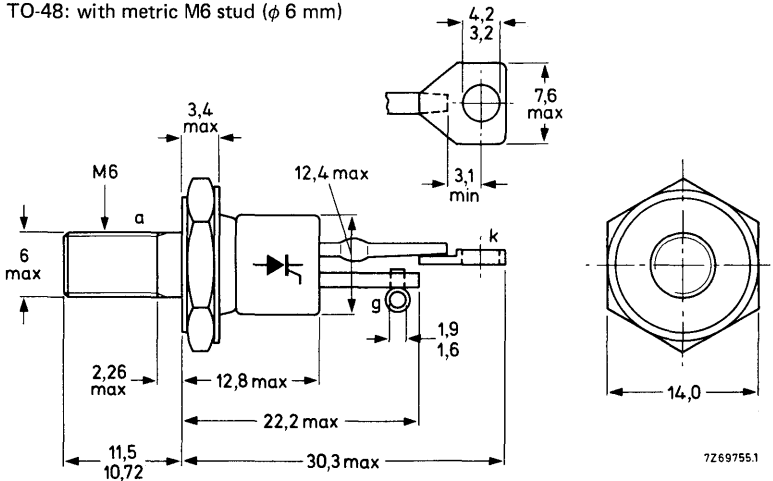
QUICK REFERENCE DATA

	V_{DRM}/V_{RRM}	BTW30-800RS 1000RS 1200RS		
		max.	800	1000 1200 V
Repetitive peak voltages				
Average on-state current			$I_T(AV)$	max. 16 A
R.M.S. on-state current			$I_T(RMS)$	max. 24 A
Non-repetitive peak on-state current			I_{TSM}	max. 150 A
Rate of rise of on-state current			dI_T/dt	max. 100 A/ μs
Rate of rise of off-state voltage that will not trigger any device			dV_D/dt	< 200 V/ μs
Circuit-commutated turn-off time			t_q	< 15 μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-48: with metric M6 stud (ϕ 6 mm)



7269755.1

Net mass: 14 g
Diameter of clearance hole: max. 6,5 mm
Accessories supplied on request: 56264A
(mica washer, insulating ring, soldering tag)

Torque on nut: min. 1,7 Nm (17 kg cm)
max. 3,5 Nm (35 kg cm)

Supplied with device:
1 nut, 1 lock washer
Nut dimensions across the flats: 10 mm

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Anode to cathode

		BTW30-800RS	1000RS	1200RS
Non-repetitive peak voltages ($t \leq 10$ ms)	V_{DSM}^{**}/V_{RSM}	max. 800	1000	1200 V
Repetitive peak voltages	V_{DRM}/V_{RRM}	max. 800	1000	1200 V ▲
Crest working off-state voltage square-wave; $\delta = 0,5$	V_{DWM}	max. 600	800	1000 V*
Average on-state current assuming zero switching losses (averaged over any 20 ms period)				
square-wave; $\delta = 0,5$; up to $T_{mb} = 65$ °C		$I_T(AV)$	max.	16 A
square-wave; $\delta = 0,5$; at $T_{mb} = 85$ °C		$I_T(AV)$	max.	12 A
sinusoidal; at $T_{mb} = 85$ °C		$I_T(AV)$	max.	10 A
R.M.S. on-state current		$I_T(RMS)$	max.	24 A
Repetitive peak on-state current		I_{TRM}	max.	150 A
Non-repetitive peak on-state current				
$T_j = 125$ °C prior to surge (see Fig. 6)				
$t = 10$ ms; half sine-wave		I_{TSM}	max.	150 A
$t = 5$ ms; square pulse		I_{TSM}	max.	150 A
$I^2 t$ for fusing ($t = 10$ ms)		$I^2 t$	max.	115 A ² s
Rate of rise of on-state current after triggering with $I_G = 1$ A to $I_T = 50$ A; $dI_G/dt = 1$ A/ μ s				
		dI_T/dt	max.	100 A/ μ s

Gate to cathode

Reverse peak voltage	V_{RGM}	max.	10 V
Average power dissipation (averaged over any 20 ms period)	$P_G(AV)$	max.	1 W
Peak power dissipation	P_{GM}	max.	5 W

Temperatures

Storage temperature	T_{stg}	-55 to + 125 °C
Junction temperature	T_j	max. 125 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th j-mb}$	=	1 °C/W
From mounting base to heatsink	$R_{th mb-h}$	=	0,2 °C/W
Transient thermal impedance ($t = 1$ ms)	$Z_{th j-mb}$	=	0,06 °C/W

* To ensure thermal stability: $R_{th j-a} < 3$ °C/W (d.c. blocking) or < 6 °C/W (square-wave; $\delta = 0,5$). For smaller heatsinks $T_{j max}$ should be derated. For square-wave see Fig. 5.

** Although not recommended, higher off-state voltages may be applied without damage, but the thyristor may switch into the on-state. The rate of rise of on-state current should not exceed 30 A/ μ s.

▲ Thermal stability at higher voltage ratings is dependent on duty factor. See Figs 15 and 16.

CHARACTERISTICS

Anode to cathode

On-state voltage

$I_T = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$

$V_T < 3,5 \text{ V}^*$

Rate of rise of off-state voltage that will not trigger

any device; exponential method; $V_D = 2/3 V_{DRM \text{ max}};$
 $T_j = 125 \text{ }^\circ\text{C}$

$dV_D/dt < 200 \text{ V}/\mu\text{s}$

Off-state current

$V_D = V_{DWM \text{ max}}; T_j = 125 \text{ }^\circ\text{C}$

$I_D < 7 \text{ mA}$

Holding current; $T_j = 25 \text{ }^\circ\text{C}$

$I_H < 200 \text{ mA}$

Gate to cathode

Voltage that will trigger all devices

$V_D = 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

$V_{GT} > 2,5 \text{ V}$

Voltage that will not trigger any device

$V_D = V_{DRM \text{ max}}; T_j = 125 \text{ }^\circ\text{C}$

$V_{GD} < 0,2 \text{ V}$

Current that will trigger all devices

$V_D = 6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

$I_{GT} > 200 \text{ mA}$

Switching characteristics

Gate-controlled turn-on time ($t_{gt} = t_d + t_r$) when
switched from $V_D = V_{DWM \text{ max}}$ to $I_T = 50 \text{ A};$

$I_{GT} = 200 \text{ mA}; dI_G/dt = 1 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$

$t_d < 1 \mu\text{s}$

$t_r < 1 \mu\text{s}$

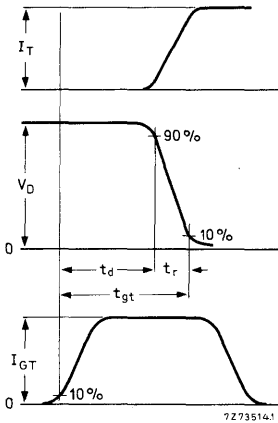


Fig. 2 Gate-controlled turn-on time definitions.

* Measured under pulse conditions to avoid excessive dissipation.

CHARACTERISTICS (continued)

Circuit-commutated turn-off time when switched
from $I_T = 10 \text{ A}$ to $V_R \geq 50 \text{ V}$ with $-dI_T/dt = 10 \text{ A}/\mu\text{s}$;
 $dV_D/dt = 50 \text{ V}/\mu\text{s}$; $T_j = 125 \text{ }^\circ\text{C}$

$$t_q < 15 \mu\text{s}$$

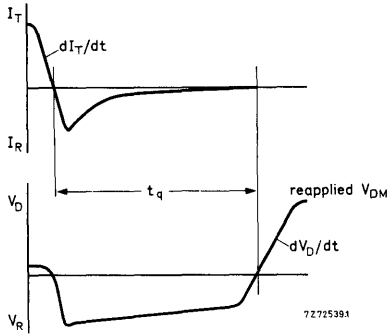
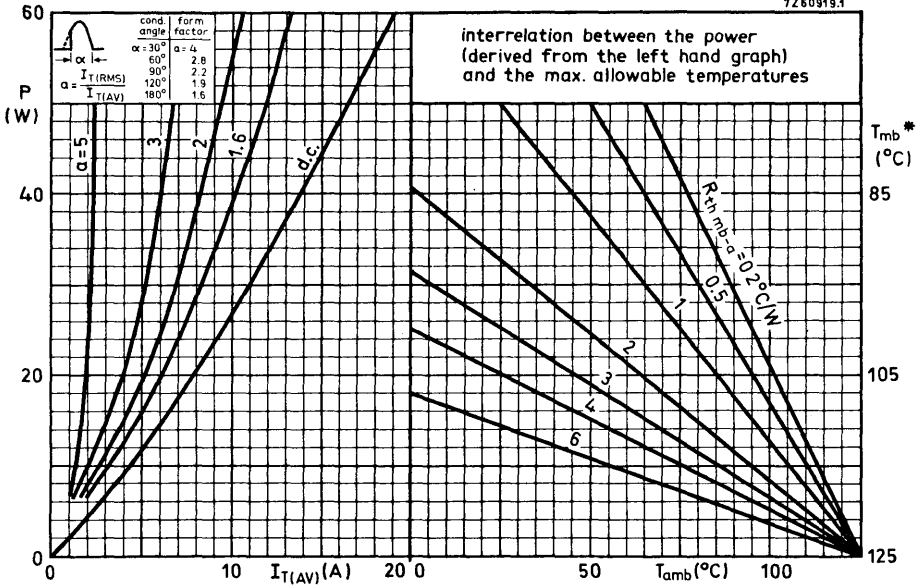


Fig. 3 Circuit-commutated turn-off time definitions.

OPERATING NOTES

1. The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.
During soldering the heat conduction to the junction should be kept to a minimum.
2. High frequency operation.
 - a. The curves in Figs 13 and 14 show the additional average power losses due to turning on and turning off the thyristor in square pulse operation. This power should be added to that derived from the curves in Fig. 5.
 - b. Power loss due to turn-off may be discounted if an inverse parallel diode is connected across the thyristor to clip any reverse voltage which may occur following commutation. Note should be taken of the consequent increase in turn-off time (see Fig. 11).

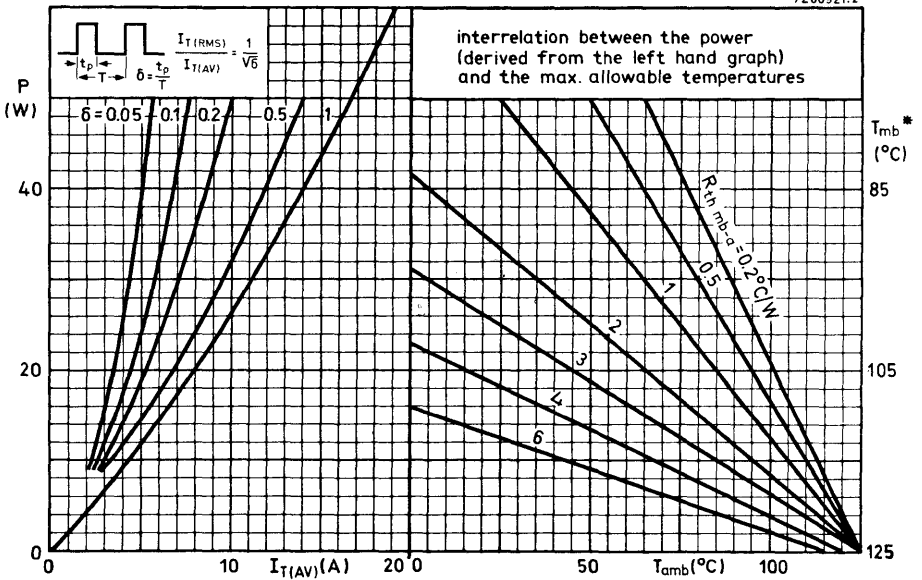
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* T_{mb} -scale is for comparison purposes only and is correct only for $R_{th mb-a} \leq 6^\circ\text{C/W}$

Fig. 4.

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* T_{mb} -scale is for comparison purposes only and is correct only for $R_{th mb-a} \leq 2^\circ\text{C/W}$

Fig. 5.

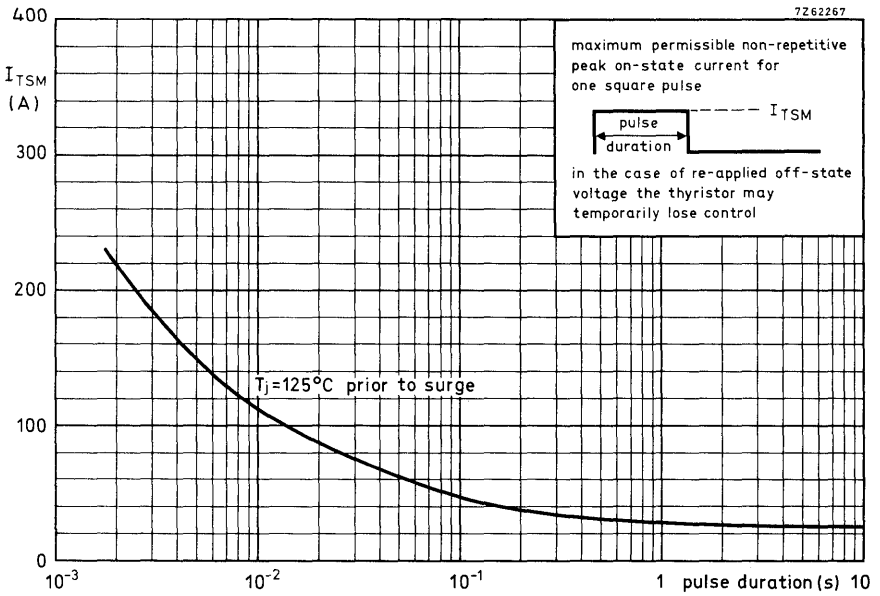


Fig. 6.

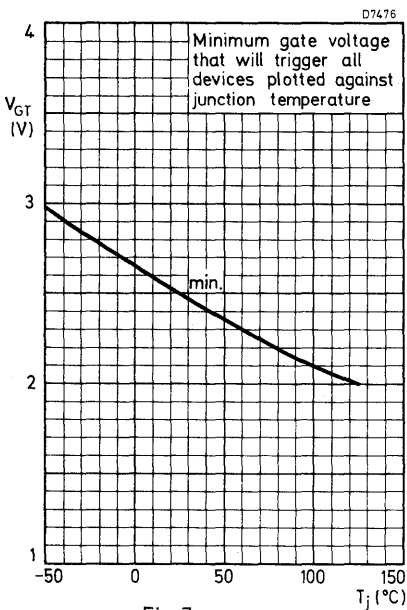


Fig. 7.

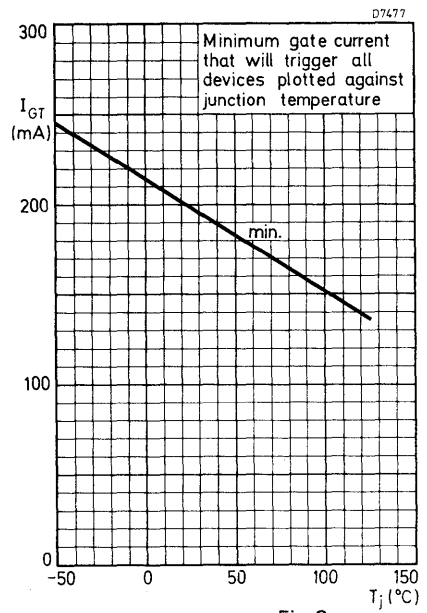


Fig. 8.

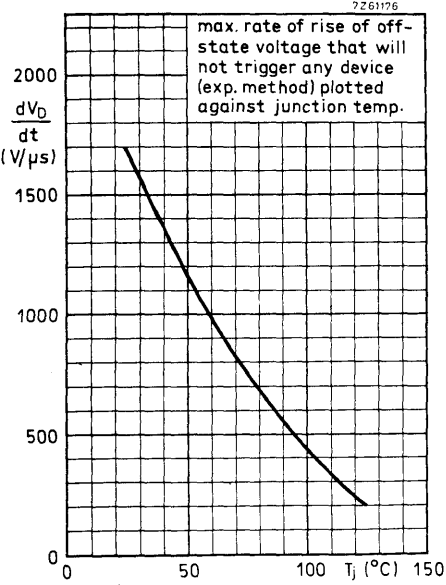


Fig. 9.

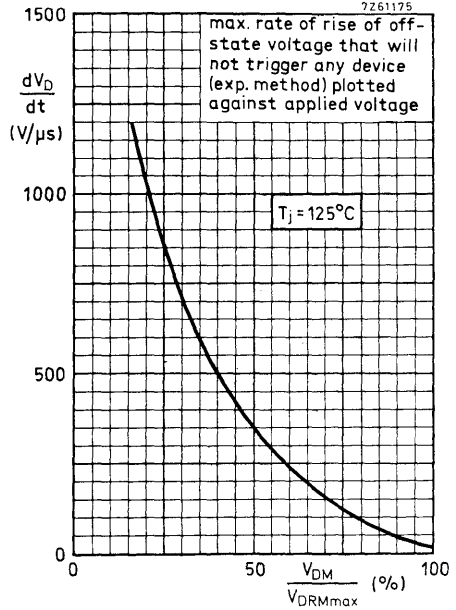


Fig. 10.

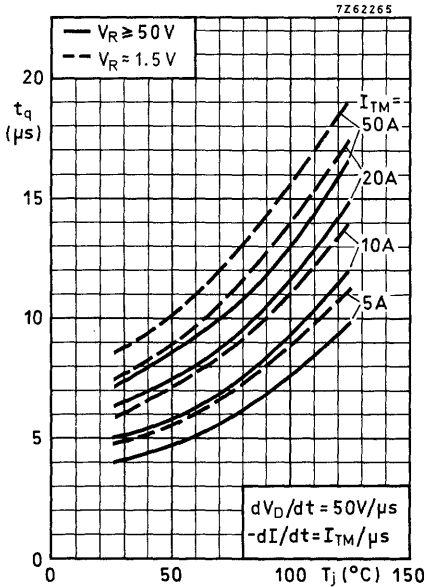


Fig. 11.

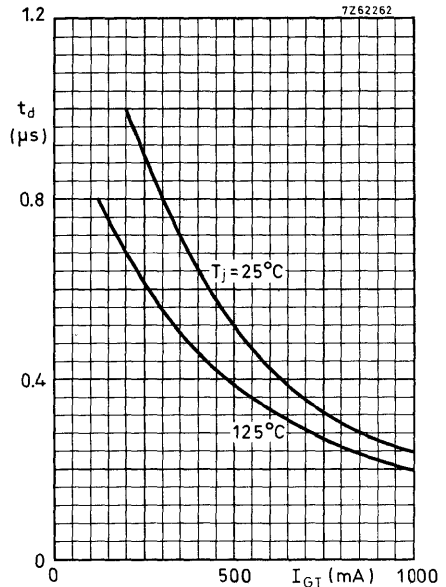


Fig. 12.

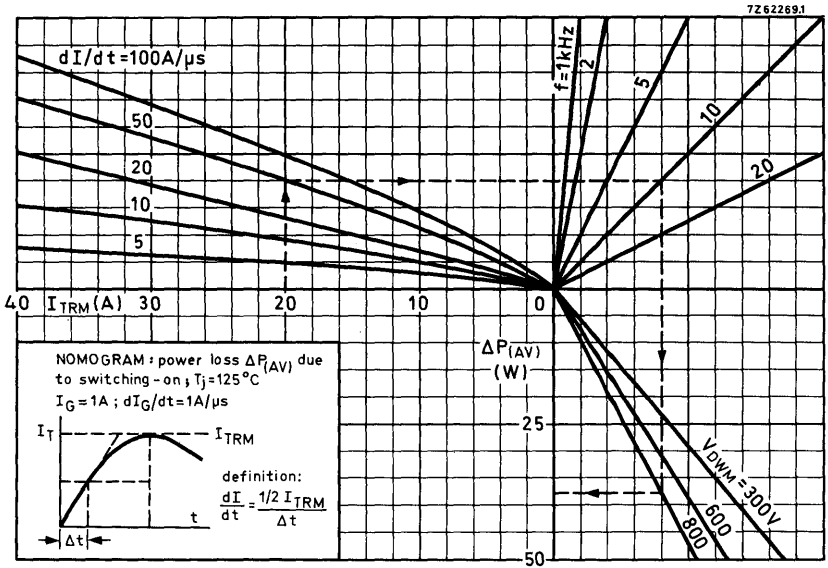


Fig. 13.

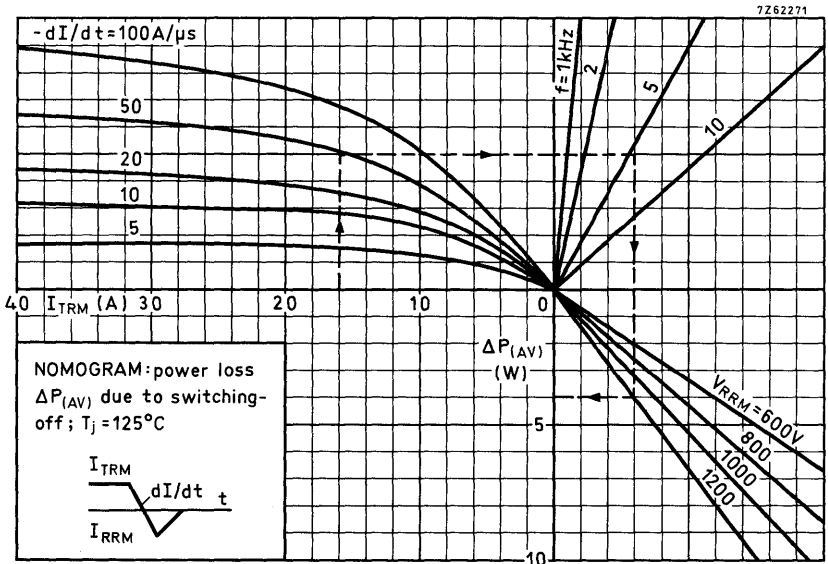


Fig. 14.

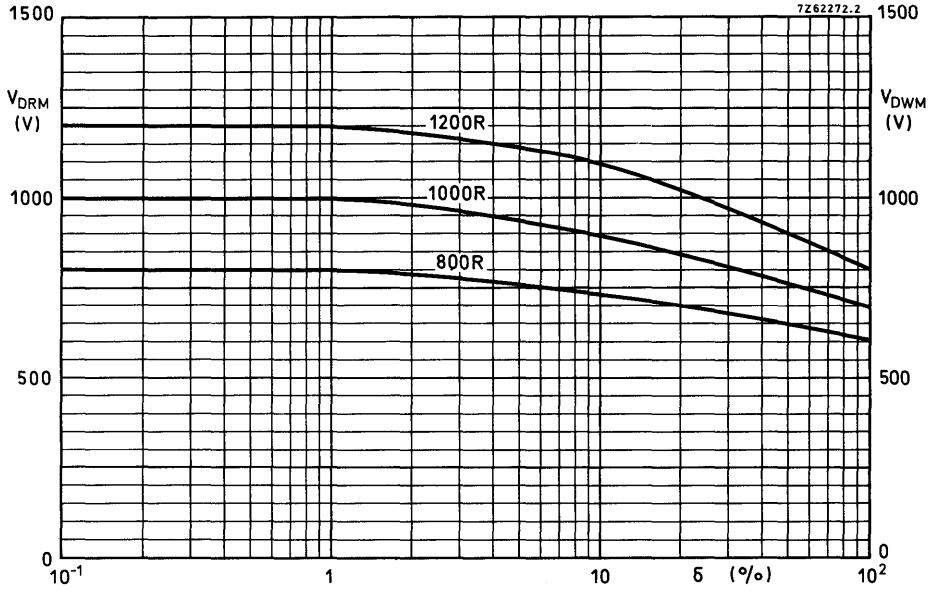


Fig. 15.

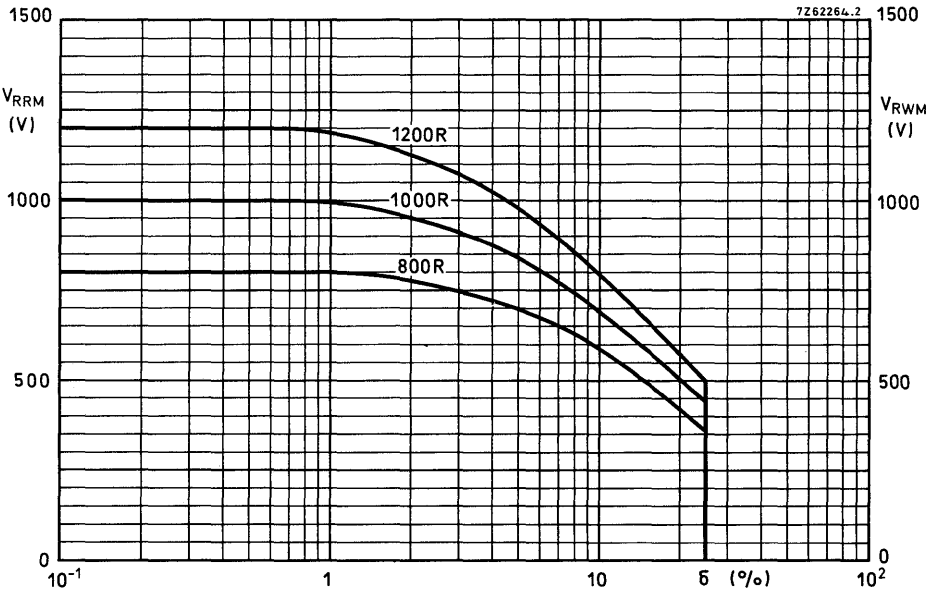


Fig. 16.

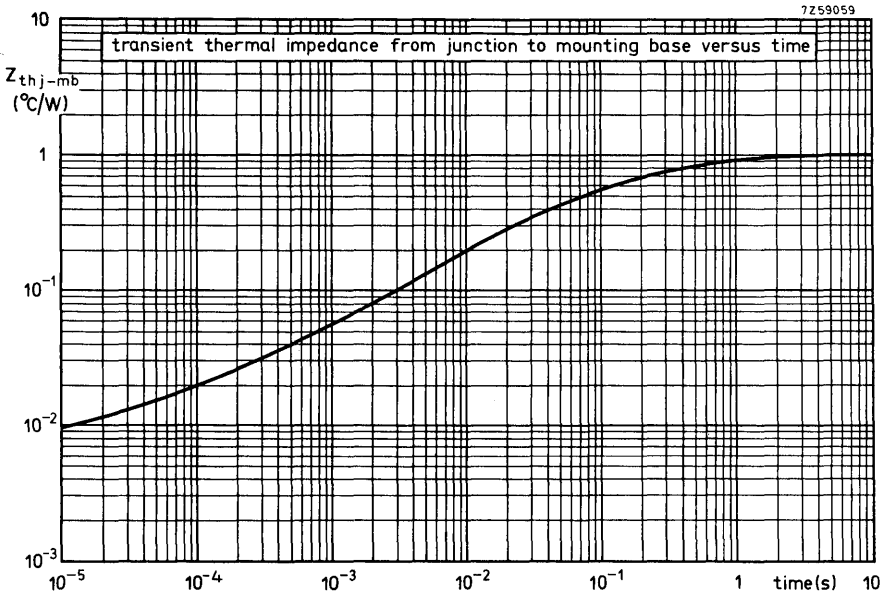


Fig. 17.