THYRISTORS

Also available to BS9341-F084

Silicon thyristors in metal envelopes with high dV_D/dt capabilities. They are intended for use in power control circuits and switching systems where high transients can occur (e.g. phase control in three-phase systems).

The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTW42-600R to 1200R.

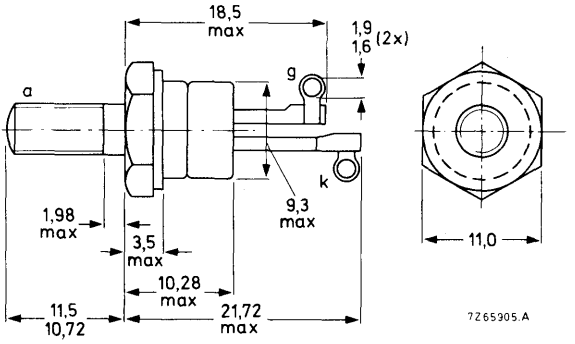
QUICK REFERENCE DATA

			BTW42- 600R	800R	1000R	1200R	
Repetitive peak voltages	V_{DRM}/V_{RRM}	max.	600	800	1000	1200	V
Average on-state current			$I_{T(AV)}$		max.	10	A
R.M.S. on-state current			$I_{T(RMS)}$		max.	16	A
Non-repetitive peak on-state current			I_{TSM}		max.	150	A
Rate of rise of off-state voltage that will not trigger any device			dV_D/dt		<	200	V/μs
On request (see ordering note on page 2)			dV_D/dt		<	1000	V/μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-64: with metric M5 stud (ϕ5 mm); e.g. BTW42-600R.



Net mass: 7 g
Diameter of clearance hole: max. 5,2 mm
Accessories supplied on request:
56295 (PTFE bush, 2 mica washers, plain washer, tag)
56262A (mica washer, insulating ring, plain washer)

Supplied with device: 1 nut, 1 lock washer
Nut dimensions across the flats; M5: 8,0 mm

Torque on nut: min. 0,9 Nm (9 kg cm)
max. 1,7 Nm (17 kg cm)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Anode to cathode

			BTW42-600R	800R	1000R	1200R	
Non-repetitive peak voltages ($t \leqslant 10$ ms)	V_{DSM}/V_{RSM}	max.	600	800	1000	1200	V
Repetitive peak voltages	V_{DRM}/V_{RRM}	max.	600	800	1000	1200	V
Crest working voltages	V_{DWM}/V_{RWM}	max.	400	600	700	800	V *

Average on-state current (averaged over any 20 ms period) up to $T_{mb} = 85$ °C	$I_{T(AV)}$	max.	10	A
R.M.S. on-state current	$I_{T(RMS)}$	max.	16	A
Repetitive peak on-state current	I_{TRM}	max.	75	A
Non-repetitive peak on-state current; t = 10 ms; half sine-wave; $T_j = 125$ °C prior to surge; with reapplied V_{RWMmax}	I_{TSM}	max.	150	A
I^2t for fusing (t = 10 ms)	I^2t	max.	112	A^2s
Rate of rise of on-state current after triggering with $I_G = 250$ mA to $I_T = 25$ A; $dI_G/dt = 0{,}25$ A/µs	dI_T/dt	max.	50	A/µs

Gate to cathode

Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	0,5	W
Peak power dissipation	P_{GM}	max.	5	W

Temperatures

Storage temperature	T_{stg}		−55 to + 125	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,8	°C/W
From mounting base to heatsink with heatsink compound	$R_{th\ mb\text{-}h}$	=	0,5	°C/W
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	45	°C/W
Transient thermal impedance (t = 1 ms)	$Z_{th\ j\text{-}mb}$	=	0,1	°C/W

OPERATING NOTE

The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.
During soldering the heat conduction to the junction should be kept to a minimum.

ORDERING NOTE

Types with dV_D/dt of 1000 V/µs are available on request. Add suffix C to the type number when ordering; e.g. BTW42-600RC.

* To ensure thermal stability: $R_{th\ j\text{-}a} < 4$ °C/W (d.c. blocking) or < 8 °C/W (a.c.). For smaller heatsinks $T_{j\ max}$ should be derated. For a.c. see Fig. 3.

CHARACTERISTICS

Anode to cathode

On-state voltage I_T = 20 A; T_j = 25 °C	V_T	<	2 V *
Rate of rise of off-state voltage that will not trigger any device; exponential method; V_D = 2/3 V_{DRMmax}; T_j = 125 °C	dV_D/dt	<	200 V/μs
Reverse current $V_R = V_{RWMmax}$; T_j = 125 °C	I_R	<	3 mA
Off-state current $V_D = V_{DWMmax}$; T_j = 125 °C	I_D	<	3 mA
Latching current; T_j = 25 °C	I_L	<	150 mA
Holding current; T_j = 25 °C	I_H	<	75 mA

Gate to cathode

Voltage that will trigger all devices V_D = 6 V; T_j = 25 °C	V_{GT}	>	1,5 V
Voltage that will not trigger any device $V_D = V_{DRMmax}$; T_j = 125 °C	V_{GD}	<	200 mV
Current that will trigger all devices V_D = 6 V; T_j = 25 °C	I_{GT}	>	50 mA

Switching characteristics

Gate-controlled turn-on time ($t_{gt} = t_d + t_r$) when switched from V_D = 800 V to I_T = 25 A; I_{GT} = 250 mA; dI_G/dt = 0,25 A/μs; T_j = 25 °C	t_{gt} t_r	< typ.	1,5 μs 0,2 μs

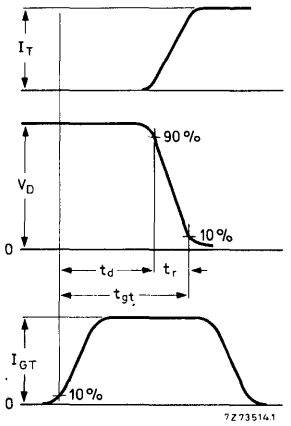


Fig. 2 Gate-controlled turn-on time definitions.

* Measured under pulse conditions to avoid excessive dissipation.

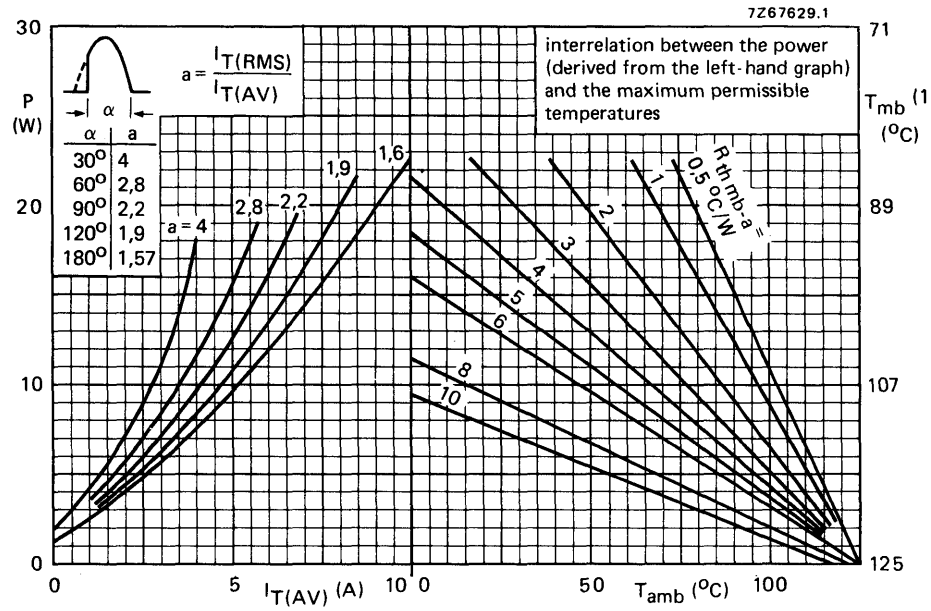


Fig. 3 (1) T_{mb}-scale is for comparison purposes only and is correct only for $R_{th\ mb\text{-}a} \leqslant 6$ °C/W.

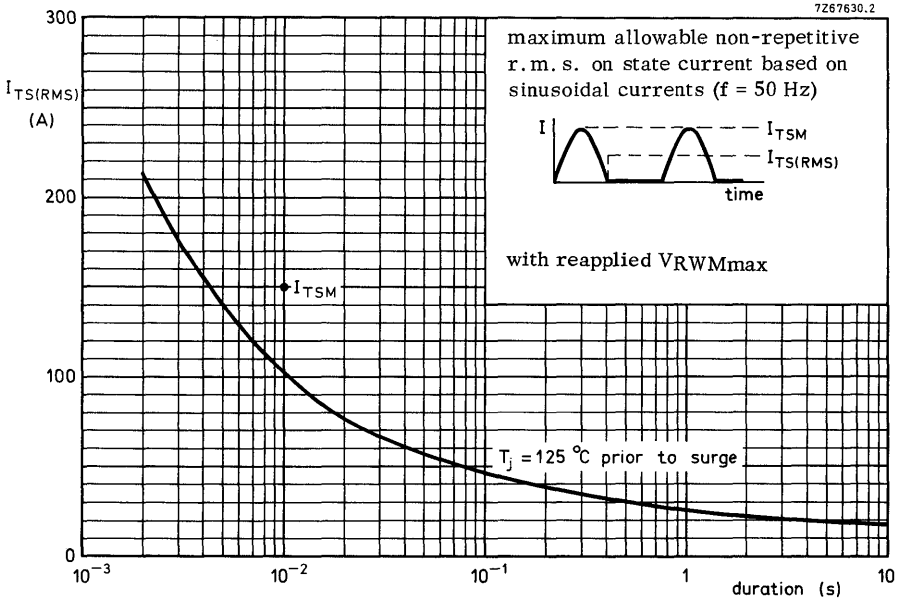


Fig. 4.

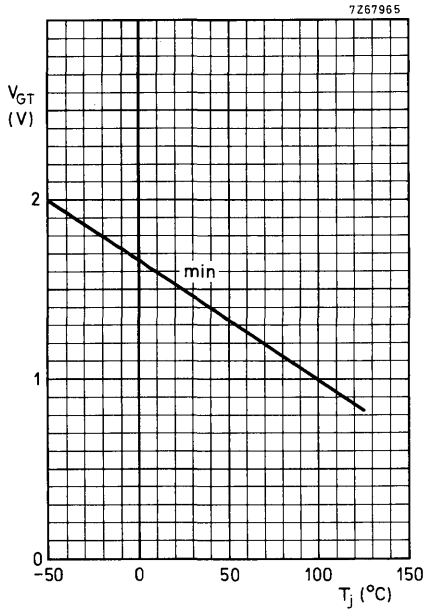


Fig. 5 Minimum gate voltage that will trigger all devices as a function of T_j.

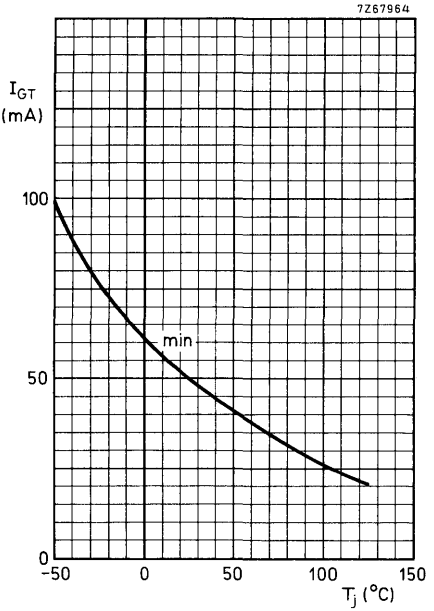


Fig. 6 Minimum gate current that will trigger all devices as a function of T_j.

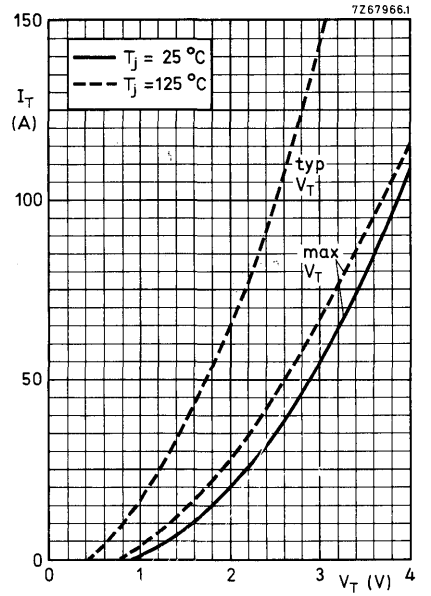


Fig. 7.

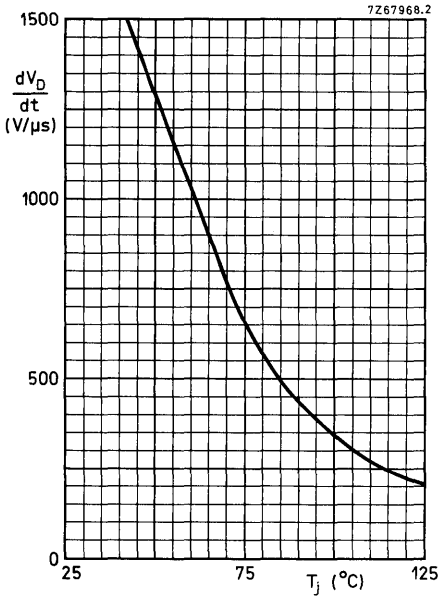


Fig. 8 Maximum rate of rise of off-state voltage that will not trigger any device (exponential method) as a function of T_j.

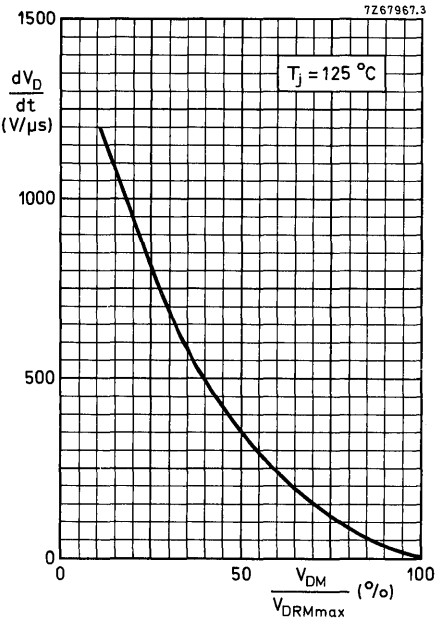
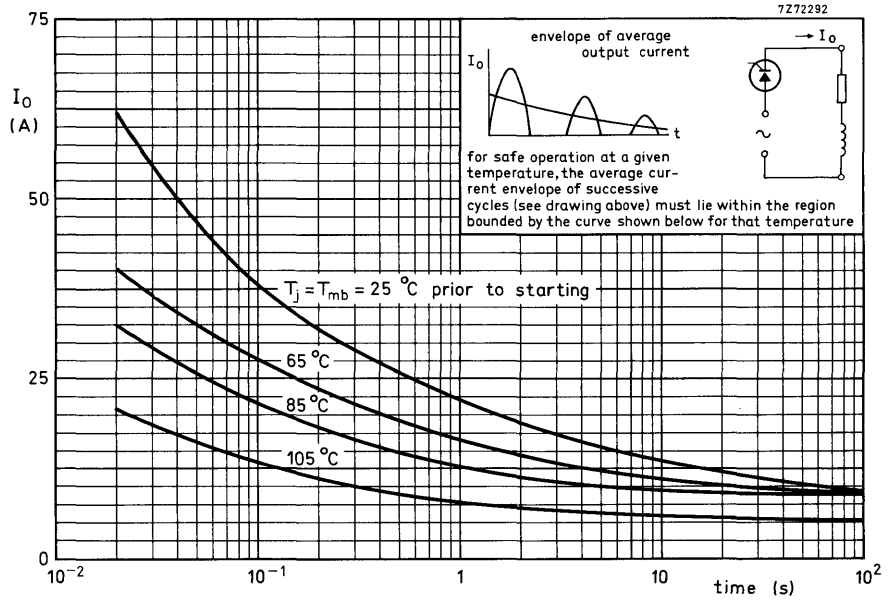


Fig. 9 Maximum rate of rise of off-state voltage that will not trigger any device (exponential method) as a function of applied voltage.



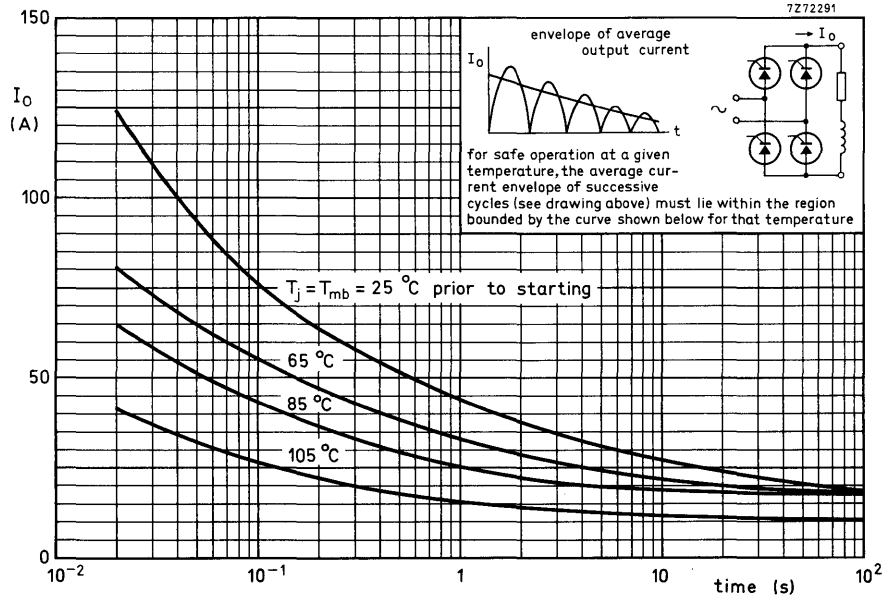


Fig. 10 Limits for starting or inrush currents.

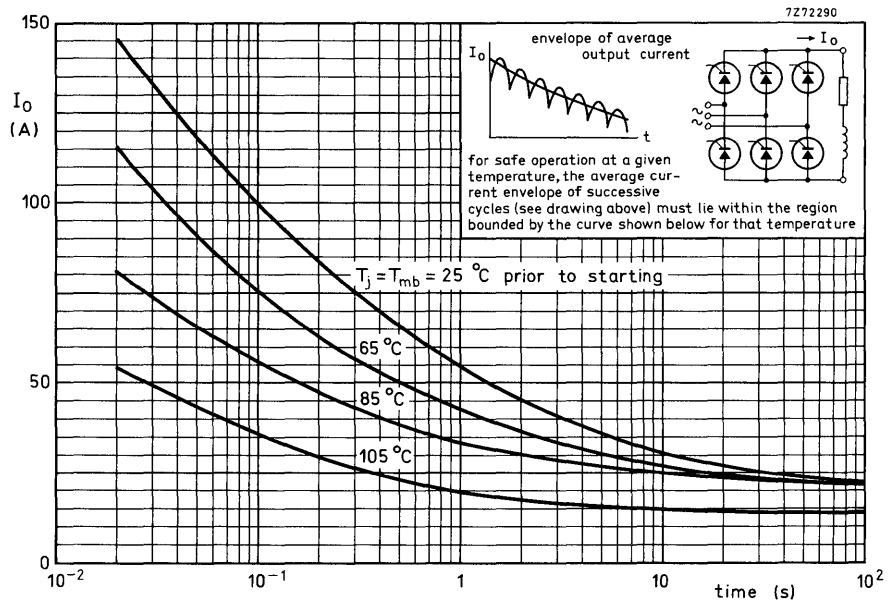


Fig. 11 Limits for starting or inrush currents.

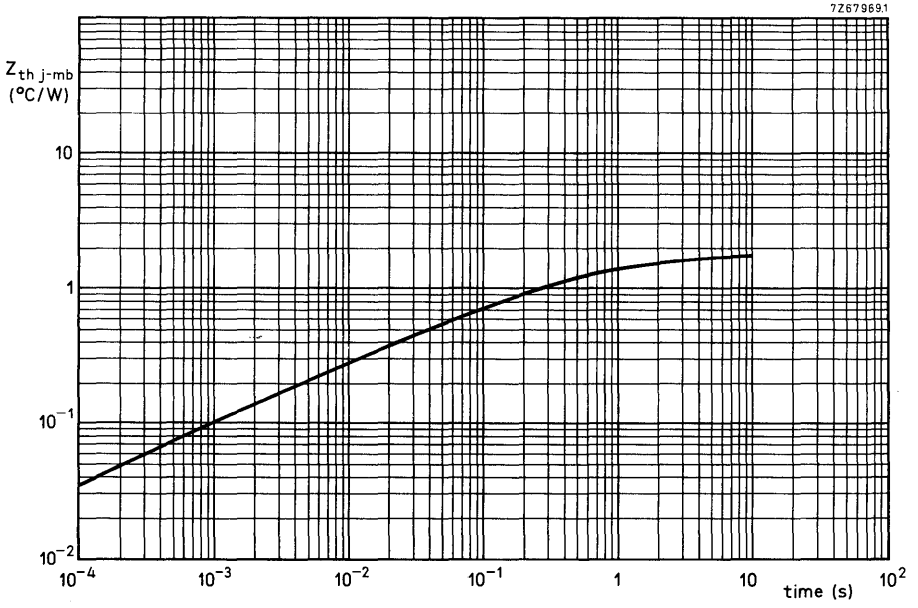


Fig. 12.