THYRISTORS

Silicon thyristors in metal envelopes, intended for power control applications.

The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTW45-400R to 1200R.

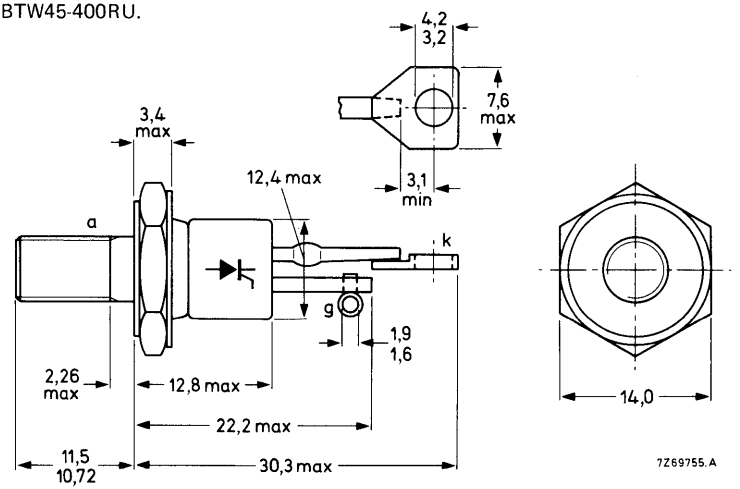
QUICK REFERENCE DATA

	BTW45-	400R	600R	800R	1000R	1200R	
Repetitive peak voltages $V_{DRM} = V_{RRM}$	max.	400	600	800	1000	1200	V
Average on-state current				$I_{T(AV)}$	max.	16	A
R.M.S. on-state current				$I_{T(RMS)}$	max.	25	A
Non-repetitive peak on-state current				I_{TSM}	max.	300	A
Rate of rise of off-state voltage that will not trigger any device				dV_D/dt	<	200	V/μs
On request (see ordering note on page 3)				dV_D/dt	<	1000	V/μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-48: with metric M6 stud (ϕ 6 mm); e.g. BTW45-400R.
Types with ¼ in x 28 UNF stud (ϕ 6,35 mm) are available on request. These are indicated by the suffix U: BTW45-400RU.



Net mass: 14 g
Diameter of clearance hole: max. 6,5 mm
Accessories supplied on request: 56264A
(mica washer, insulating ring, soldering tag)

Torque on nut: min. 1,7 Nm (17 kg cm)
max. 3,5 Nm (35 kg cm)
Supplied with the device:
1 nut, 1 lock washer
Nut dimensions across the flats;
M6: 10 mm
¼ in x 28 UNF: 11,1 mm

Products approved to CECC 50 011-002, available on request

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Anode to cathode

			BTW45-400R	600R	800R	1000R	1200R	
Non-repetitive peak voltages ($t \leqslant 10$ ms)	V_{DSM}/V_{RSM}	max.	400	600	800	1000	1200	V
Repetitive peak voltages	V_{DRM}/V_{RRM}	max.	400	600	800	1000	1200	V
Crest working voltages	V_{DWM}/V_{RWM}	max.	300	400	600	700	800	V*

Average on-state current (averaged over any 20 ms period) up to $T_{mb} = 85$ °C	$I_{T(AV)}$	max.	16	A
R.M.S. on-state current	$I_{T(RMS)}$	max.	25	A
Repetitive peak on-state current	I_{TRM}	max.	200	A
Non-repetitive peak on-state current; t = 10 ms; half sine-wave; $T_j = 125$ °C prior to surge; with reapplied V_{RWM} max	I_{TSM}	max.	300	A
I^2t for fusing (t = 10 ms)	I^2t	max.	450	A^2s
Rate of rise of on-state current after triggering with $I_G = 400$ mA to $I_T = 60$ A; $dI_G/dt = 0{,}4$ A/µs	dI_T/dt	max.	100	A/µs

Gate to cathode

Reverse peak voltage	V_{RGM}	max.	10	V
Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	1	W
Peak power dissipation	P_{GM}	max.	5	W

Temperatures

Storage temperature	T_{stg}		−55 to + 125	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,33	°C/W
From mounting base to heatsink; with heatsink compound	$R_{th\ mb\text{-}h}$	=	0,2	°C/W
Transient thermal impedance (t = 1 ms)	$Z_{th\ j\text{-}mb}$	=	0,1	°C/W

OPERATING NOTE

The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.
During soldering the heat conduction to the junction should be kept to a minimum.

* To ensure thermal stability: $R_{th\ j\text{-}a} < 6{,}5$ °C/W (d.c. blocking) or < 13 °C/W (a.c.). For smaller heatsinks $T_{j\ max}$ should be derated. For a.c. see Fig. 2.

CHARACTERISTICS

Anode to cathode

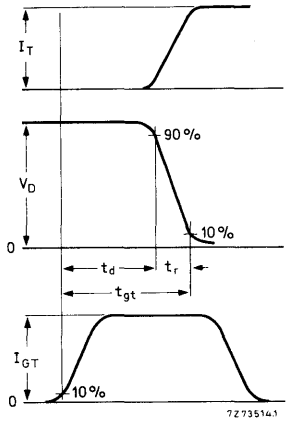
On-state voltage I_T = 50 A; T_j = 25 °C	V_T	<	2 V*
Rate of rise of off-state voltage that will not trigger any device; exponential method; V_D = 2/3 $V_{DRM\,max}$; T_j = 125 °C	dV_D/dt	<	200 V/μs
Reverse current V_R = $V_{RWM\,max}$; T_j = 125 °C	I_R	<	3 mA
Off-state current V_D = $V_{DWM\,max}$; T_j = 125 °C	I_D	<	3 mA
Latching current; T_j = 25 °C	I_L	<	150 mA
Holding current; T_j = 25 °C	I_H	<	75 mA

Gate to cathode

Voltage that will trigger all devices V_D = 6 V; T_j = 25 °C	V_{GT}	>	1,5 V
Voltage that will not trigger any device V_D = $V_{DRM\,max}$; T_j = 125 °C	V_{GD}	<	200 mV
Current that will trigger all devices V_D = 6 V; T_j = 25 °C	I_{GT}	>	75 mA

Switching characteristics ←

Gate-controlled turn-on time (t_{gt} = t_d + t_r) when switched from V_D = $V_{DWM\,max}$ to I_T = 100 A; I_{GT} = 400 mA; dI_G/dt = 1 A/μs; T_j = 25 °C	t_{gt} t_r	< <	1 μs 0,5 μs



Gate-controlled turn-on time definition.

ORDERING NOTE

Types with dV_D/dt of 1000 V/μs are available on request. Add suffix C to the type number when ordering; e.g. BTW45-400RC.

*Measured under pulse conditions to avoid excessive dissipation.

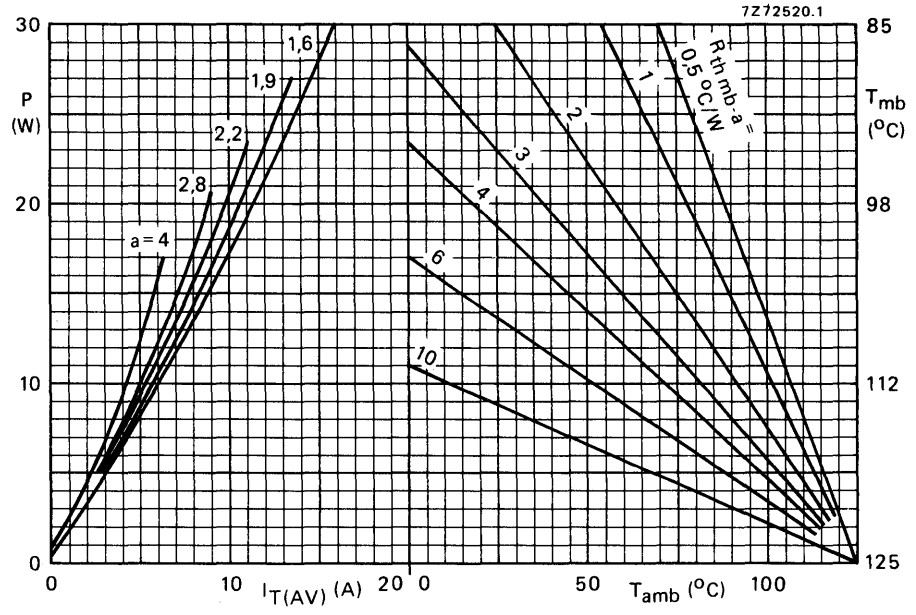

7Z72520.1
30
P
(W)
20
10
0
85
Tmb
(°C)
98
112
125
1,6
1,9
2,2
2,8
a = 4
Rth mb-a =
0,5 °C/W
1
2
3
4
6
10
0
10
IT(AV) (A)
20
0
50
Tamb (°C)
100

Fig. 2.

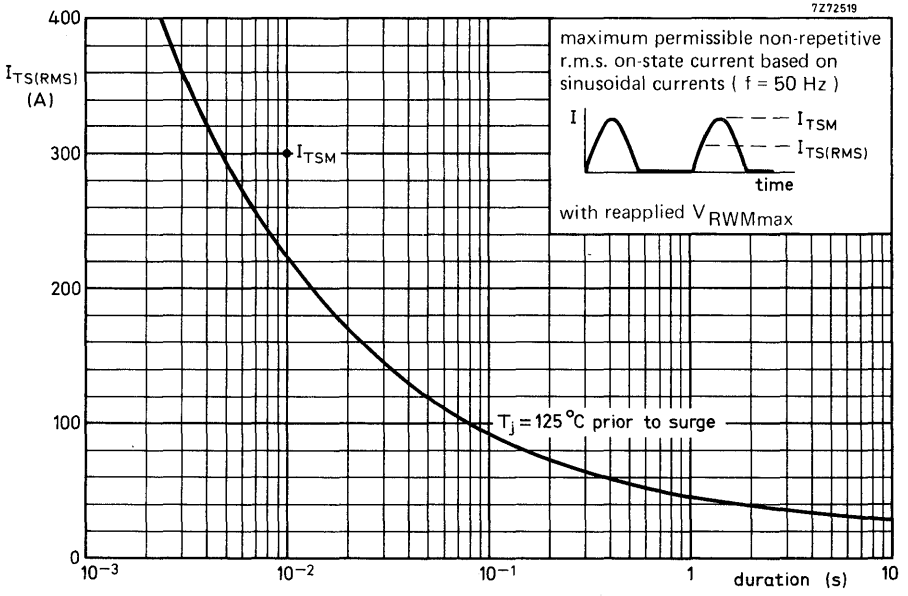

7Z72519
400
ITS(RMS)
(A)
300
200
100
0
ITSM
maximum permissible non-repetitive
r.m.s. on-state current based on
sinusoidal currents (f = 50 Hz)
I
ITSM
ITS(RMS)
time
with reapplied VRWMmax
Tj = 125 °C prior to surge
10−3
10−2
10−1
1
10
duration (s)

Fig. 3.

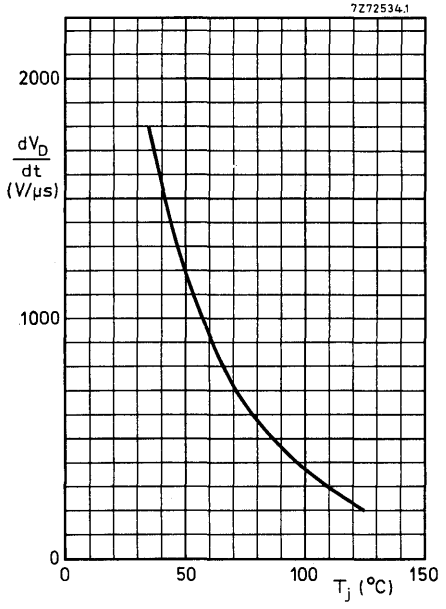


Fig. 4 Maximum rate of rise of off-state voltage that will not trigger any device (exponential method) as a function of T_j.

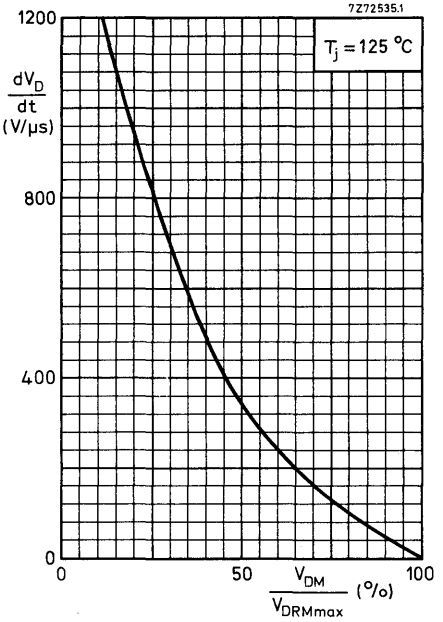


Fig. 5 Maximum rate of rise of off-state voltage that will not trigger any device (exponential method) as a function of applied voltage.

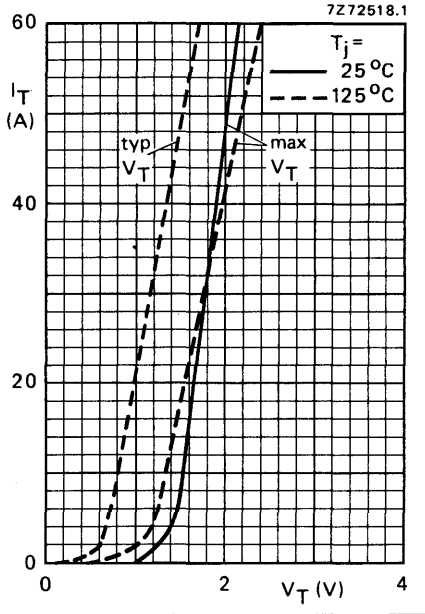


Fig. 6.

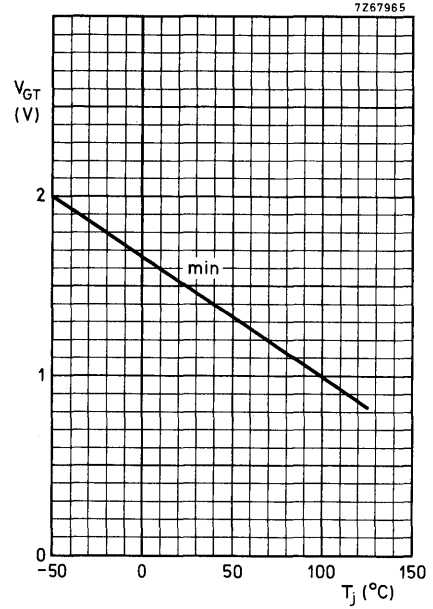


Fig. 7 Minimum gate voltage that will trigger all devices as a function of T_j.

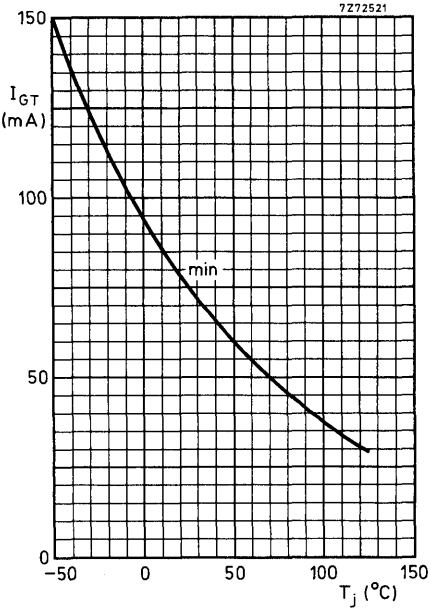


Fig. 8 Minimum gate current that will trigger all devices as a function of T_j.

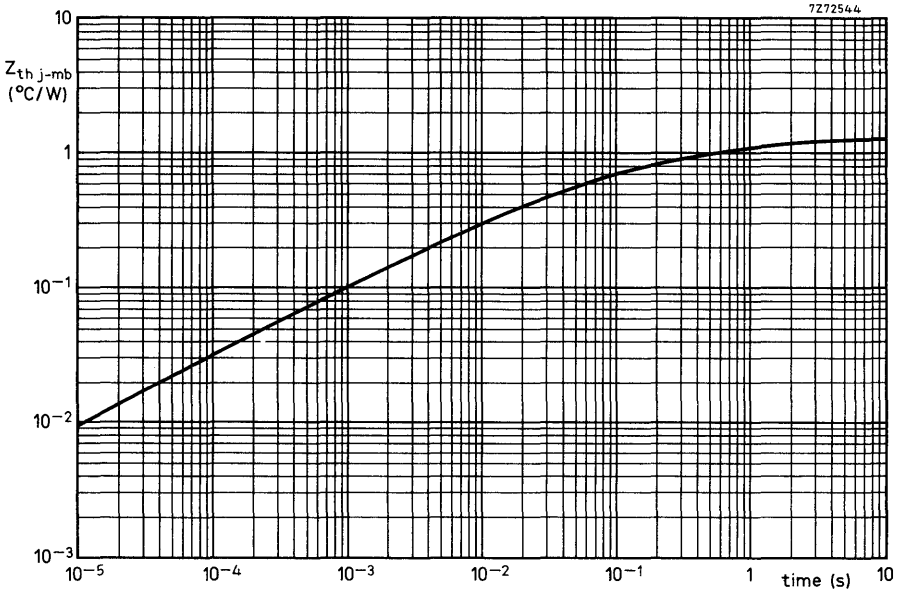


Fig. 9.