THYRISTORS

Silicon thyristors in metal envelopes, primarily intended for three-phase mains operation. The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTW47-800R to 1600R.

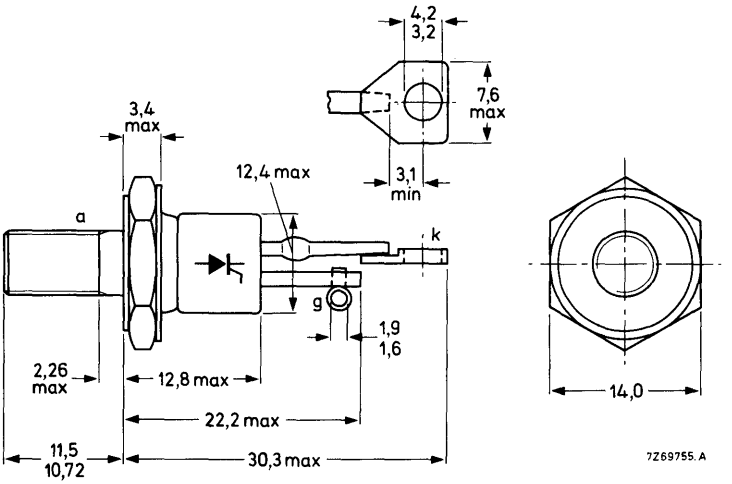
QUICK REFERENCE DATA

	BTW47-800R	1000R	1200R	1400R	1600R	
Repetitive peak voltages $V_{DRM} = V_{RRM}$	max. 800	1000	1200	1400	1600	V
Average on-state current			$I_{T(AV)}$ max.		16	A
R.M.S. on-state current			$I_{T(RMS)}$ max.		25	A
Non-repetitive peak on-state current			I_{TSM} max.		300	A
Rate of rise of off-state voltage that will not trigger any device			dV_D/dt <		300	V/μs
On request (see ordering note on page 4)			dV_D/dt <		1000	V/μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-48: with metric M6 stud (φ 6 mm); e.g. BTW47-800R.
Types with ¼ in x 28UNF stud (φ 6,35 mm) are available on request. These are indicated by the suffix U: BTW47-800RU.



Net mass: 14 g
Diameter of clearance hole: max. 6,5 mm
Accessories supplied on request: 56264A
(mica washer, insulating ring, soldering tag)

Torque on nut: min. 1,7 Nm (17 kg cm)
max. 3,5 Nm (35 kg cm)
Supplied with the device:
1 nut, 1 lock washer
Nut dimensions across the flats;
M6: 10 mm
¼ in x 28 UNF: 11,1 mm

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Anode to cathode

		BTW47-800R	1000R	1200R	1400R	1600R	
Non-repetitive peak voltages ($t \leqslant 10$ ms)	V_{DSM}/V_{RSM}	max. 800	1000	1200	1400	1600	V
Repetitive peak voltages	V_{DRM}/V_{RRM}	max. 800	1000	1200	1400	1600	V
Crest working voltages	V_{DWM}/V_{RWM}	max. 600	700	800	800	800	V*

Average on-state current (averaged over any 20 ms period) up to T_{mb} = 77 °C	$I_{T(AV)}$	max.	16	A
at T_{mb} = 85 °C	$I_{T(AV)}$	max.	14	A
R.M.S. on-state current	$I_{T(RMS)}$	max.	25	A
Repetitive peak on-state current	I_{TRM}	max.	150	A
Non-repetitive peak on-state current; t = 10 ms; half sine-wave; T_j = 125 °C prior to surge; with reapplied V_{RWMmax}	I_{TSM}	max.	300	A
I^2t for fusing (t = 10 ms)	I^2t	max.	450	A^2s
Rate of rise of on-state current after triggering with I_G = 500 mA to I_T = 50 A	dI_T/dt	max.	200	A/μs
Rate of change of commutation current	see Fig. 9			

Gate to cathode

Reverse peak voltage	V_{RGM}	max.	10	V
Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	1	W
Peak power dissipation	P_{GM}	max.	5	W

Temperatures

Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1	°C/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,2	°C/W
Transient thermal impedance (t = 1 ms)	$Z_{th\ j\text{-}mb}$	=	0,06	°C/W

* To ensure thermal stability: $R_{th\ j\text{-}a} < 1{,}5$ °C/W (d.c. blocking) or < 3 °C/W (a.c.). For smaller heatsinks $T_{j\ max}$ should be derated. For a.c. see Fig. 3.

CHARACTERISTICS

Anode to cathode

On-state voltage I_T = 50 A; T_j = 25 °C	V_T	<	3 V*
Rate of rise of off-state voltage that will not trigger any device; exponential method; V_D = 2/3 V_{DRMmax}; T_j = 125 °C	dV_D/dt	<	300 V/μs
Reverse current V_R = V_{RWMmax}; T_j = 125 °C	I_R	<	5 mA
Off-state current V_D = V_{DWMmax}; T_j = 125 °C	I_D	<	5 mA
Latching current; T_j = 25 °C	I_L	<	200 mA
Holding current; T_j = 25 °C	I_H	<	200 mA

Gate to cathode

Voltage that will trigger all devices V_D = 6 V; T_j = 25 °C	V_{GT}	>	3,5 V
Voltage that will not trigger any device V_D = V_{DRMmax}; T_j = 125 °C	V_{GD}	<	200 mV
Current that will trigger all devices V_D = 6 V; T_j = 25 °C	I_{GT}	>	100 mA

Switching characteristics

Gate-controlled turn-on time (t_{gt} = t_d + t_r) when switched from V_D = V_{DWMmax} to I_T = 10 A; I_{GT} = 150 mA; dI_G/dt = 1 A/μs; T_j = 25 °C	t_{gt} t_r	typ. typ.	2 μs 1,2 μs

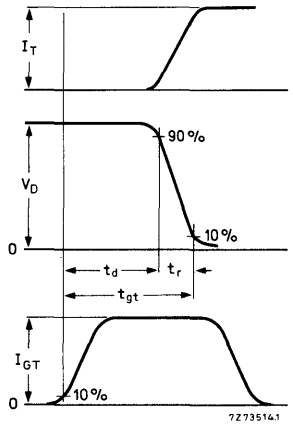


Fig. 2 Gate-controlled turn-on time definitions.

* Measured under pulse conditions to avoid excessive dissipation.

OPERATING NOTES

1. The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.
   During soldering the heat conduction to the junction should be kept to a minimum.
2. Switching losses in commutation

   For applications in which the thyristor is forced to switch from an on-state current I_{TRM} to a high reverse voltage at a high commutation rate ($-dI_T/dt$), consult Fig. 9 (nomogram) to find the increase in total average power. This increase must be added to the loss from the curves in Fig. 3.

ORDERING NOTE

Types with dV_D/dt of 1000 V/μs are available on request. Add suffix C to the type number when ordering; e.g. BTW47-800RC.

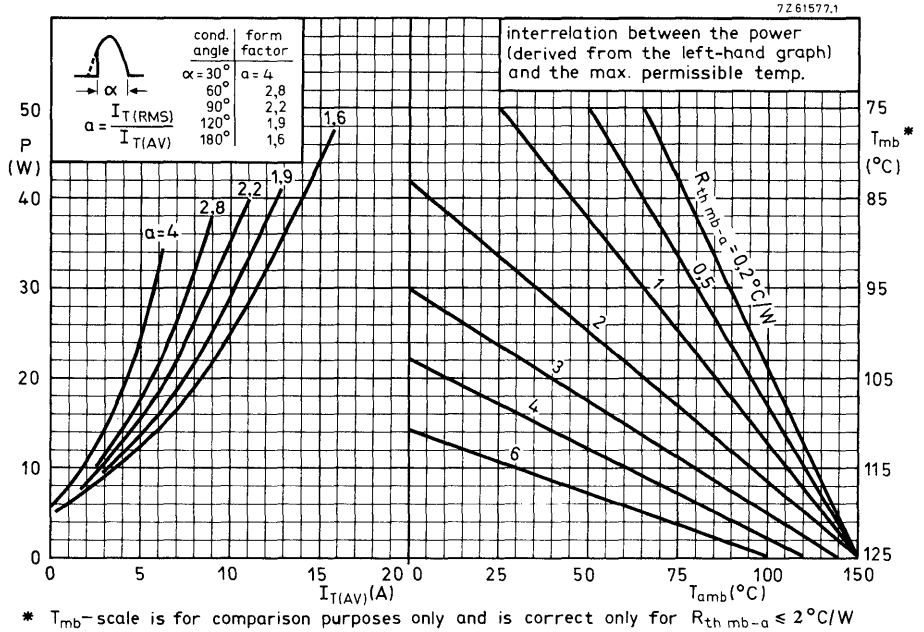


Fig. 3.

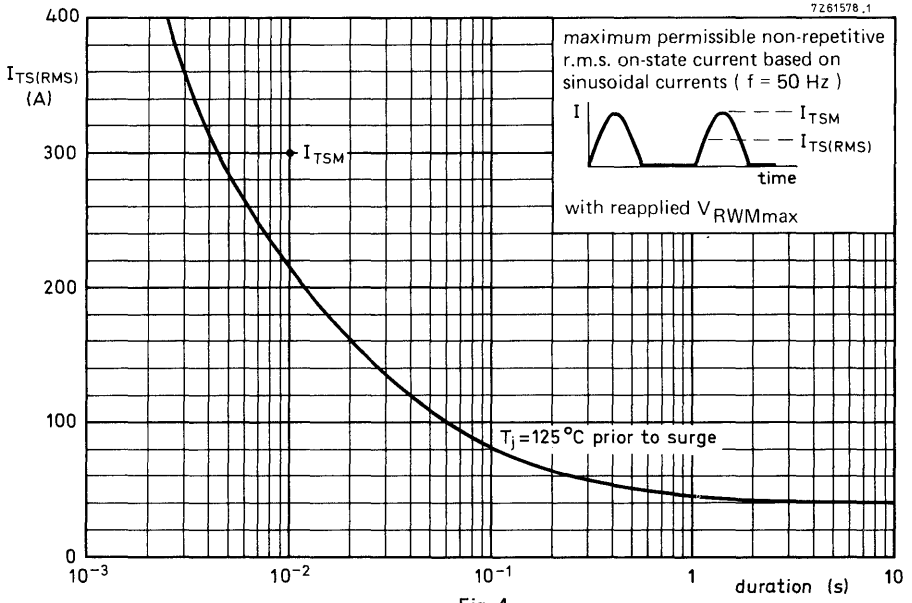


Fig. 4.

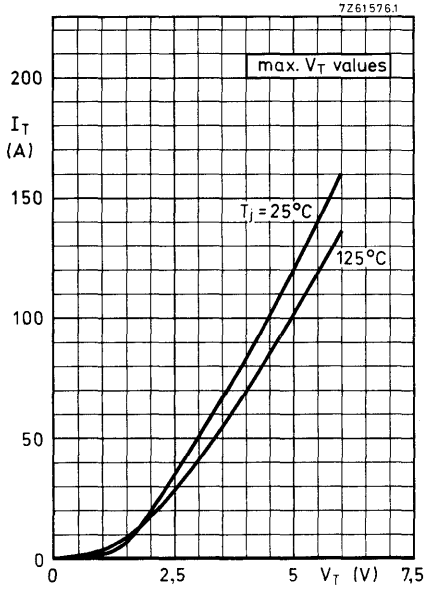


Fig. 5.

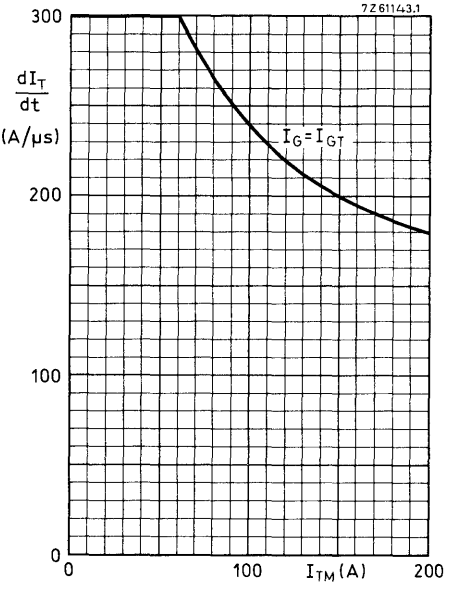


Fig. 6.

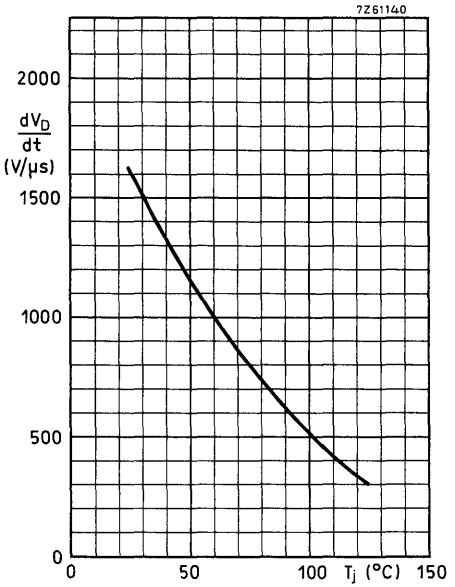


Fig. 7 Maximum rate of rise of off-state voltage that with not trigger any device (exponential method) as a function of T_j.

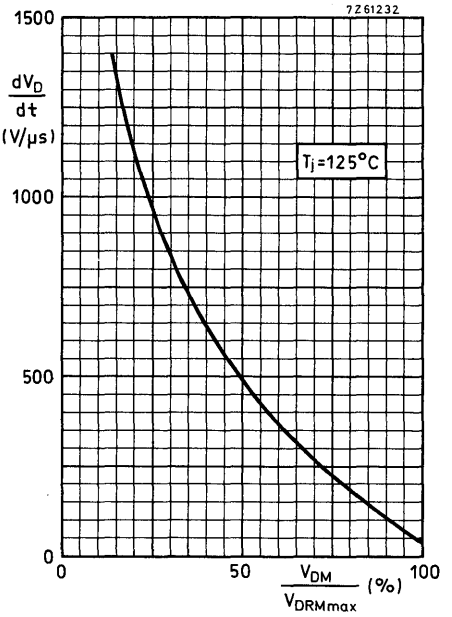


Fig. 8 Maximum rate of rise of off-state voltage that with not trigger any device (exponential method) as a function of applied voltage.

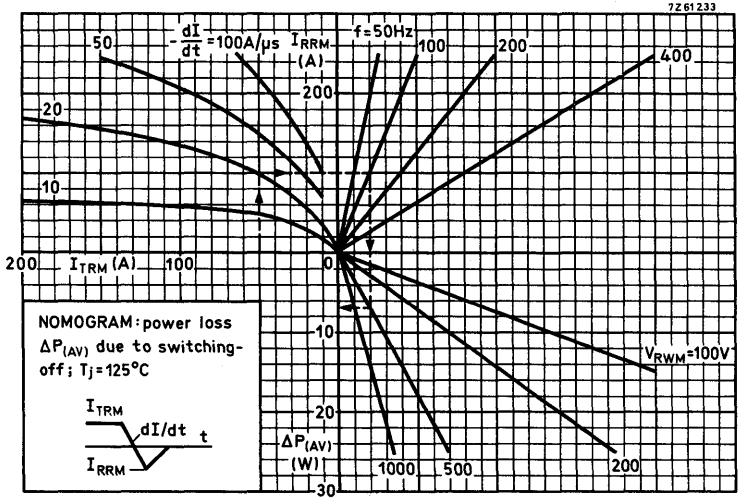


Fig. 9.

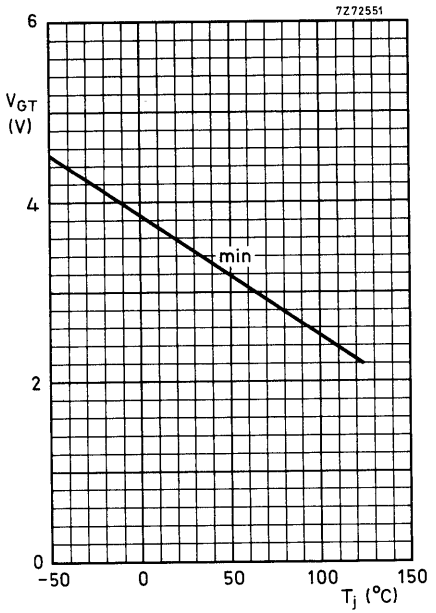


Fig. 10 Minimum gate voltage that will trigger all devices as a function of T_j.

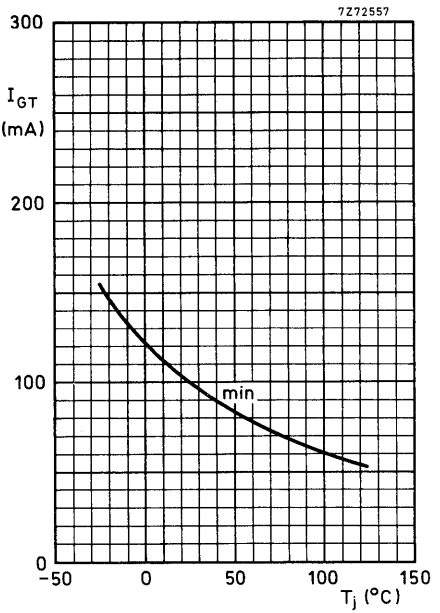


Fig. 11 Minimum gate current that will trigger all devices as a function of T_j.

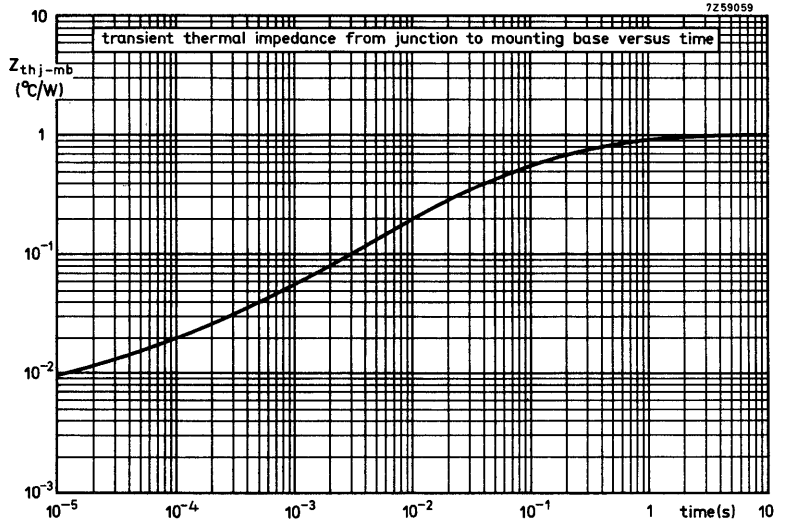
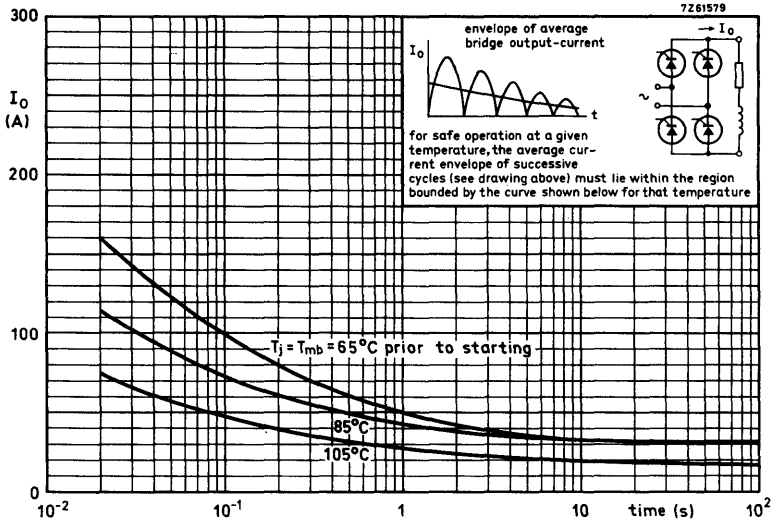


Fig. 12.



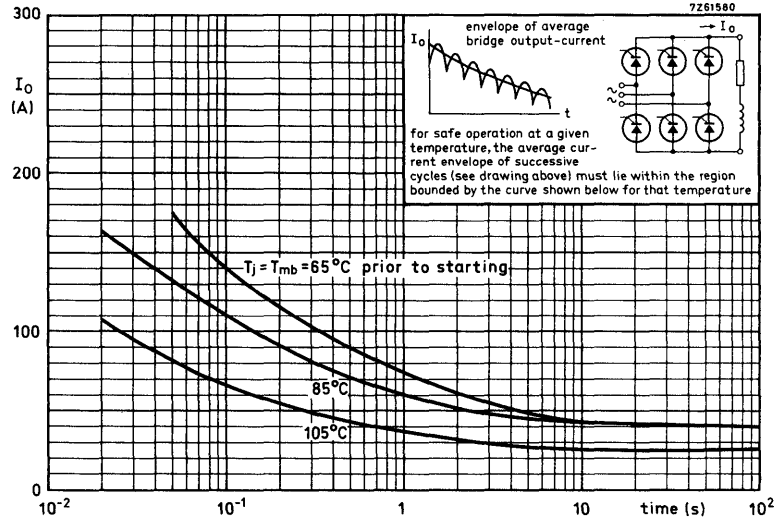


Fig. 13 Limits for starting or inrush currents.