THYRISTORS

Silicon thyristors in metal envelopes, intended for power control and power switching applications. The series consists of reverse polarity types (anode to stud) identified by a suffix R: BTY91-400R to 800R.

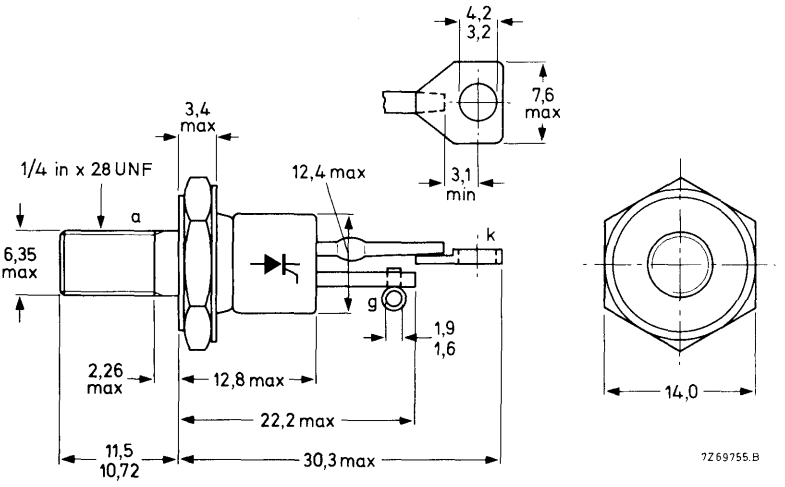
QUICK REFERENCE DATA

		BTY91-	400R	500R	600R	800R	
Repetitive peak voltages	V_{DRM}/V_{RRM}	max.	400	500	600	800	V
Average on-state current	$I_{T(AV)}$	max.		16			A
R.M.S. on-state current	$I_{T(RMS)}$	max.		25			A
Non-repetitive peak on-state current	I_{TSM}	max.		200			A

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-48: with ¼ in x 28 UNF stud (ϕ 6,35 mm).



Net mass: 14 g
Diameter of clearance hole: max. 6,5 mm
Accessories supplied on request: 56264A
(mica washer, insulating ring, soldering tag)

Torque on nut: min. 1,7 Nm (17 kg cm)
max. 3,5 Nm (35 kg cm)
Supplied with the device:
1 nut, 1 lock washer
Nut dimensions across the flats: 11,1 mm

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BTY91-400R	500R	600R	800R	
Anode to cathode							
Non-repetitive peak off-state voltage ($t \leqslant 10$ ms)	V_{DSM}	max.	500	850	850	850	V
Non-repetitive peak reverse voltage ($t \leqslant 5$ ms)	V_{RSM}	max.	500	600	720	960	V
Repetitive peak voltages	V_{DRM}/V_{RRM}	max.	400	500	600	800	V
Crest working voltages	V_{DWM}/V_{RWM}	max.	400	500	600	800	V *

Average on-state current (averaged over any 20 ms period) up to $T_{mb} = 77$ °C	$I_{T(AV)}$	max.	16	A
at $T_{mb} = 85$ °C	$I_{T(AV)}$	max.	14	A
R.M.S. on-state current	$I_{T(RMS)}$	max.	25	A
Repetitive peak on-state current	I_{TRM}	max.	200	A
Non-repetitive peak on-state current; t = 10 ms; half sine-wave; $T_j = 125$ °C prior to surge; with reapplied V_{RWMmax}	I_{TSM}	max.	200	A
I^2t for fusing (t = 10 ms)	I^2t	max.	200	A^2s
Rate of rise of on-state current after triggering with $I_G = 200$ mA to $I_T = 50$ A	dI_T/dt	max.	20	A/μs
Gate to cathode				
Reverse peak voltage	V_{RGM}	max.	5	V
Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	0,5	W
Peak power dissipation	P_{GM}	max.	5	W
Temperatures				
Storage temperature	T_{stg}		−55 to + 125	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1,6	°C/W
From mounting base to heatsink with heatsink compound	$R_{th\ mb\text{-}h}$	=	0,2	°C/W
Transient thermal impedance (t = 1 ms)	$Z_{th\ j\text{-}mb}$	=	0,09	°C/W

OPERATING NOTE

The terminals should neither be bent nor twisted; they should be soldered into the circuit so that there is no strain on them.
During soldering the heat conduction to the junction should be kept to a minimum.

* To ensure thermal stability: $R_{th\ j\text{-}a} < 4{,}5$ °C/W (d.c. blocking) or < 9 °C/W (a.c.). For smaller heatsinks $T_{j\ max}$ should be derated. For a.c. see Fig. 3.

CHARACTERISTICS

Anode to cathode

On-state voltage I_T = 50 A; T_j = 25 °C	V_T	<	2 V *
Rate of rise of off-state voltage that will not trigger any device; exponential method; V_D = 2/3 V_{DRMmax}; T_j = 125 °C	dV_D/dt	<	20 V/μs
Reverse current V_R = V_{RWMmax}; T_j = 125 °C	I_R	<	3 mA
Off-state current V_D = V_{DWMmax}; T_j = 125 °C	I_D	<	3 mA
Latching current; T_j = 25 °C	I_L	typ.	20 mA
Holding current; T_j = 25 °C	I_H	typ.	10 mA

Gate to cathode

Voltage that will trigger all devices V_D = 6 V; T_j = 25 °C	V_{GT}	>	3 V
Voltage that will not trigger any device V_D = V_{DRMmax}; T_j = 125 °C	V_{GD}	<	200 mV
Current that will trigger all devices V_D = 6 V; T_j = 25 °C	I_{GT}	>	40 mA

Switching characteristics

Gate-controlled turn-on time (t_{gt} = t_d + t_r) when switched from V_D = 400 V to I_T = 10 A; I_{GT} = 200 mA; T_j = 25 °C	t_{gt}	typ.	2 μs

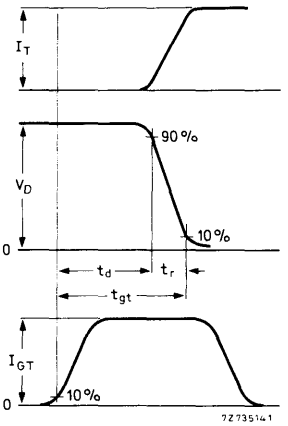


Fig. 2 Gate-controlled turn-on time definitions.

* Measured under pulse conditions to avoid excessive dissipation.

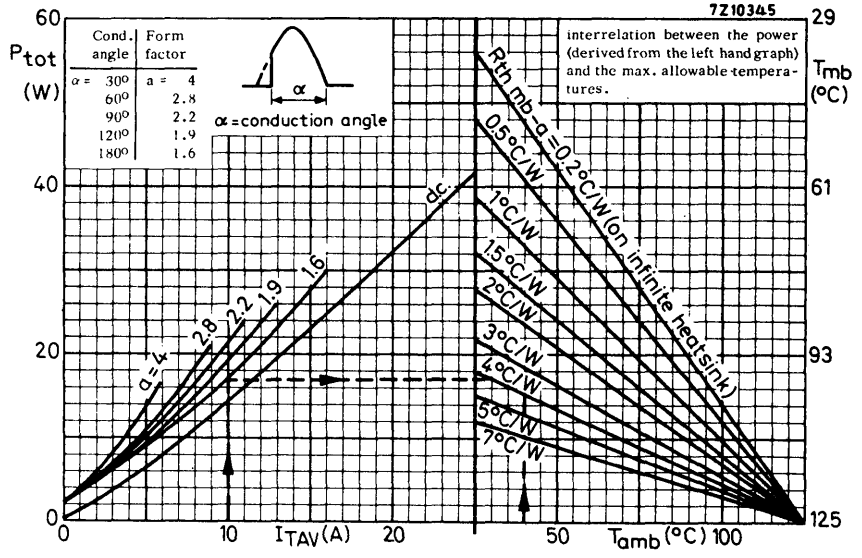

7Z10345
Cond. angle | Form factor
α = 30° | a = 4
60° | 2.8
90° | 2.2
120° | 1.9
180° | 1.6
α = conduction angle
interrelation between the power (derived from the left hand graph) and the max. allowable temperatures.
Ptot (W)
Tmb (°C)
Rth mb-a = 0.2°C/W (on infinite heatsink)
0.5°C/W
1°C/W
1.5°C/W
2°C/W
3°C/W
4°C/W
5°C/W
7°C/W
d.c.
a = 4
2.8
2.2
1.9
1.6
ITAV (A)
Tamb (°C)
60
40
20
0
29
61
93
125
0
10
20
50
100

Fig. 3.

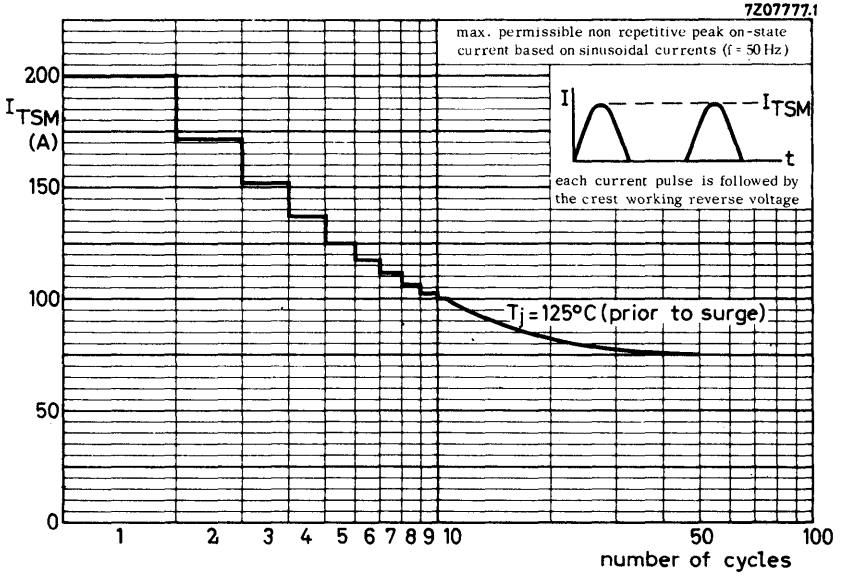

7Z07777.1
max. permissible non repetitive peak on-state current based on sinusoidal currents (f = 50 Hz)
each current pulse is followed by the crest working reverse voltage
ITSM (A)
Tj = 125°C (prior to surge)
number of cycles
200
150
100
50
0
1
2
3
4
5
6
7
8
9
10
50
100

Fig. 4.

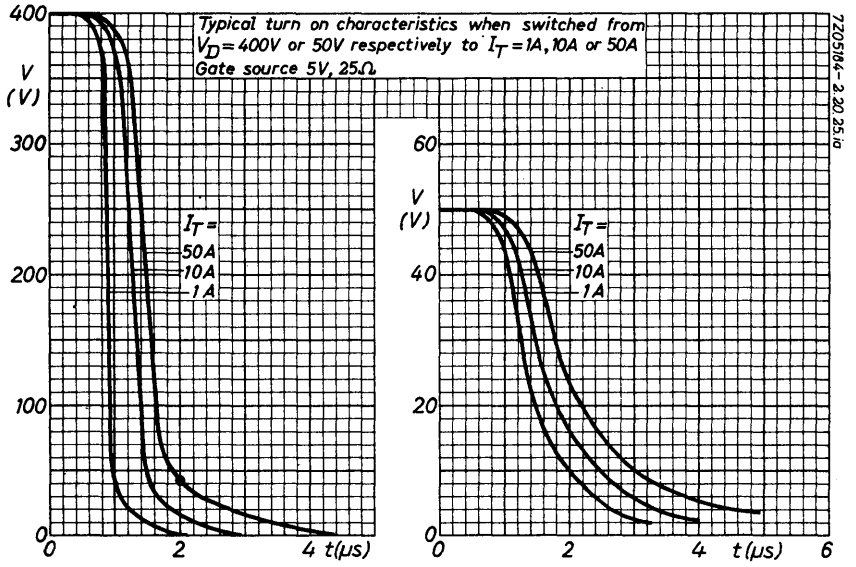

Typical turn on characteristics when switched from
V_D=400V or 50V respectively to I_T=1A, 10A or 50A
Gate source 5V, 25Ω
400
V
(V)
300
200
100
0
0
2
4 t(μs)
I_T =
50A
10A
1A
60
V
(V)
40
20
0
0
2
4
t(μs)
6
I_T =
50A
10A
1A
7Z05104-2.20.25.10

Fig. 5.

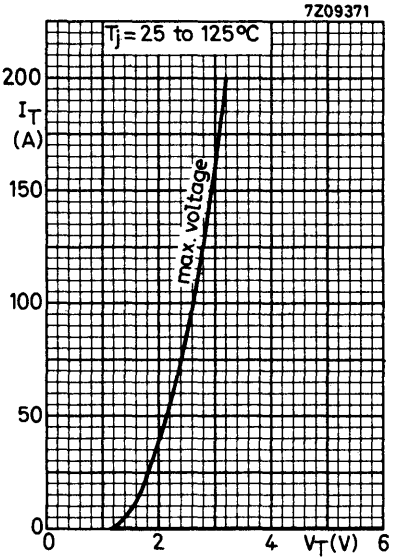

7Z09371
Tj=25 to 125°C
200
I_T
(A)
150
100
50
0
max. voltage
0
2
4
V_T(V)
6

Fig. 6.

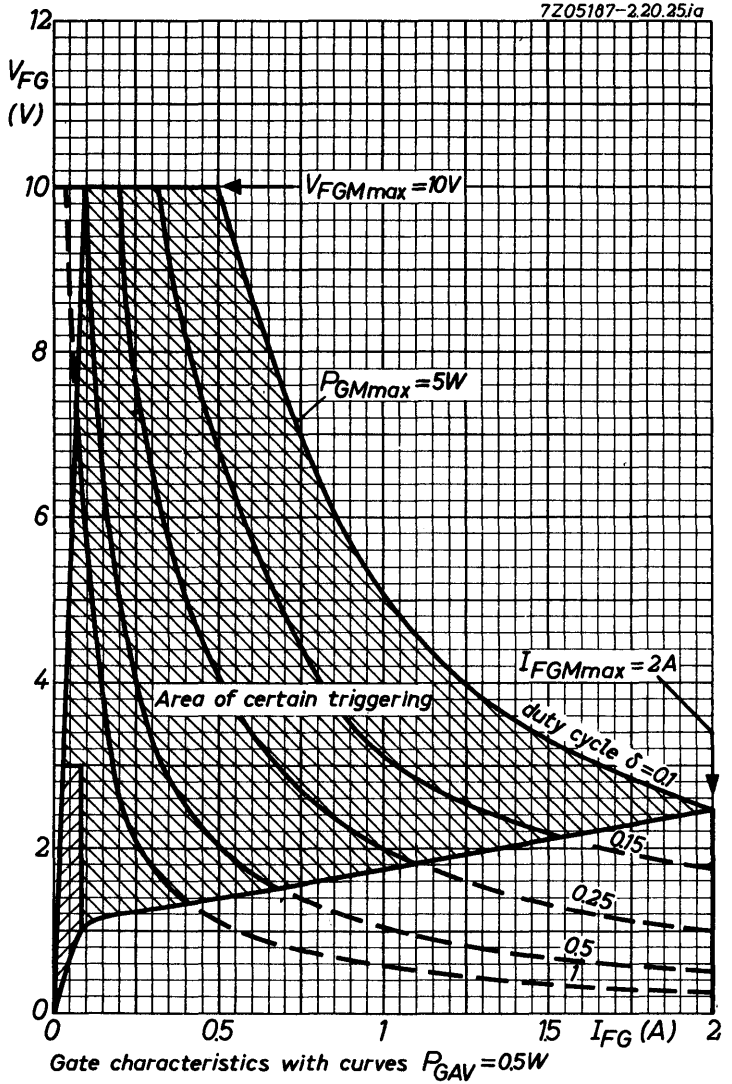

7Z05187-2.20.25.ia
12
V_{FG} (V)
10
8
6
4
2
0
V_{FGMmax} = 10V
P_{GMmax} = 5W
I_{FGMmax} = 2A
Area of certain triggering
duty cycle δ = 0.1
0.15
0.25
0.5
1
0
0.5
1
1.5
I_{FG} (A)
2
Gate characteristics with curves P_{GAV} = 0.5W

Fig. 7.

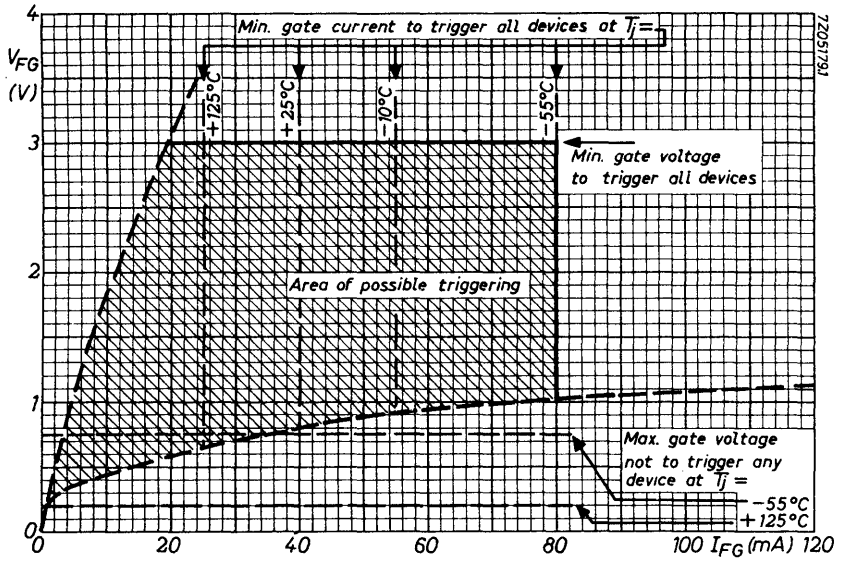

7Z05179J
Min. gate current to trigger all devices at Tj =
+125°C
+25°C
-10°C
-55°C
Min. gate voltage to trigger all devices
Area of possible triggering
Max. gate voltage not to trigger any device at Tj =
-55°C
+125°C
VFG (V)
IFG (mA)
0
20
40
60
80
100
120
1
2
3
4

Fig. 8.

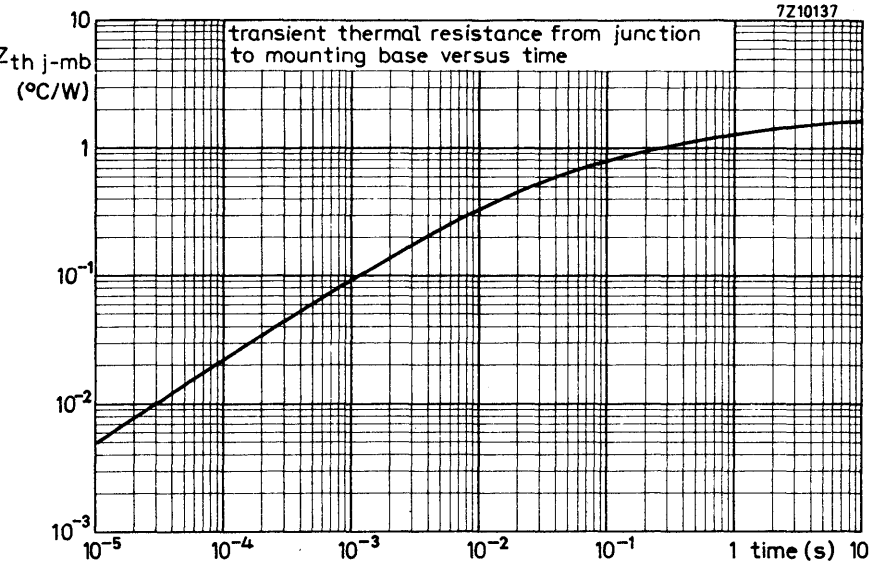
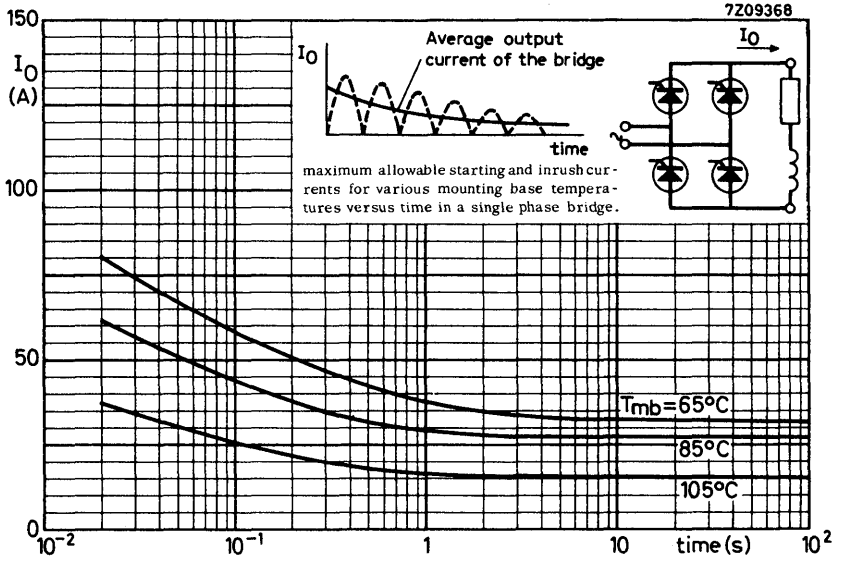
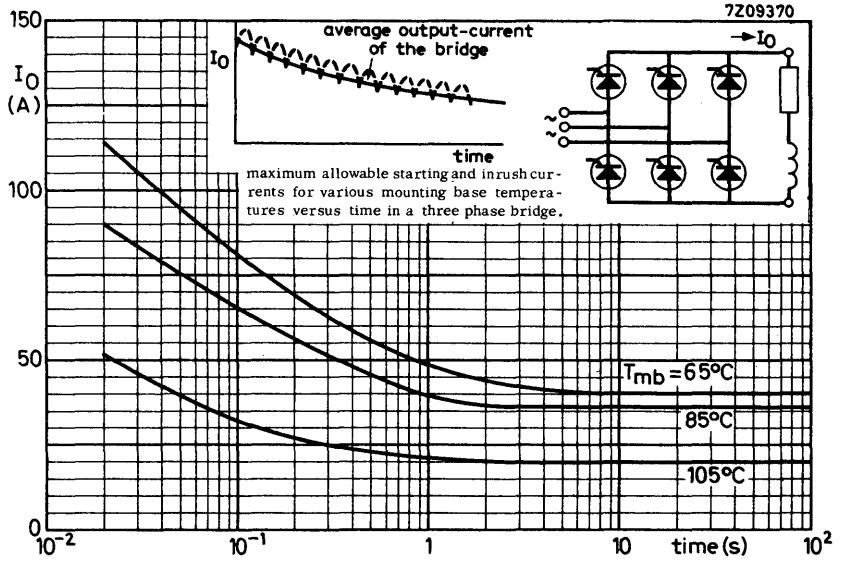

7Z10137
transient thermal resistance from junction to mounting base versus time
Zth j-mb (°C/W)
10
1
10-1
10-2
10-3
10-5
10-4
10-3
10-2
10-1
1
10
time (s)

Fig. 9.



maximum allowable starting and inrush currents for various mounting base temperatures versus time in a single phase bridge.

Fig. 10.



maximum allowable starting and inrush currents for various mounting base temperatures versus time in a three phase bridge.

Fig. 11.