

Structure Silicon monolithic integrated circuit

Product Name System LSI for Event data recorder

Type **BU1511KV2**

Function BU1511KV2 is a system LSI for event data recorder that makes developing it easier
BU1511KV2 have built-in specific hardware to communicate and control with a 3-axis accelerometer and a camera module, SD card, etc. that are recommended for event data recorder.

The specific hardware are controllerable by built-in ARM946E-S, which can execute various applications.

The following function blocks are built-in.

- ARM946E-S
- External Memory Interface
- GPIO(16ch, PWM 4ch(shared), IRQ 4ch(shared))
- SD Card Interface/SD Card Controller
- SSI(Synchronous Serial Interface)
- Watch Dog Timer
- ADPCM Audio Codec with IIS Interface
- TV Encoder(within 75Ω driver)
- Interrupt Controller
- Timer/Timer Counter
- UART(2ch)
- I2C Master Controller
- Camera Interface (up to 2M pixels)
- JPEG Codec
- Clock Controller/PLL
- A/D Converter(4ch)

○ Absolute maximum ratings

Parameter	Symbol	Rating	Unit	Parameter	Symbol	Rating	Unit
Power supply voltage 1 (DAC)	DAVDD	-0.3~+4.2	V	Input voltage (ADC)	VIN1	-0.3~ADVDD+0.3	V
Power supply voltage 2 (ADC)	ADVDD	-0.3~+4.2	V	Input voltage (I2C-1)	VIN2	-0.3~I1VDD+0.3	V
Power supply voltage 3 (I2C-1)	I1VDD	-0.3~+4.2	V	Input voltage (I2C-2)	VIN3	-0.3~I2VDD+0.3	V
Power supply voltage 4 (I2C-2)	I2VDD	-0.3~+4.2	V	Input voltage (SD-CARD)	VIN4	-0.3~SDVDD+0.3	V
Power supply voltage 5 (SD-CARD)	SDVDD	-0.3~+4.2	V	Input voltage (CAMERA)	VIN5	-0.3~CAVDD+0.3	V
Power supply voltage 6(CAMERA)	CAVDD	-0.3~+4.2	V	Input voltage (Other IO)	VIN6	-0.3~IOVDD+0.3	V
Power supply voltage 7(Other IO)	IOVDD	-0.3~+4.2	V	Storage temperature range	Tstg	-40~+150	°C
Power supply voltage 8(Digital CORE)	DVDD	-0.3~+2.1	V	Power dissipation	PD	1200*1, 1700*2	mW

*1 IC only. In the case of exceeding 25°C, 12.0 mW should be reduced at the rating 1°C.

*2 When packaging a glass epoxy board of 270x70x1.6mm. If exceeding 25°C, 17mW should be reduced at the rating 1°C.

* Has not been designed to withstand radiation.

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○ Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage 1 (DAC)	DAVDD	3.00	3.30	3.60	V
Power supply voltage 2 (ADC)	ADVDD	3.00	3.30	3.60	V
Power supply voltage 3 (I2C-1)	I1VDD	2.40	3.30	3.60	V
Power supply voltage 4 (I2C-2)	I2VDD	2.40	3.30	3.60	V
Power supply voltage 5 (SD-CARD)	SDVDD	2.70	3.30	3.60	V
Power supply voltage 6 (CAMERA)	CAVDD	2.30	2.85	3.30	V
Power supply voltage 7 (Other IO)	IOVDD	1.70	3.30	3.60	V
Power supply voltage 8 (Digital CORE)	DVDD	1.45	1.50	1.55	V

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage range (ADC)	VIN1	-0.3	-	ADVDD +0.3	V
Input voltage range (I2C-1)	VIN2	-0.3	-	I1VDD +0.3	V
Input voltage range (I2C-2)	VIN3	-0.3	-	I2VDD +0.3	V
Input voltage range (SD-CARD)	VIN4	-0.3	-	SDI1 VDD+0.3	V
Input voltage range (CAMERA)	VIN5	-0.3	-	CAVDD +0.3	V
Input voltage range (Other IO)	VIN6	-0.3	-	IOVDD +0.3	V
Output "H" Current *1	IOH	-13	-	-	mA
Output "L" Current *1	IOL	-	-	13	mA
Operating temperature range	Topr	-40	-	85	°C

*1 Sum of absolute current of IOs in IOVDD system must be less than 100mA, and every sum of absolute current of IOs in CAVDD, SDVDD, I1VDD and I2VDD system must be less than 26mA.

* Please supply power source in order of CORE(DVDD) → IO (IOVDD,CAVDD,SDVDD,I1VDD,I2VDD,ADVDD,DAVDD)

* Please keep RESETB terminal is LOW, until power supply is stable.

○ Electric characteristics

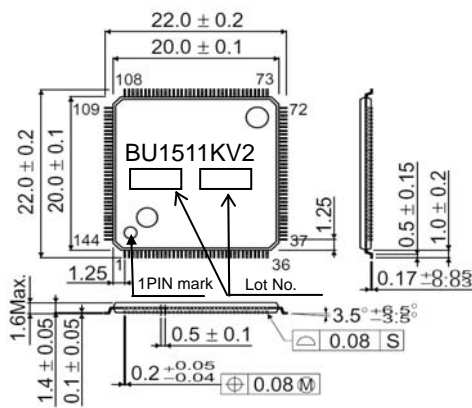
(Unless otherwise specified, DVDD=1.50V, DAVDD=ADVDD=I1VDD=I2VDD=SDVDD=IOVDD=3.30V, CAVDD=2.85V, DAVSS=ADVSS=DVSS=0.0V, Ta=25°C, fXIN=13.5MHz, fAXIN=16.384MHz, fSYS=41.0MHz(Internal Clock with PLL) IOPWR is a generic name of I1VDD,I2VDD,SDVDD,CAVDD,IOVDD.)

Parameter	Symbol	Specification		Unit	Conditions
		Min	Max		
Common					
Input frequency 1	fXIN	5.0	30.0	MHz	XIN (Duty 50±10%), When PLL is ON.
Input frequency 2	fAXIN	8.284	32.768	MHz	AXIN(Duty 50±10%)
Internal clock frequency 1	fSYS	-	41.0	MHz	When PLL is ON, Except I2S Audio Block
Internal clock frequency 2	f AUD	-	32.768	MHz	I2S Audio Block
Static consumption current	IDDST	-	200	µA	When all clock stop
Logic Block					
Input "H" Leakage current	IIHL	-10	10	µA	VIH=IOPWR
Input "L" Leak current	IIHL	-10	10	µA	VIL=0V
Input Pull down "H" current 1	IIHPD1	25	100	µA	Pull down pin, VIH=IOVDD
Input Pull down "H" current 2	IIHPD2	25	100	µA	Pull down pin, VIH=CAVDD
Input Pull down "L" current	IILPD	-10	10	µA	Pull down pin, VIL=0V
Input "H" voltage 1	VIH1	IOPWR × 0.8	IOPWR+0.3	V	Normal Input
Input "L" voltage 1	VIL1	-0.3	IOPWR × 0.2	V	Normal Input
Input "H" voltage 2	VIH2	IOPWR × 0.85	IOPWR+0.3	V	Hysteresis input pin
Input "L" voltage 12	VIL2	-0.3	IOPWR × 0.15	V	(TIM_TRIG,NTRST,RESETB,BIT_SEL,TCM_SEL,AUTO_READ)
Output "H" voltage 1	VOH1	IOPWR-0.4	IOPWR	V	IOH=-2.0mA(DC), Output except SD_CLK, When CAVDD=3.3V
Output "L" voltage 1	VOL1	0.0	0.4	V	IOL=2.0mA(DC), Output except SD_CLK, When CAVDD=3.3V.
Output "H" voltage 2	VOH2	IOPWR-0.4	IOPWR	V	IOH=-4.0mA(DC), SD_CLK
Output "L" voltage 2	VOL2	0.0	0.4	V	IOL=4.0mA(DC), SD_CLK
DACBlock					
DAC Bit Width	RES_DA	-	10	bits	
DAC Operating current	IDDDA	32	42	mA	RL=37.5Ω, RREF=2.4kΩ, DAVDD Pin current
DAC Static consumption current	IDDSTDA	-	5	µA	RL=37.5Ω, RREF=2.4kΩ, DAVDD Pin current
Integral Non-linearity	INL_DA	-8.0	+8.0	LSB	RL=37.5Ω, RREF=2.4kΩ
Differential Non-linearity	DNL_DA	-2.0	+2.0	LSB	RL=37.5Ω, RREF=2.4kΩ
Full scale voltage	VFS_DA	1.1	1.4	V	RL=37.5Ω, RREF=2.4kΩ
ADCBlock					
ADC Bit Width	RES_AD	-	8	bits	
Input voltage range(Upper Limit)	VIN_AD_T	ADVDD × 0.85	ADVDD × 0.95	V	
Input voltage range(Lower Limit)	VIN_AD_B	ADVDD × 0.05	ADVDD × 0.15	V	
Integral Non-linearity	INL_AD	-2.0	+2.0	LSB	
Differential Non-linearity	DNL_AD	-2.0	+2.0	LSB	
Change Standard clock cycle	f ADC	4.0	16.0	MHz	
Change cycle	fsps	30.8K	123K	sps	Sample per second Need 130°ADC_CLK for conversion by sweeping

○ Pin Function Descriptions

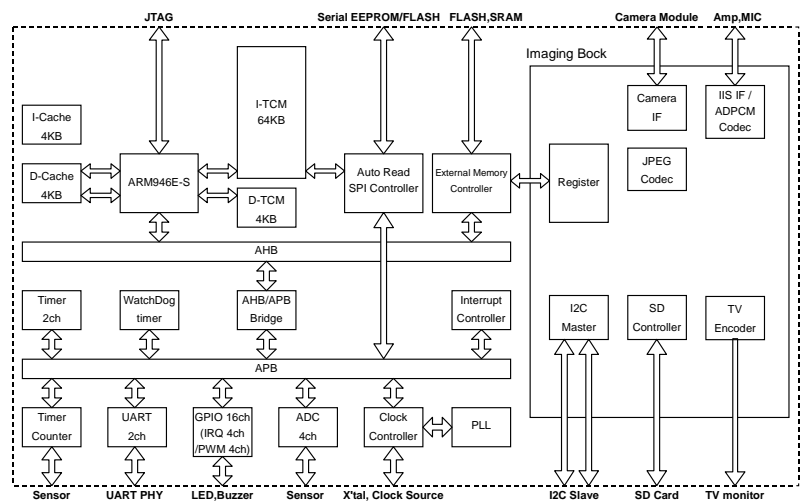
PIN No.	Pin Name	Function	PIN No.	Pin Name	Function	PIN No.	Pin Name	Function	
1	EXT_ADR20	External Bus	49	SSI_CSB0	Serial	97	TCM_SEL	System setting	
2	EXT_ADR19		50	SSI_WPB		98	AUTO_READ		
3	EXT_ADR18		51	SSI_DOUT		99	ADVDD	--	
4	EXT_ADR17		52	SSI_DIN	100	ADVSS	--		
5	EXT_ADR16		53	DVDD	101	ADIN3	ADC input		
6	EXT_ADR15		54	TIM_TRIG	102	ADIN2			
7	EXT_ADR14		55	GPIO15	103	ADIN1			
8	EXT_ADR13		56	GPIO14	104	ADIN0	Video output (75Ω)		
9	EXT_ADR12		57	GPIO13	105	VOUT			
10	EXT_ADR11		58	GPIO12	106	DAVSS		--	
11	EXT_ADR10		59	GPIO11	107	IREF	Video output Reference		
12	EXT_ADR9		60	GPIO10	108	DAVDD	--		
13	EXT_ADR8		61	GPIO9	109	I1VDD	--		
14	EXT_ADR7		62	GPIO8	110	DVSS	--		
15	EXT_ADR6		63	GPIO7	111	SDC1	I2C Master Interface		
16	EXT_ADR5		64	GPIO6	112	SDA1			
17	IOVDD		--	65	GPIO5	113		SDC2	
18	DVSS	--	66	GPIO4	114	SDA2	Camera Interface		
19	EXT_ADR4	External Bus	67	IOVDD	--	115		I2VDD	--
20	EXT_ADR3		68	DVSS	--	116		CAMCKO	
21	EXT_ADR2		69	GPIO3	117	CAVDD	--		
22	EXT_ADR1		70	GPIO2	118	CAMHS	Camera Interface		
23	EXT_DATA15		71	GPIO1	119	CAMVS			
24	EXT_DATA14		72	GPIO0	120	CAMD7			
25	EXT_DATA13		73	TX1	121	CAMD6			
26	EXT_DATA12	74	RX1	122	CAMD5				
27	IOVDD	--	75	RTS1	123	CAMD4	Camera Interface		
28	DVSS	--	76	CTS1	124	DVDD		--	
29	EXT_DATA11	External Bus	77	TX2	125	CAMD3			
30	EXT_DATA10		78	RX2	126	CAMD2			
31	EXT_DATA9		79	TDL	127	CAMD1			
32	EXT_DATA8		80	TDO	128	CAMD0			
33	EXT_DATA7		81	TCK	129	CAMCKI	SD card Interface		
34	EXT_DATA6		82	TMS	130	SD_CLK			
35	EXT_DATA5		83	NTRST	131	SD_CMD			
36	EXT_DATA4	84	AUDCKI	132	SD_DAT3				
37	EXT_DATA3	85	AUDLRI	133	SD_DAT2				
38	EXT_DATA2	86	AUDDTI	134	SD_DAT1				
39	EXT_DATA1	87	AUDCKO	135	SD_DAT0	--			
40	EXT_DATA0	88	AUDLRO	136	SDVDD	--			
41	EXT_CSB2	89	AUDDTO	137	DVSS	--			
42	EXT_CSB1	90	AUDMCKO	138	AXIN	Clock input or X'tal			
43	EXT_CSB0	91	IOVDD	139	AXOUT	Clock input or X'tal			
44	EXT_WEB	92	DVSS	140	IOVDD	--			
45	EXT_OEB	93	DVDD	141	XIN	Clock input or X'tal			
46	EXT_WPB	94	RESETB	142	XOUT	Clock input or X'tal			
47	SSI_CLK	95	TEST	143	DVSS	--			
48	SSI_CSB1	Serial	96	BIT_SEL	144	EXT_ADR21	External Bus		

○ Physical dimensions



VQFP-T144 (Unit:mm)

○ Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.

In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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