AD Converter Series

Successive Approximation A/D Converter 12bit, 0.5M to 1MSPS, 2.7 to 5.25V, 1-channel, SPI™ Interface

BU1S12S1AG-LB

General Description

This is the product guarantees long time support in Industrial market.

The BU1S12S1AG-LB is a general purpose, 12-bit 1-channel successive approximation AD converter. The sampling rate of BU1S12S1AG-LB ranges from 0.5MSPS to 1MSPS.

Features

- Long Time Support Product for Industrial Applications
- Maximum 1MSPS Sampling Rate
- Low Power Consumption
- Small SSOP6 Package Compatible with SOT23-6
- Serial Interface Compatible with SPI™/QSPI™/MICROWIRE™
- Operational Supply Voltage Range: 2.7V to 5.25V
- Single-ended Input
- Output Code in Straight Binary Format

Applications

- Industrial Equipment
- Instrumentation and Control Systems
- Motor Control Systems
- Data Acquisition Systems

Key Specifications

- Supply Voltage Range: 2.7V to 5.25V
- Sampling Rate: 0.5MSPS to 1MSPS
- Power Consumption
  In 1MSPS Operation: 8mW @V_A=5V (Typ)
  1.5mW @V_A=3V (Typ)
- INL: -1.1 to +1.0 LSB
- DNL: -0.9 to +1.0 LSB
- SNR: 71.5dB @ V_A=3V (Typ)
- SINAD: 71dB @ V_A=3V (Typ)
- Operational Temperature Range: -40°C to +105°C

Package

	W(Typ) x D(Typ) x H(Max)
SSOP6	2.90mm x 2.80mm x 1.25mm

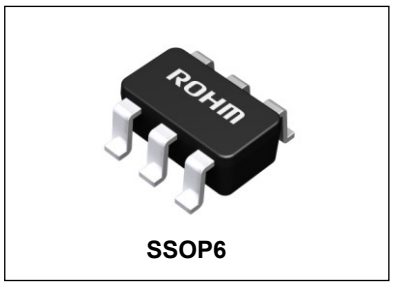


Figure 1. Package Outline

Typical Application Circuit

Figure 2 shows a typical application circuit of BU1S12S1AG-LB.

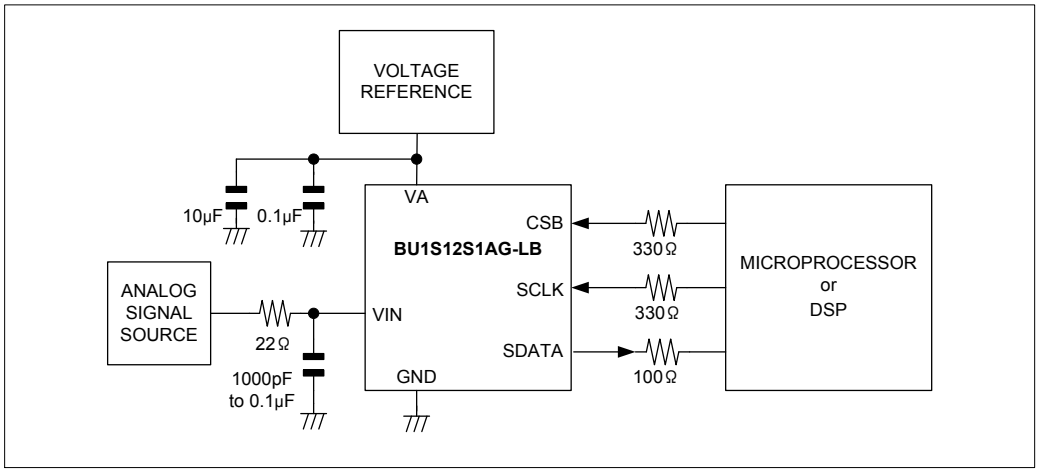


Figure 2. Typical Application Circuit

Pin Configuration

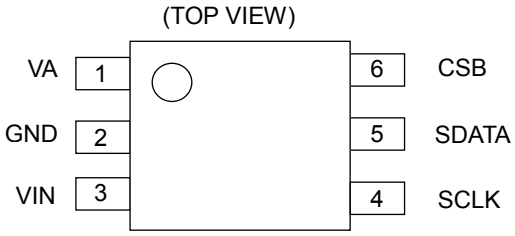


Figure 3. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Description
1	VA	Power supply pin. This voltage is the full scale of the analog input.
2	GND	Ground pin. This voltage level is the zero scale of the analog input.
3	VIN	Analog input pin. The voltage range must be between 0V and $V_{A.}$
4	SCLK	Digital clock input pin.
5	SDATA	Digital data output pin.
6	CSB	Chip select pin. A/D conversion starts at the falling edge of this signal.

Block Diagram

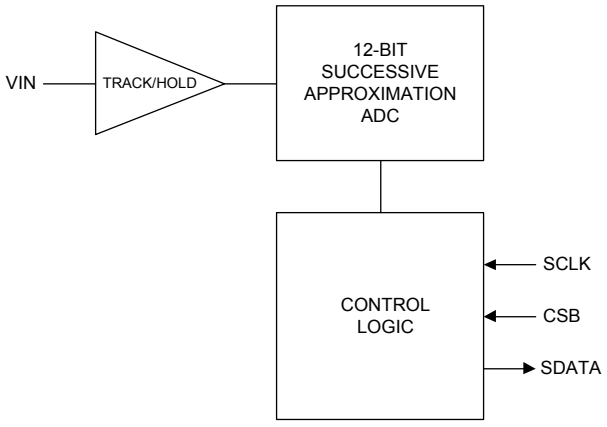


Figure 4. Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_A	5.7	V
Analog Input Voltage	V_{IN}	-0.3 to V_A +0.3	V
Digital Input Voltage	V_{DIN}	-0.3 to 5.7	V
Power Dissipation	P_D	0.54(Note1)	W
Junction Temperature	T_{Jmax}	125	°C
Storage Temperature	T_{stg}	-55 to +125	°C

(Note 1) Derate by 5.4mW/°C when operating above Ta=25°C. (when mounted on a 70mm×70mm×1.6mm, 1-layer, glass-epoxy board.)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operational Conditions

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_A	2.7 to 5.25	V
Analog Input Voltage	V_{IN}	0 to V_A	V
Digital Input Voltage	V_{DIN}	0 to 5.25	V
Operational Temperature	T_{opr}	-40 to +105	°C
Clock Frequency	f_{SCLK}	10 to 20	MHz
Sampling Rate	f_S	0.5 to 1	MSPS

Electrical Characteristics

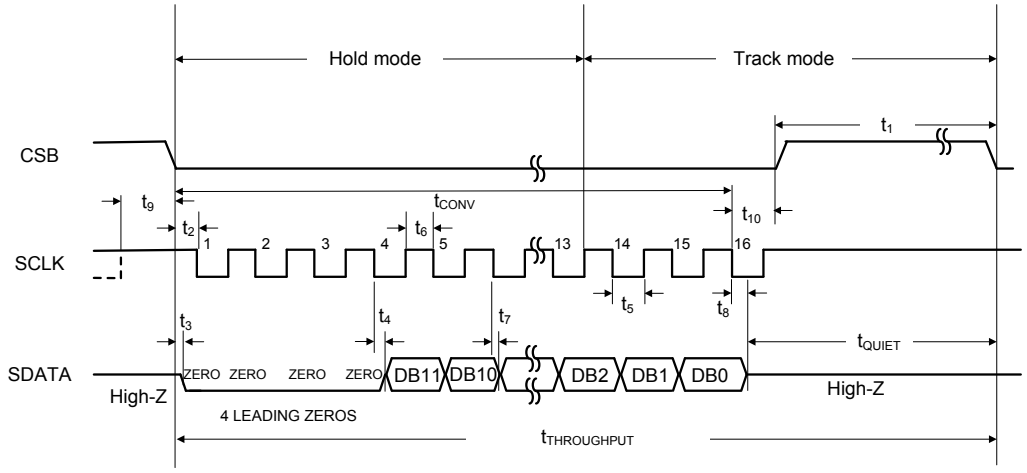
Unless otherwise specified, Ta=-40°C to +105°C (typical: Ta=25°C), V_A=2.7 to 5.25V, f_{SCLK}=20MHz, f_S=1MSPS

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Statistic Converter Characteristics						
Resolution with No missing codes	RES	-	12	-	bit	V_A=2.7 to 3.6V
Integral Non-Linearity	INL	-1.1	-	+1.0	LSB	V_A=2.7 to 3.6V
Differential Non-Linearity	DNL	-0.9	-	+1.0	LSB	V_A=2.7 to 3.6V
Offset Error	OE	-1.2	±0.2	+1.2	LSB	V_A=2.7 to 3.6V
Gain Error	GE	-1.2	±0.3	+1.2	LSB	V_A=2.7 to 3.6V
Dynamic Converter Characteristics						f_{IN}=100kHz, V_{IN}=-0.02dBFS
Signal-to-Noise and Distortion Ratio	SINAD	70	71	-	dB	V_A=2.7 to 3.6V
		68	70	-	dB	V_A=4.75 to 5.25V
Signal-to-Noise-Ratio	SNR	70.8	71.5	-	dB	V_A=2.7 to 3.6V
		68.8	71	-	dB	V_A=4.75 to 5.25V
Total Harmonic Distortion	THD	-	-80	-	dB	V_A=2.7 to 3.6V
Spurious-Free Dynamic Range	SFDR	-	82	-	dB	V_A=2.7 to 3.6V
Effective Number of Bits	ENOB	11.3	11.5	-	bit	V_A=2.7 to 3.6V
		11.0	11.3	-	bit	V_A=4.75 to 5.25V
Inter-modulation Distortion 1, (Second Order Term)	IMD1	-	-78	-	dB	V_A=5.25V 103.5kHz, 113.5kHz
Inter-modulation Distortion 2, (Third Order term)	IMD2	-	-76	-	dB	V_A=5.25V 103.5kHz, 113.5kHz
Full Power Band Width 1	FPBW1	-	10.1	-	MHz	V_A=5V
Full Power Band Width 2	FPBW2	-	7.2	-	MHz	V_A=3V
Aperture Delay	t_{AD}	-	4.3	-	ns	V_A=5V
Aperture Jitter	t_{AJ}	-	30	-	ps	V_A=5V
Clock Frequency	f_{SCLK}	10	-	20	MHz	
Sampling Rate	f_S	500k	-	1M	SPS	
Track/Hold Acquisition Time	t_{ACQ}	-	-	350	ns	
Analog Input Characteristics						
Input Voltage Range	V_{IN}	0	-	V_A	V	
Input DC Leakage Current	I_{LEAK}	-1	±0.1	+1	µA	V_{IN}=0V or V_A
Input Capacitance	C_{INA}	-	28	-	pF	Track mode, V_A=5V
		-	4	-	pF	Hold mode, V_A=5V
Digital Input Characteristics						
High Input Voltage	V_{IH}	2.4	-	-	V	V_A=5.25V
	V_{IH}	2.1	-	-	V	V_A=3.6V
Low Input Voltage	V_{IL}	-	-	0.8	V	V_A=5V
	V_{IL}	-	-	0.4	V	V_A=3V
Input Current	I_{IND}	-1	±0.1	+1	µA	V_{IND}=0V or V_A
Input Capacitance	C_{IND}	-	2.5	4	pF	
Digital Output Characteristics						
Output High Voltage	V_{OH}	V_A-0.2	V_A-0.03	-	V	Isource=200µA
	V_{OH}	-	V_A-0.1	-	V	Isource=1mA
Output Low Voltage	V_{OL}	-	0.02	0.4	V	Isink=200µA
	V_{OL}	-	0.1	-	V	Isink=1mA
High-Z Leakage Current	I_{OZ}	-10	±0.1	+10	µA	V_{OZ}=0V or V_A
High-Z Output Capacitance	C_{OUT}	-	2	4	pF	
Power Supply Characteristics						
Supply Voltage	V_A	2.7	-	5.25	V	
Operational Current Consumption	I_A	-	1.6	2.8	mA	V_A=5.25V, f_S=1MSPS
		-	0.5	1.2	mA	V_A=3.6V, f_S=1MSPS
		-				

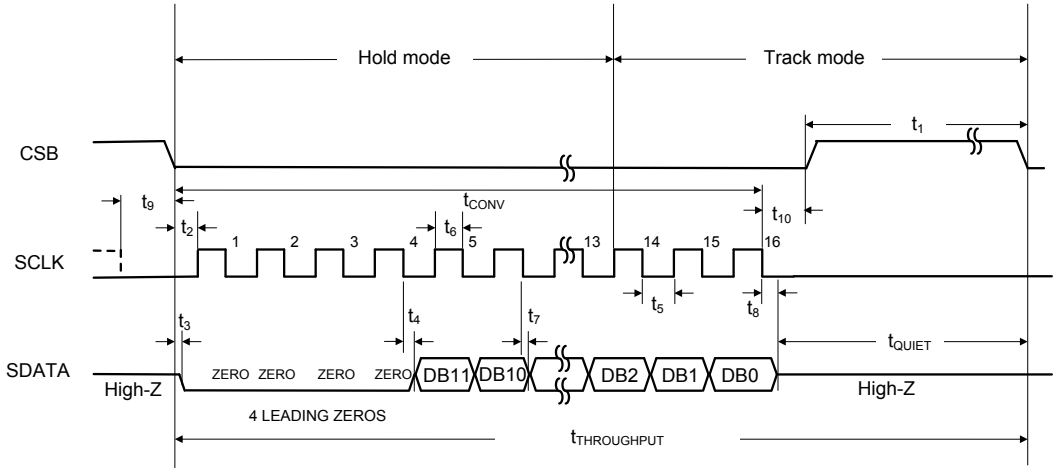
Timing Specifications

Unless otherwise specified, Ta=-40°C to +85°C (Typical: Ta=25°C), V_A=2.7 to 5.25V, f_{SCLK}=10 to 20MHz, C_L=25pF

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Conversion Time	t_{CONV}	-	16	-	SCLK	
CSB Pulse Width	t_1	10	-	-	ns	
CSB Setup Time	t_2	10	-	-	ns	
SDATA Enable Time	t_3	-	-	20	ns	
SDATA Access Time 1	t_4	-	-	40	ns	V_A=2.7 to 3.6V
SDATA Access Time 2	t_4	-	-	20	ns	V_A=4.75 to 5.25V
SCLK Low Pulse Width	t_5	0.4 x t_{SCLK}	-	-	ns	
SCLK High Pulse Width	t_6	0.4 x t_{SCLK}	-	-	ns	
SDATA Hold Time 1	t_7	7	-	-	ns	V_A=2.7 to 3.6V
SDATA Hold Time 2	t_7	5	-	-	ns	V_A=4.75 to 5.25V
SDATA Disable Time 1	t_8	6	-	25	ns	V_A=2.7 to 3.6V
SDATA Disable Time 2	t_8	5	-	25	ns	V_A=4.75 to 5.25V
CSB Hold Time	t_9	10	-	-	ns	
SCLK Setup Time	t_{10}	10	-	-	ns	
Quiet Time	t_{QUIET}	50	-	-	ns	
Power-Up Time	t_{POWUP}	-	1	-	µs	
Throughput Period	$t_{THROUGHPUT}$	1	-	20	µs	



(a) If SCLK is high at the falling edge of CSB



(b) If SCLK is low at the falling edge of CSB

Figure 5. Serial Interface Timing Chart

(Note 1) When the BU1S12S1AG-LB is used at the sampling frequency of 1MSPS, it is recommended to hold SCLK high at the falling edge of CSB as shown in Figure 5(a). (See also “3. Serial Interface” on page 10.)

Term Definitions

ACQUISITION TIME:
At the 13th rising edge of SCLK, the mode is changed from Hold mode to Track mode and the sampling capacitor starts to be charged by the analog input voltage. This charge time is defined as the acquisition time.

APERTURE DELAY:
It is defined as the time from falling edge of CSB to the time when the analog input voltage is acquired.

APERTURE JITTER:
The variation in the aperture delays in sampling operations. Aperture jitter gets to affect signal-to-noise ratio.

INTEGRAL NON-LINEARLITY (INL):
It is a measure of the deviation of each individual code from a line drawn from zero scale (0.5 LSB below the first code transition) through full scale (0.5 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

DIFFERENTIAL NON-LINEARLITY (DNL):
It is the measure of the maximum deviation from the ideal step size of 1 LSB.

OFFSET ERROR (OE):
It is the deviation of the first code transition “(000…000) to (000…001)” from the ideal of 0.5 LSB.

FULL SCALE ERROR (FSE):
It is the deviation of the last code transition “(111…110) to (111…111)” from the ideal of “V_A – 1.5LSB.”

GAIN ERROR (GE):
It is defined as full scale error minus offset error.

TOTAL HARMONIC DISTORTION (THD):
It is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

SIGNAL TO NOISE AND DISTORTION RATIO(SINAD):
It is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the sampling frequency, including harmonics but excluding d.c.

EFFECTIVE NUMBER OF BITS(ENOB):
It is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as “(SINAD – 1.76) / 6.02” and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

SIGNAL TO NOISE RATIO (SNR):
It is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below half the sampling frequency, not including harmonics.

SPURIOUS FREE DYNAMIC RANGE (SFDR):
It is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may be a harmonic.

CONVERSION TIME:
It is the required time for the A/D converter to convert the sampled analog input signal to the digital code.

THROUGHPUT PERIOD:
It is the period that should be used as an interval time between any adjacent conversions.

Typical Performance Characteristics

Unless otherwise noted, Ta=25 °C.

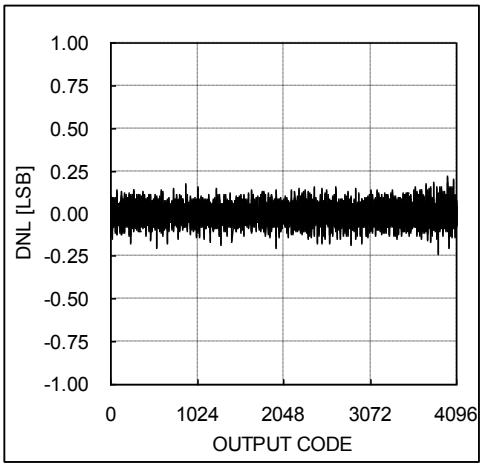


Figure 6. DNL vs OUTPUT CODE
(V_A=3V, f_{SCLK}=10MHz, f_S=500kSPS)

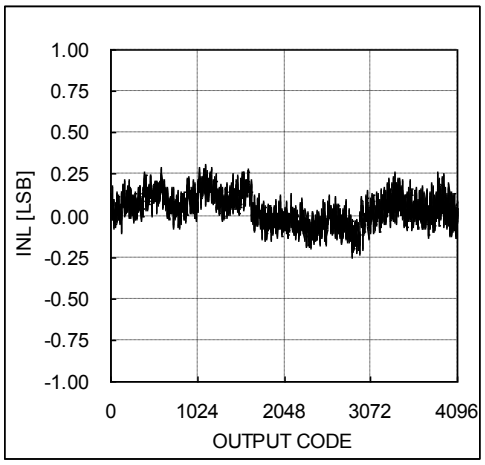


Figure 7. INL vs OUTPUT CODE
(V_A=3V, f_{SCLK}=10MHz, f_S=500kSPS)

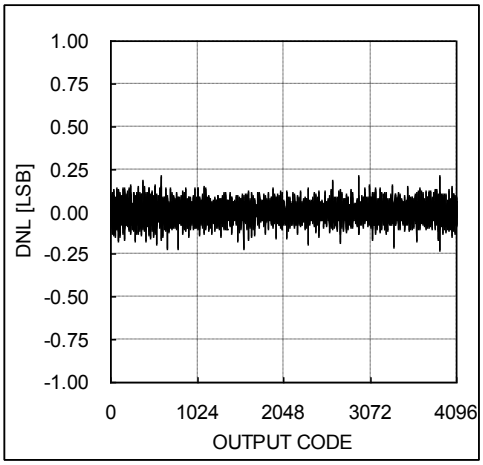


Figure 8. DNL vs OUTPUT CODE
(V_A=3V, f_{SCLK}=20MHz, f_S=1MSPS)

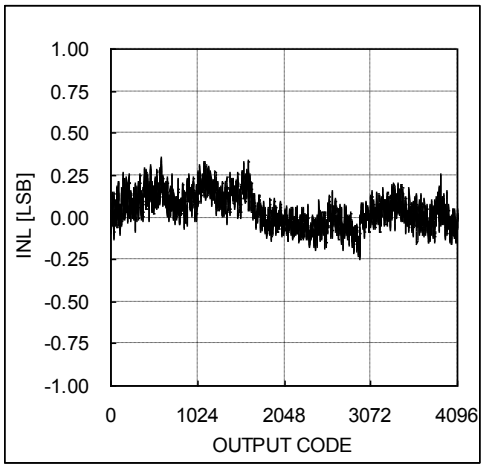


Figure 9. INL vs OUTPUT CODE
(V_A=3V, f_{SCLK}=20MHz, f_S=1MSPS)

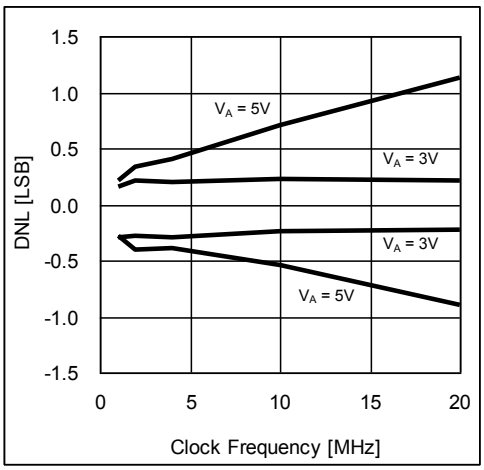


Figure 10. DNL vs CLOCK FREQUENCY

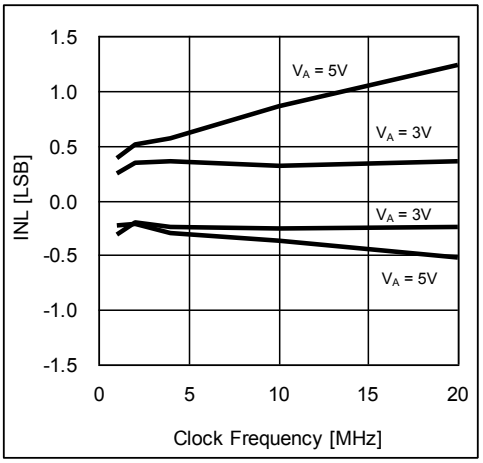


Figure 11. INL vs CLOCK FREQUENCY

Typical Performance Characteristics – continued

Unless otherwise noted, Ta=25 °C, f_{IN} =100 kHz.

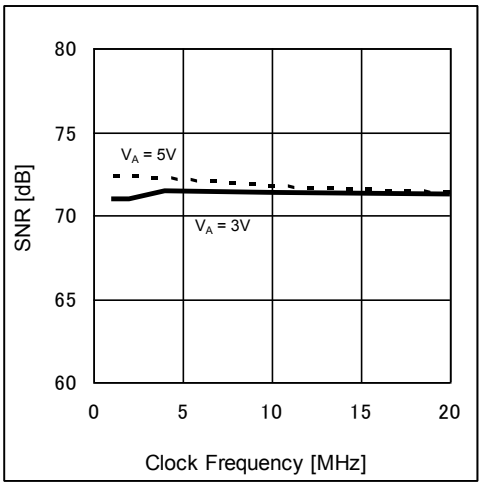


Figure 12. SNR vs CLOCK FREQUENCY

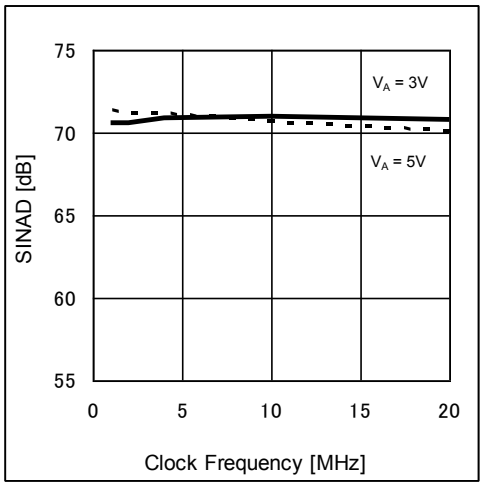


Figure 13. SINAD vs CLOCK FREQUENCY

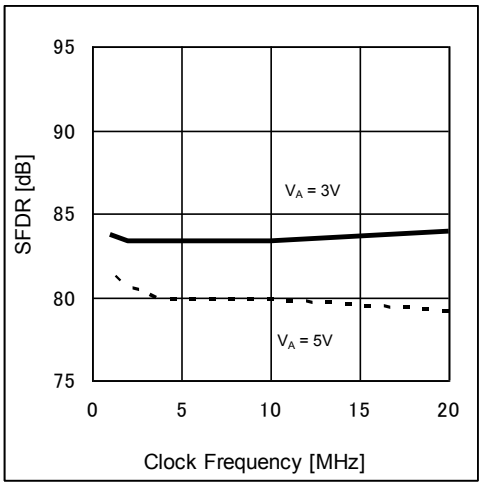


Figure 14. SFDR vs CLOCK FREQUENCY

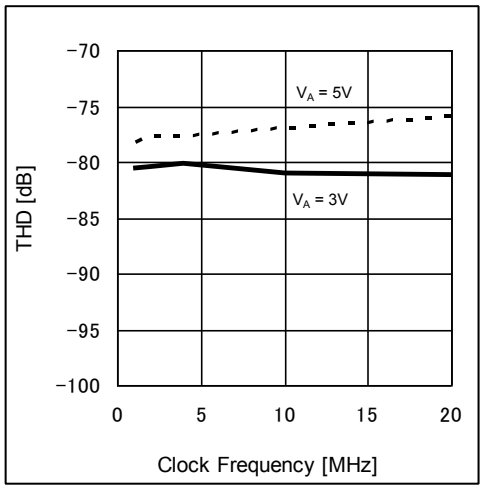


Figure 15. THD vs CLOCK FREQUENCY

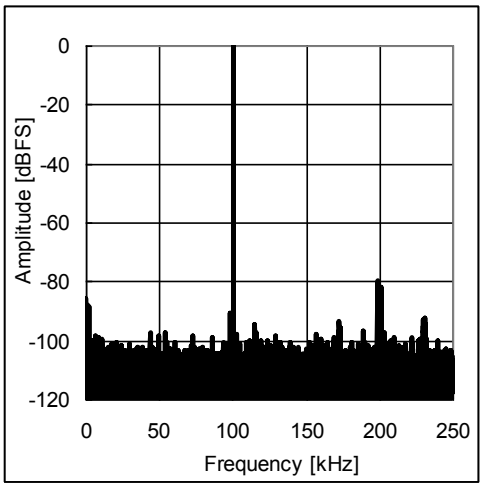


Figure 16. SPECTRAL RESPONCE
(V_A=5V, f_{SCLK}=10MHz, f_S=500kSPS)

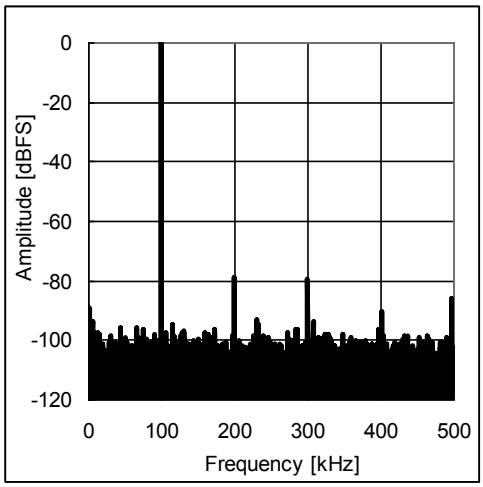


Figure 17. SPECTRAL RESPONCE
(V_A=5V, f_{SCLK}=20MHz, f_S=1MSPS)

Description of Functions

1. Overview of A/D Conversion Process

BU1S12S1AG-LB is a successive-approximation A/D converter designed with a charge-redistribution D/A converter. Simplified schematics of the A/D converter are shown in Figure 18 and Figure 19.
Figure 18 shows the A/D converter in Track mode: the switch SW1 is in the position A, SW2 is closed and balances the comparator. Then, the sampling capacitor is charged with the analog input voltage V_{IN}.
Figure 19 shows the A/D converter in Hold mode. When a conversion starts, the A/D converter goes into Hold mode: SW2 becomes open, SW1 connects the sampling capacitor to ground through the terminal B and the comparator loses its balance. The control logic controls the input voltage of the comparator via the sampling capacitors of the charge-redistribution D/A converter to get the comparator back into a balanced state. A/D conversion finishes when the comparator balances again. The control logic also generates the output code of the A/D converter.

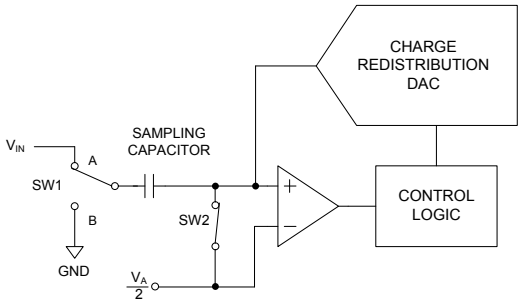


Figure 18. Track mode

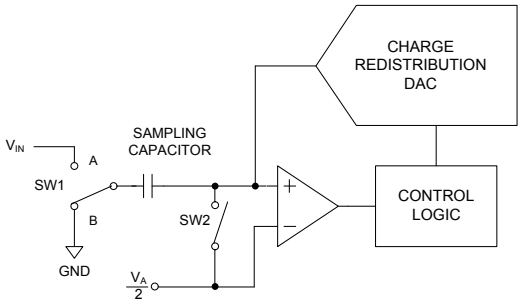


Figure 19. Hold mode

2. Ideal Transfer Characteristics

Figure 20 shows the ideal transfer characteristics of BU1S12S1AG-LB. Code transitions occur midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB, and so on. The LSB size for the BU1S12S1AG-LB is V_A / 4096. The output code format of the A/D converter is straight binary

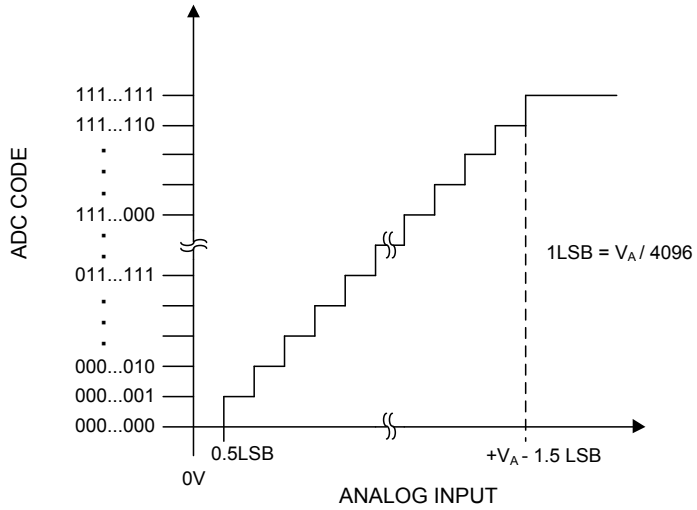
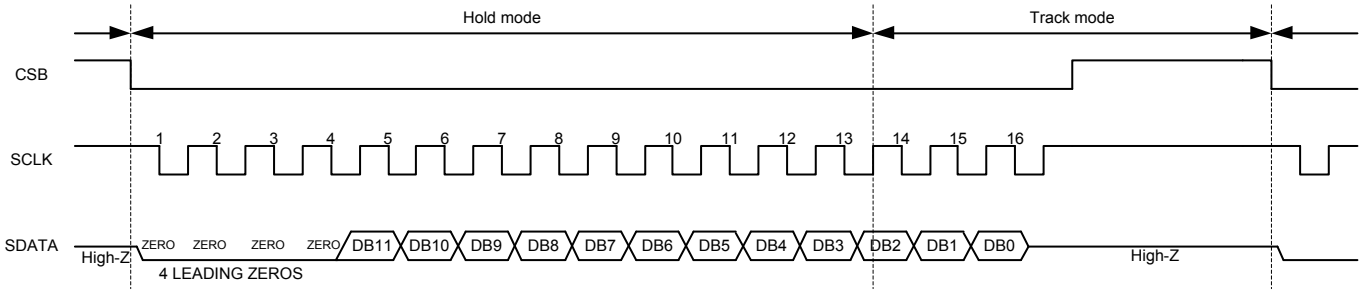


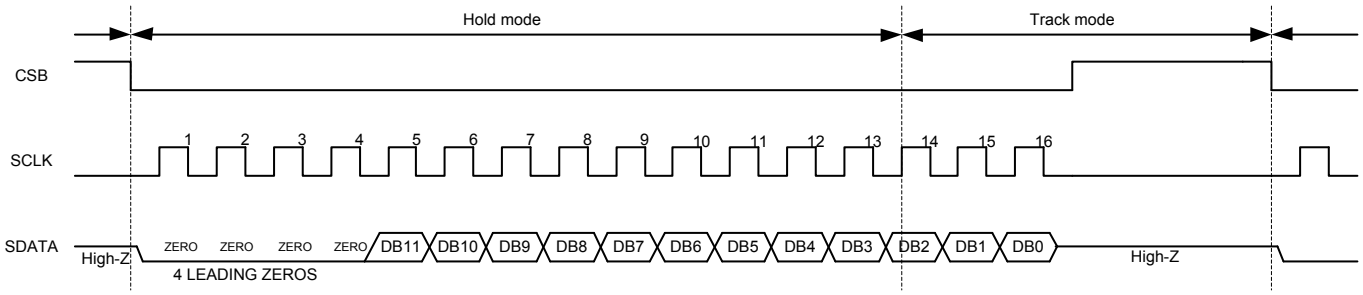
Figure 20. Ideal Transfer Characteristics

3. Serial Interface

The serial interface timing is shown in Figure 21. When CSB goes low, both a conversion process and data transfer are started. At the falling edge of CSB, SDATA changes its state from High-Z to Low, the converter moves from Track mode to Hold mode. A tracked input signal is sampled and held for conversion at this point. The converter returns from Hold mode back to Track mode at the rising edge of SCLK subsequent to the 13th falling edge of it. SDATA goes back to High-Z at the 16th falling edge of SCLK or at the rising edge of CSB. After a conversion, the quiet time t_{QUIET} must be satisfied before the next conversion triggered by the falling edge of CSB.
Sixteen SCLK cycles are needed to read a complete data of the A/D conversion from BU1S12S1AG-LB. First, four leading zeros come out from SDATA. Then, the 12bit data comes out bit by bit, starting from the MSB. The first zero is clocked out at the falling edge of CSB. The remaining leading 3 zeros and data bits are clocked out to SDATA at the falling edge of SCLK; the host IC, the receiver of the A/D conversion data, is intended to receive the data at the subsequent falling edge of SCLK.
To perform A/D conversion properly, the BU1S12S1AG-LB needs at least 16 SCLK cycles while CSB is low. If an A/D conversion is interrupted in the middle of the conversion with CSB going to high before the 16th SCLK falling edge, the following A/D conversion may not be performed normally. Therefore, it is necessary that equal to or more than 16 falling edges of SCLK exist while CSB is low.
In addition, SCLK should be held either high or low at the falling edge of CSB. If SCLK is low at the falling edge of CSB, as shown in Figure 21(b), a Hold mode time length is about a half clock period longer than one if SCLK is high as shown in Figure 21(a). Therefore, when the BU1S12S1AG-LB is used at the sampling frequency of 1MSPS, it is recommended to hold SCLK high at the falling edge of CSB, as shown in Figure 21(a), in order to ensure sufficient Track mode time for the maximum acquisition time.



(a) If SCLK is high at the falling edge of CSB



(b) If SCLK is low at the falling edge of CSB

Figure 21. Serial Interface Timing

4. Dummy Conversion

Dummy conversions are necessary in the following cases.

(1) A/D conversion after power-up

The first A/D conversion data after applying power to the BU1S12S1AG-LB is invalid. Therefore, a dummy conversion is necessary after power-up before getting valid data. In addition, the power-up time is satisfied with a cycle of the dummy conversion.

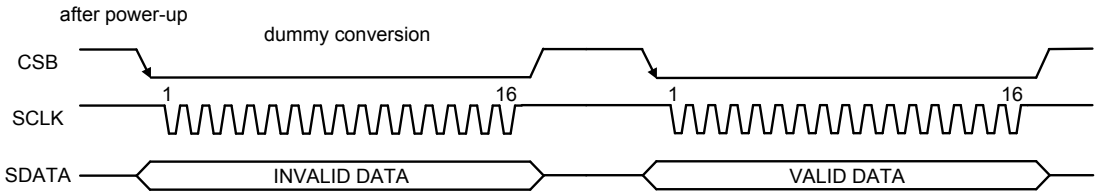


Figure 22. A/D conversion after power-up

(2) A/D conversion after a stop period more than the maximum throughput time

The BU1S12S1AG-LB may stop performing A/D conversion between some A/D conversion cycles. If the maximum limit of the throughput period of 20µsec is violated, the first A/D conversion data after the resumption is not valid similar to the case after power-up. Therefore, a dummy conversion cycle is necessary when A/D conversions are resumed after a stop period longer than the limit and the results later than the dummy conversion can be used validly.

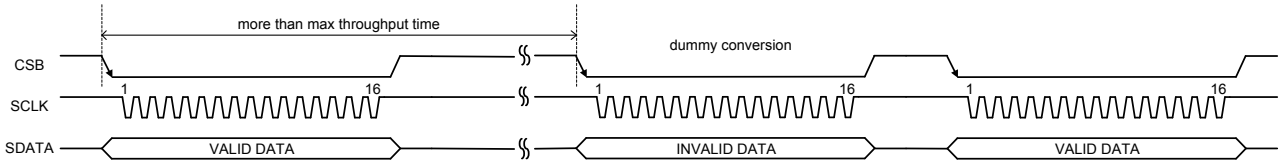


Figure 23. A/D conversion after a long suspension

5. Pin Information

(1) Analog Input Pin

The equivalent analog input circuit is shown in Figure 24. The diodes, D1 and D2, are placed for ESD protection. If the analog input voltage is more than "V_A + 0.3V", or less than "GND – 0.3V", these diodes are turned on and forward current is generated. This current might cause malfunction or irreversible damage to BU1S12S1AG-LB. The capacitance value of the C1 in Figure 24 is typically 4pF, derived from the package parasitic capacitance. The R1 is the resistance of the track/hold switch, typically 500Ω. The C2 is the sampling capacitance of BU1S12S1AG-LB, and the capacitance value is typically 24pF.

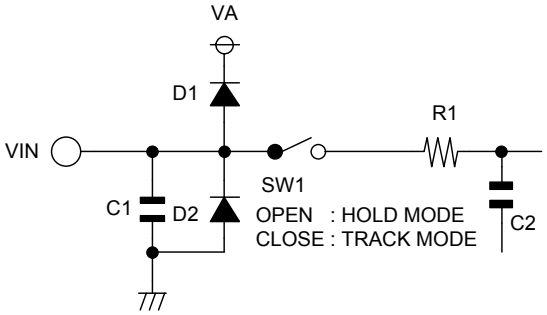


Figure 24. Analog Input Equivalent Circuit

(2) Digital Input and Output Pins

The equivalent digital input circuit is shown in Figure 25. Digital input pins, CSB and SCLK, don't have any diodes to VA. Thus, the maximum rating of "V_A + 0.3V" is not applied to these digital input pins. Digital input voltage range can vary from ground to 5.25V regardless of the supply voltage V_A. This enables BU1S12S1AG-LB to be interfaced with a wide range of logic levels, independent of the supply voltage V_A.

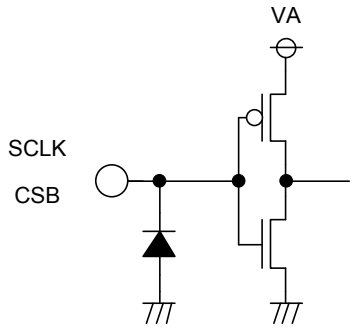


Figure 25. Equivalent Digital Input Circuit

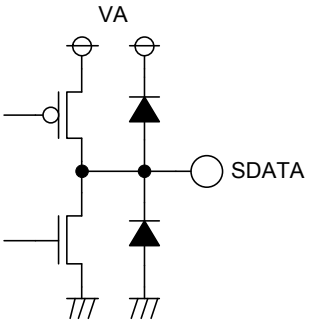


Figure 26. Equivalent Digital Output Circuit

6. Considerations in Application Circuits

As shown in Figure 2, a voltage reference IC is used; 0.1μF and 10μF bypass capacitors between VA and GND are used as measures against high and low frequency noise respectively to make the maximum use of the AD converter's capability. Ceramic capacitors of 0.1μF and 1μF to 10μF are to be used as decoupling capacitor near the AD converter. Especially, the capacitor of 0.1μF should be placed as close to VA pin of BU1S12S1AG-LB as possible.
Because the voltages of VA and GND are used as the reference voltages for the A/D converter, the deviation of the supply voltage directly affects the full scale and has much influence on its characteristics. Therefore, the fully stable supply voltage should be connected to VA.

The output impedance of the analog input signal source should be small enough. Charge stored internally in the sampling capacitor of the track/hold circuit is swept out to the analog input pin VIN at the transition from Hold mode to Track mode because of the difference of the voltage between the input signal voltage and the sampling capacitor voltage. This charge could cause undesirable voltage deviation. If influence of the deviation remains at the transition from Track mode to Hold mode, it could cause the conversion error.
If a buffer amplifier is used to get the analog input to be low impedance, high-speed response is required of the buffer amplifier. A decoupling capacitor and a resister on the VIN analog input could support the amplifier to reduce the influence of the charge.

The voltage fluctuation on the supply and ground pins is caused by the charge and discharge of the digital input and output pins through the digital signals. This fluctuation can be reduced by inserting resisters serially to the digital input and output pins. The resistance values must be small enough not to cause critical delay errors. It is more effective to place these resisters as close to the digital pins as possible.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

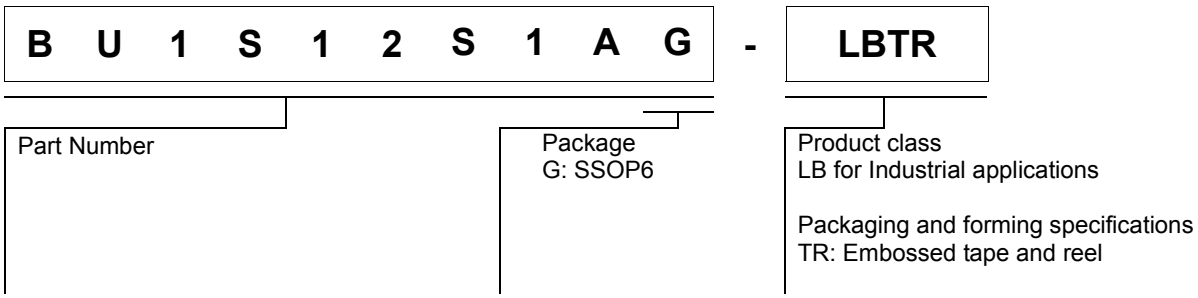
12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

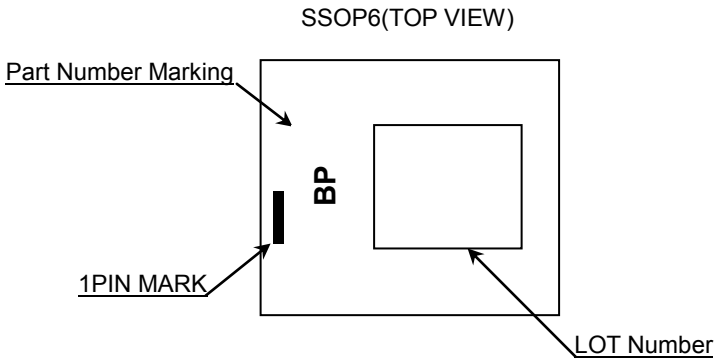
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

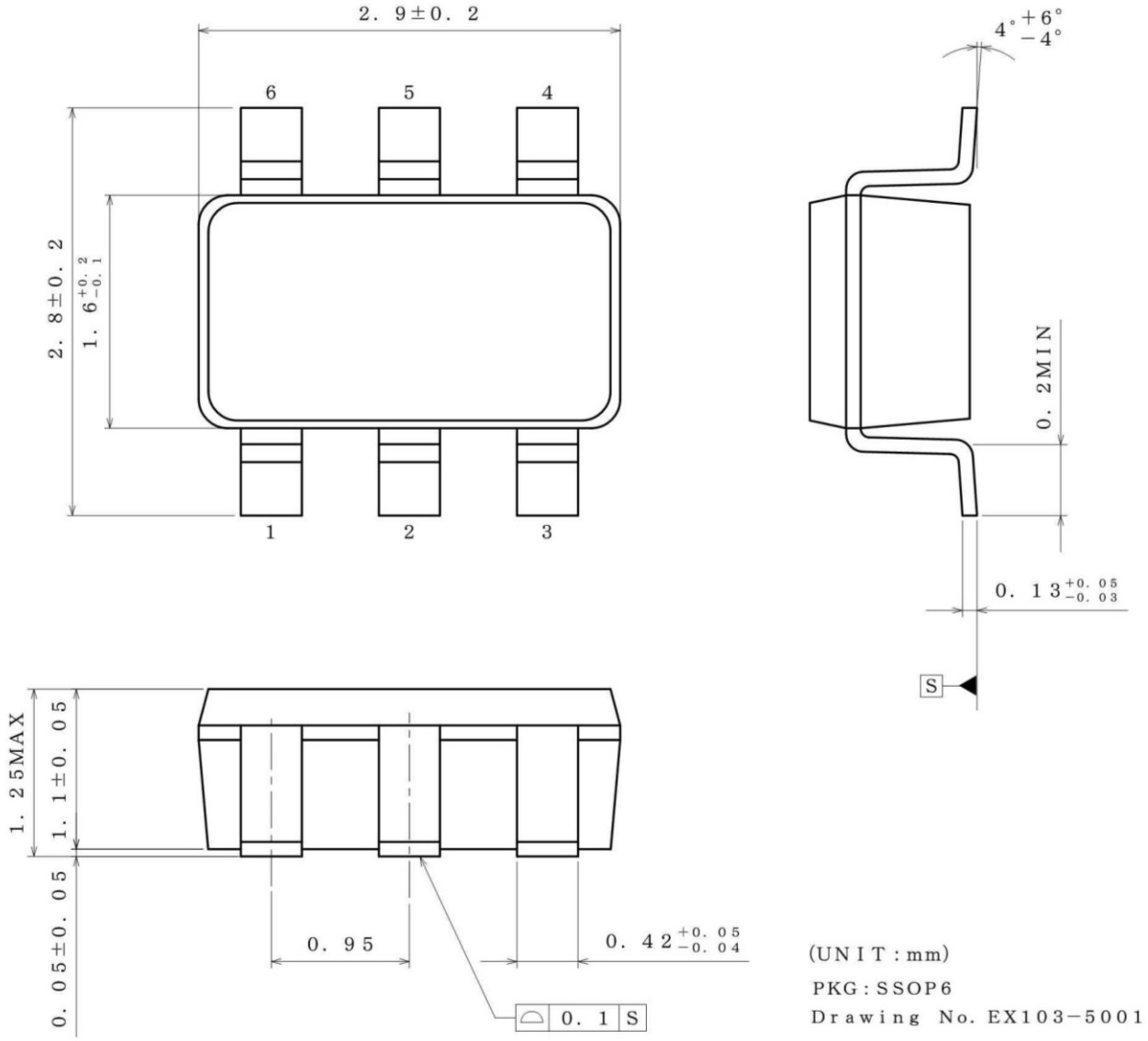


Marking Diagrams



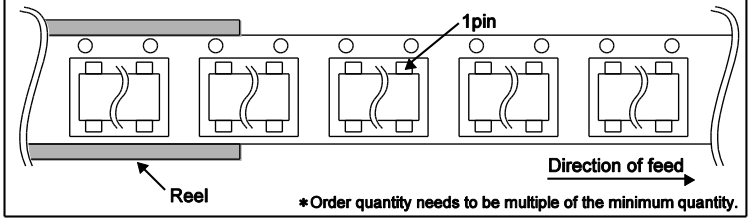
Physical Dimension, Tape and Reel Information

Package Name	SSOP6



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
04.Jul.2016	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

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BU1S12S1AG-LB - Web Page

Part Number	BU1S12S1AG-LB
Package	SSOP6
Unit Quantity	3000
Minimum Package Quantity	3000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes