

Serial-in / Parallel-out Driver Series

4-input Serial-in / Parallel-out Drivers

BU2050F

Description

BU2050F is a CMOS output driver. It incorporates a built-in shift register and a latch circuit to turn on a maximum of 8 outputs by a 4-line interface, linked to a

A CMOS output provides maximum 25mA current.

Features

- LED can be driven directly
- 8 bit parallel output

Applications

- Drive of LED
- Drive of Solenoid
- Drive of Relay

Key Specifications

Power supply voltage range: 4.5V to 5.5V 0V to Output voltage: V_{DD}

Operating temperature range: -40°C to +85°C

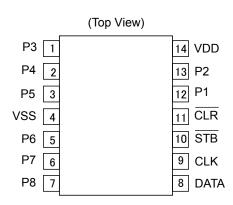
Package SOP14

W(Typ) x D(Typ) x H(Max) 8.70mm x 6.20mm x 1.71mm

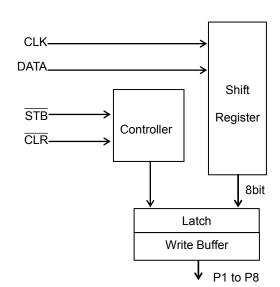


SOP14 BU2050F

Pin Configurations



Block Diagrams



Pin Descriptions

Pin No.	Pin Name	Ю	Function	
1	P3			
2	P4	0	Parallel Data Output	
3	P5			
4	VSS	-	Ground	
5	P6			
6	P7	0	Parallel Data Output	
7	P8			
8	DATA	1	Serial Data Input	
9	CLK	I	Clock Signal Input	
10	STB	I	Strobe Signal Input In case of "L", the data of shift register is outputted to P1 through P8. In case of "H", all parallel outputs and data of latch circuit do not change.	
11	CLR	I	Reset Signal Input In case of "L", the data of latch circuit reset, and all parallel outputs(P1 to P8) change into "L". Normally CLR=H	
12	P1	0	Parallal Data output	
13	P2	0	Parallel Data output	
14	VDD	-	Power Supply	

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V _{IN}	V_{SS} -0.3 to V_{DD} +0.5	V
Output Voltage	Vo	V _{SS} -0.3 to V _{DD} +0.5	V
Operating Temperature	T _{opr}	-40 to +85	°C
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _D	0.45 ^(Note 1)	W

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 4.5mW per 1°C above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (T_A=25°C, V_{SS}=0V)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	+4.5 to +5.5	V
Output Voltage	Vo	0 to V _{DD}	V

Electrical Characteristics

DC Characteristics

(unless otherwise specified, V_{DD} =5V, V_{SS} =0V, T_A =25°C)

Doromotor	Symbol	Limits			l lm:t	Condition
Parameter		Min	Тур	Max	Unit	Condition
Input high-level voltage	V _{IH}	0.7V _{DD}	-	V_{DD}	V	-
Input low-level voltage	V _{IL}	V_{SS}	ı	$0.3V_{DD}$	V	-
Input hysteresis	V_{HYS}	-	0.5	-	V	-
		V _{DD} -1.5	-	V_{DD}	>	I _{OH} =-25mA
Output high-level voltage	V _{OHD}	V _{DD} -1.0	-	V_{DD}		I _{OH} =-15mA
		V _{DD} -0.5	-	V_{DD}		I _{OH} =-10mA
	V _{OLD}	V_{SS}	-	1.5	V	I _{OL} =25mA
Output low-level voltage		V_{SS}	-	0.8		I _{OL} =15mA
		V _{SS}	1	0.4		I _{OL} =10mA
Quiescent current	I _{DD}	-	-	0.1	mA	$V_{IH}=V_{DD}, V_{IL}=V_{SS}$

Switching Characteristics

(unless otherwise specified, V_{DD} =5V, V_{SS} =0V, T_A =25°C)

Parameter	Symbol	Limits			Unit	Condition	
Farameter		Min	Тур	Max	Offic	Condition	
Set up time (DATA-CLK)	t _{SD}	20	-	-	ns	-	
Hold time (DATA-CLK)	t _{HD}	20	-	-	ns	-	
Set up time (STB – CLK)	t _{SSTB}	30	-	-	ns	-	
Hold time (STB – CLK)	t _{HSTB}	30	-	-	ns	-	
Propagation delay (CLK – P1 to P8)	t PDPCK	-	-	100	ns	P1 to P8 terminal load 20pF or less	
Propagation delay (STB – P1 to P8)	t _{PDPSTB}	-	-	80	ns	P1 to P8 terminal load 20pF or less	
Propagation delay (CLR – P1 to P8)	tpdpclr	-	-	80	ns	P1 to P8 terminal load 20pF or less	
Maximum clock frequency	f _{MAX}	5	-	-	MHz	-	

Waveform of Switching Characteristics

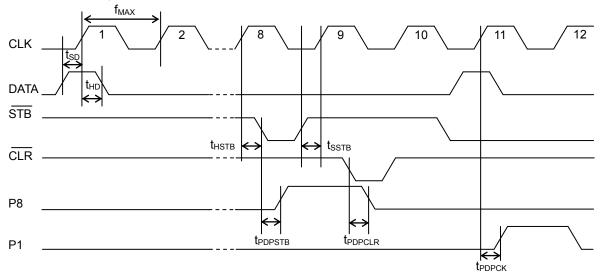


Figure 1. Waveform of Switching Characteristics

Test Circuits

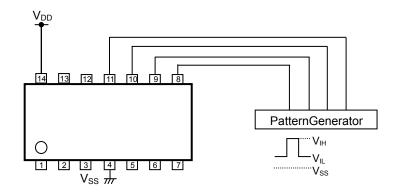


Figure 2. Test Circuit of Input H/LVoltage

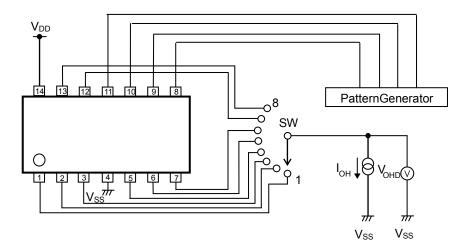


Figure 3. Test Circuit of Output H Voltage

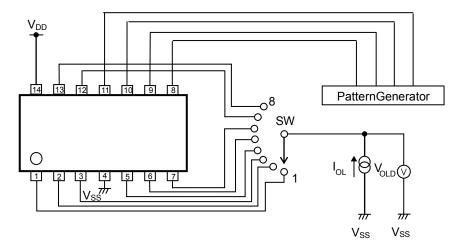


Figure 4. Test Circuit of Output L Voltage

Test Circuits - continued

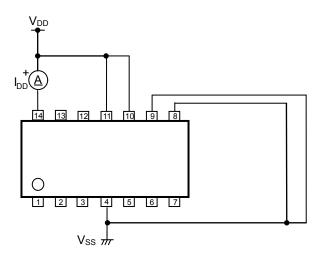


Figure 5. Test Circuit of Static Dissipation Current

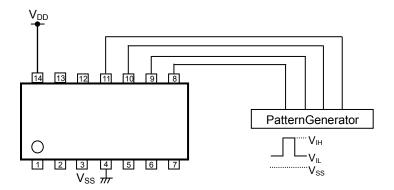


Figure 6. Test Circuit of Switching Characteristics

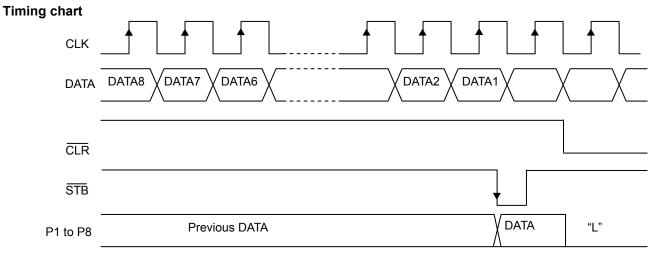


Figure 7. Timing chart

- 1. After the power is turned on and the voltage is stabilized, STB should be activated, after clocking 8 data bits into the DATA pin.
- 2. Parallel outputs (P1 to P8) are set to the shift register data after the eighth clock by the STB.
- 3. Since the $\overline{\text{STB}}$ is level latch, data is retained in the "L" section and renewed in the "H" section of the $\overline{\text{STB}}$.

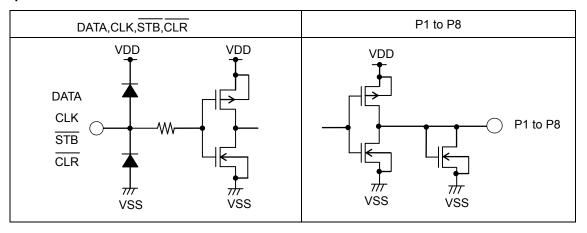
[Function Explanation]

- A latch circuit has the reset function, which is common in all bits. In case of $\overline{\text{CLR}}$ terminal is "L", the latch circuit is reset non-synchronously without the other input condition, and all parallel outputs change into "L".
- A serial data inputted from DATA terminal is read in shift register with synchronized rising transition of clock.
 In case of STB is "L" (CLR is "H"), transmit the data which read in the shift register to latch circuit, and outputs from the parallel data output terminal (P1 to P8). In case of STB is "H", all parallel outputs and the data of latch do not change.

[Truth Table]

Input			Function		
CLK	STB	CLR	Function		
×	×	L	All the data of the latch circuit are set to "L" (data of shift register does not change), all the parallel outputs are "L".		
Ŧ	Н	Н	Serial data of DATA pin are latched to the shift register. At this time, the data of the latch circuit does not change.		
L H			The data of the shift register are transferred to the latch circuit, and the data of the latch circuit are outputted from the parallel output pin.		
Ŧ	L H		The data of the shift register shifts 1bit, and the data of the latch circuit and parallel output also change.		

I/O Equivalence Circuits



Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at T_A =25°C(normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θ_{JA} (°C/W). The temperature of IC inside the package can be estimated by this thermal resistance. Figure 8 shows the model of thermal resistance of the package. Thermal resistance θ_{JA} , ambient temperature T_{A} , maximum junction temperature T_{Jmax} , and power dissipation P_D can be calculated by the equation below: $\theta_{JA} = (T_{Jmax} - T_A) / P_D$ (°C/W)

Derating curve in Figure 9 indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{JA} . Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition.

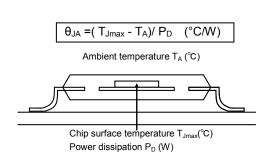


Figure 8. Thermal resistance

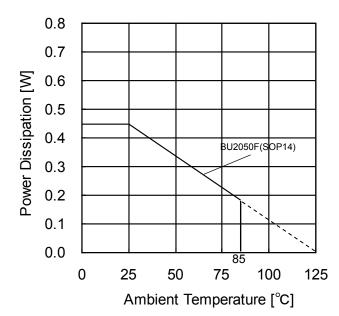


Figure 9. Derating Curve

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

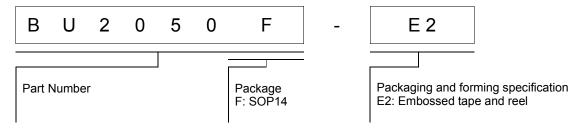
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

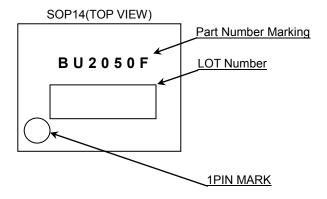
14. Area of Safe Operation (ASO)

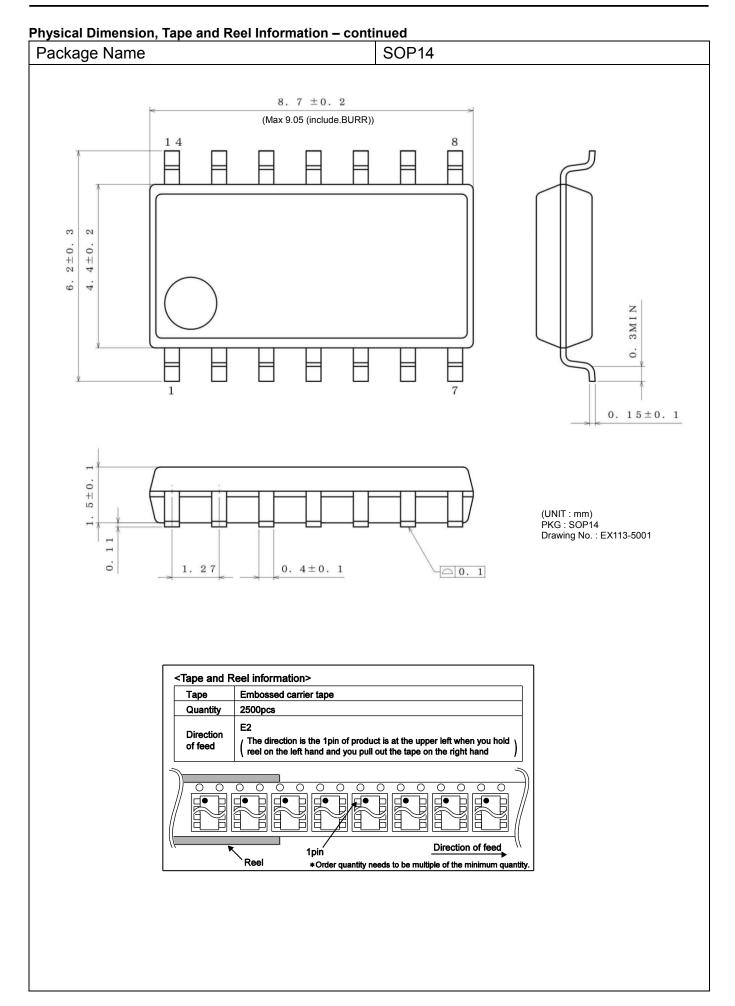
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Ordering Information



Marking Diagrams





Revision History

Date	Revision	Changes				
08.Nov.2013	001	New Release				
18.Sep.2015	002	Page.6 Truth Table : When CLR=L, modified the output=H-> L.				
18.Apr.2016	003	Page.1 Features Deleted "This product can be operated on low voltage". Page.1 Key Specifications Modified power supply voltage range from"2.7V to 5.5V" to "4.5V to 5.5V". Page.2 Pin Descriptions Modified "Function" sentences of pin name STB and CLR. Page.2 Recommended Operating Conditions Modified supply voltage from"+2.7V to +5.5V" to "+4.5V to +5.5V". Page.3 Electrical Characteristics Modified name from "Timing Characteristics" to "Switching Characteristics" Page.3 Electrical Characteristics Modified pin name of propagation delay Tpdpck from "CLR" to "CLK". Page.6 Timing chart Modified pin name from "STB" to "STB". Modified description sentences. Page.7 I/O Equivalence Circuits Modified pin name from "CLOCK" to "CLK". Page.7 Power Dissipation Modified description sentences.				

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CLASSIV	CLASSII	CLASSⅢ	CLASSⅢ

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- 8. Confirm that operation temperature is within the specified range described in the product specification.
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