

# Horizontal Deflection Transistor

... designed for use in televisions.

- Collector–Emitter Voltages  $V_{CES}$  1500 Volts
- Fast Switching — 400 ns Typical Fall Time
- Low Thermal Resistance  $1^{\circ}\text{C}/\text{W}$  Increased Reliability
- Glass Passivated (Patented Photoglass). Triple Diffused Mesa Technology for Long Term Stability

## MAXIMUM RATINGS

Rating	Symbol	BU208A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector–Emitter Voltage	$V_{CES}$	1500	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous	$I_C$	5.0	Vdc
— Peak	$I_{CM}$	7.5	
Base Current — Continuous	$I_B$	4.0	Adc
— Peak (Negative)	$I_{BM}$	3.5	
Total Power Dissipation @ $T_C = 95^{\circ}\text{C}$ Derate above $95^{\circ}\text{C}$	$P_D$	12.5 0.625	Watts $\text{W}/^{\circ}\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +115	$^{\circ}\text{C}$

## THERMAL CHARACTERISTICS

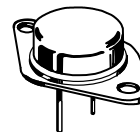
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	$T_L$	275	$^{\circ}\text{C}$

### NOTES:

1. Pulsed 5.0 ms, Duty Cycle  $\leq 10\%$ .
2. See page 3 for Additional Ratings on A Type.
3. Figures in ( ) are Standard Ratings ON Semiconductor Guarantees are Superior.

# BU208A

5.0 AMPERES  
NPN SILICON  
POWER TRANSISTOR  
700 VOLTS



CASE 1–07  
TO–204AA  
(TO–3)

# BU208A

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current <sup>1</sup> ( $V_{CE} = \text{rated } V_{CES}$ , $V_{BE} = 0$ )	$I_{CES}$	—	—	1.0	mAdc
Emitter Base Voltage <sup>1</sup> ( $I_C = 0$ , $I_E = 10\text{ mA}$ ) ( $I_C = 0$ , $I_E = 100\text{ mA}$ )	$V_{EBO}$	5 —	— 7	— —	Vdc
<b>ON CHARACTERISTICS<sup>1</sup></b>					
DC Current Gain ( $I_C = 4.5\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$h_{FE}$	2.25	—	—	
Collector–Emitter Saturation Voltage ( $I_C = 4.5\text{ Adc}$ , $I_B = 2\text{ Adc}$ )	$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage ( $I_C = 4.5\text{ Adc}$ , $I_B = 2\text{ Adc}$ )	$V_{BE(sat)}$	—	—	1.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current–Gain Bandwidth Product ( $I_C = 0.1\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	—	4	—	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	—	125	—	pF
<b>SWITCHING CHARACTERISTICS</b>					
Storage Time (see test circuit fig. 1) ( $I_C = 4.5\text{ Adc}$ , $I_{B1} = 1.8\text{ Adc}$ , $L_B = 10\text{ }\mu\text{H}$ )	$t_s$	—	8	—	$\mu\text{s}$
Fall time (see test circuit fig. 1) ( $I_C = 4.5\text{ Adc}$ , $I_{B1} = 1.8\text{ Adc}$ , $L_B = 10\text{ }\mu\text{H}$ )	$t_f$	—	0.4	—	$\mu\text{s}$

<sup>1</sup>Pulse test: PW = 300  $\mu\text{s}$ ; Duty cycle  $\leq 2\%$ .

# BU208A

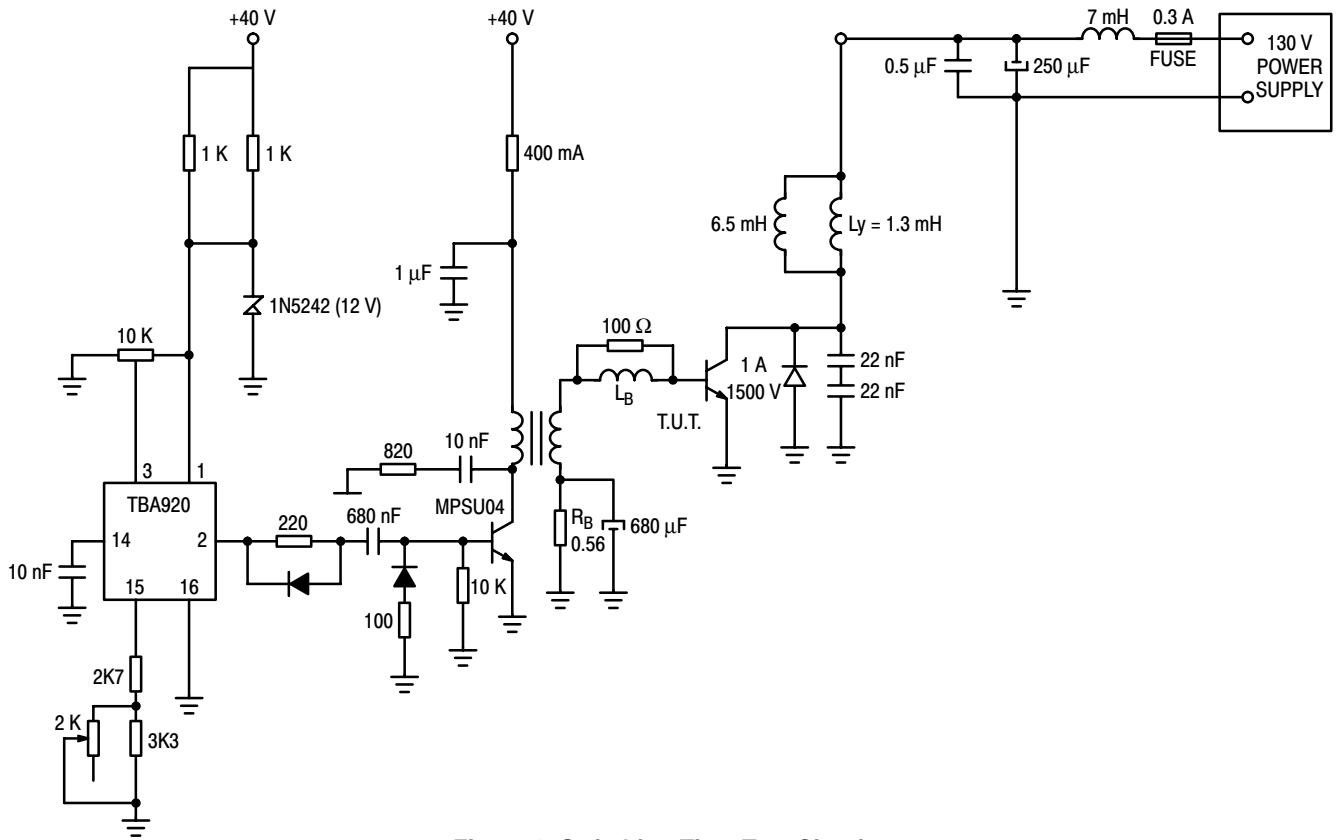


Figure 1. Switching Time Test Circuit

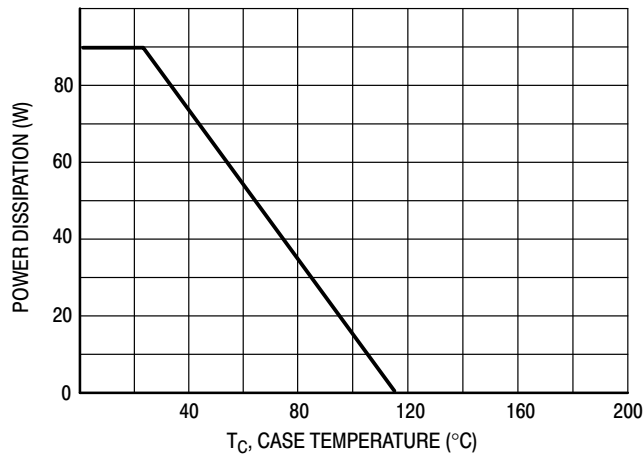


Figure 2. Power Derating

# BU208A

## BASE DRIVE The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough  $I_{B1}$  to satisfy the lowest gain output device  $h_{FE}$  at the end of scan  $I_{CM}$ . Worst-case component variations and maximum high voltage loading must also be taken into account.

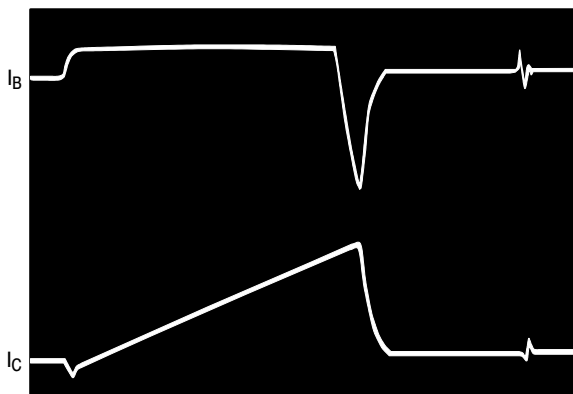
If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 3. This results in rapid, but only partial collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 4, thus allowing access carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right  $L_B$  is usually done empirically since the equivalent circuit is complex, and since there are several important variables ( $I_{CM}$ ,  $I_{B1}$ , and  $h_{FE}$  at  $I_{CM}$ ). One method is to plot fall time as a function of  $L_B$ , at the desired conditions, for several devices within the  $h_{FE}$  specification. A more informative method is to plot power dissipation versus  $I_{B1}$  for a range of values of  $L_B$ .

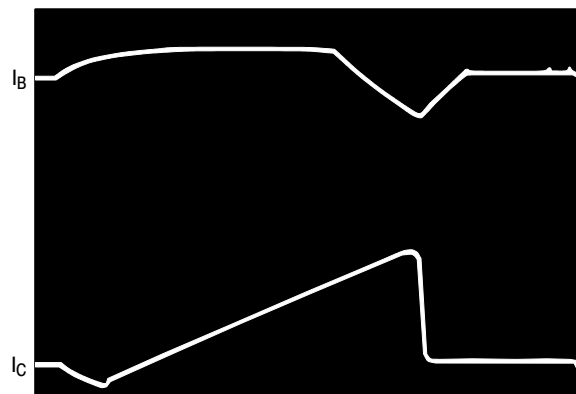
This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. For very low  $L_B$  a very narrow optimum is obtained. This occurs when  $I_{B1} h_{FE} \cong I_{CM}$ , and therefore would be acceptable only for the "typical" device with constant  $I_{CM}$ . As  $L_B$  is increased, the curves become broader and flatter above the  $I_{B1} h_{FE} = I_{CM}$  point as the turn off "tails" are brought under control. Eventually, if  $L_B$  is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different  $h_{FE}$ , essentially moves the curves to the left, or right according to the relation  $I_{B1} h_{FE} = \text{constant}$ . It then becomes obvious that, for a specified  $I_{CM}$ , an  $L_B$  can be chosen which will give low dissipation over a range of  $h_{FE}$  and/or  $I_{B1}$ . The only remaining decision is to pick  $I_{B1}$  high enough to accommodate the lowest  $h_{FE}$  part specified. Neither  $L_B$  nor  $I_{B1}$  are absolutely critical. Due to the high gain of ON Semiconductor devices it is suggested that in general a low value of  $I_{B1}$  be used to obtain optimum efficiency — eg. for BU208A with  $I_{CM} = 4.5$  A use  $I_{B1} \approx 1.5$  A, at  $I_{CM} = 4$  A use  $I_{B1} \approx 1.2$  A. These values are lower than for most competition devices but practical tests have showed comparable efficiency for ON Semiconductor devices even at the higher level of  $I_{B1}$ .

An  $L_B$  of 10  $\mu\text{H}$  to 12  $\mu\text{H}$  should give satisfactory operation of BU208A with  $I_{CM}$  of 4 to 4.5 A and  $I_{B1}$  between 1.2 and 2 A.

### TEST CIRCUIT WAVEFORMS



(TIME)  
Figure 3.



(TIME)  
Figure 4.

### TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive

power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected.

# BU208A

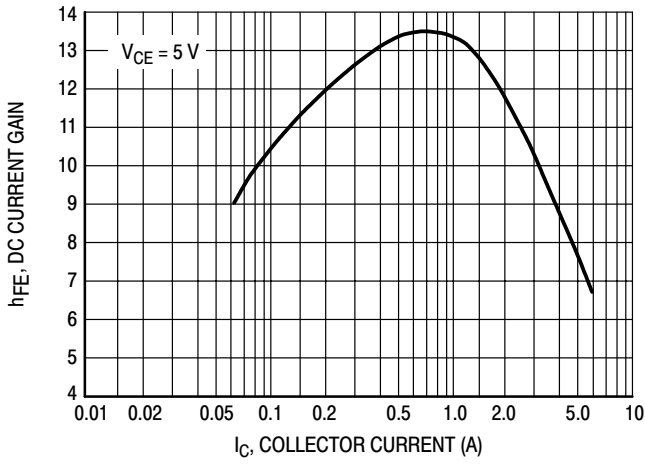


Figure 5. DC Current Gain

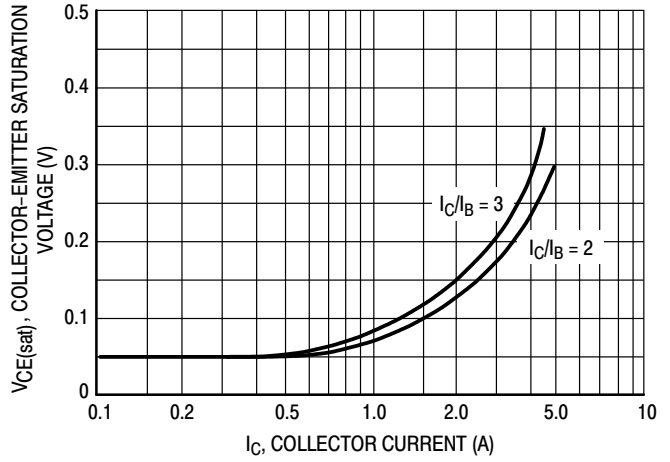


Figure 6. Collector-Emitter Saturation Voltage

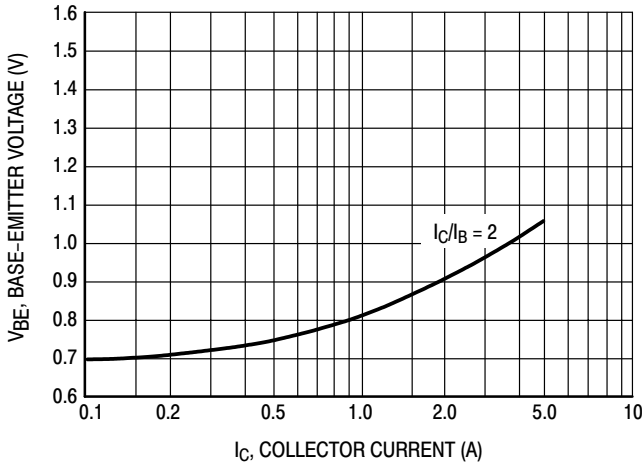


Figure 7. Base-Emitter Saturation Voltage

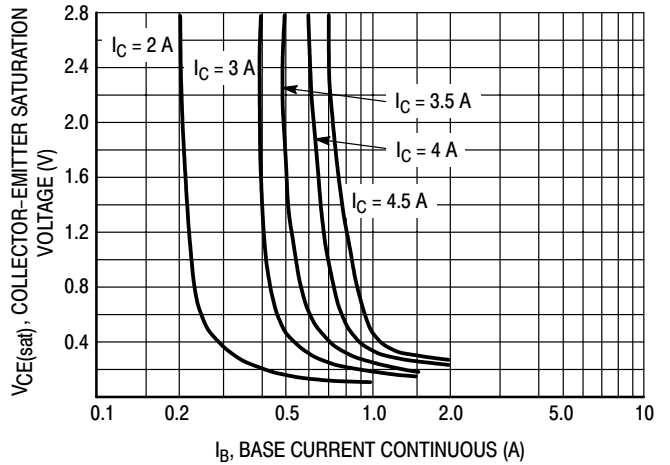


Figure 8. Collector Saturation Region

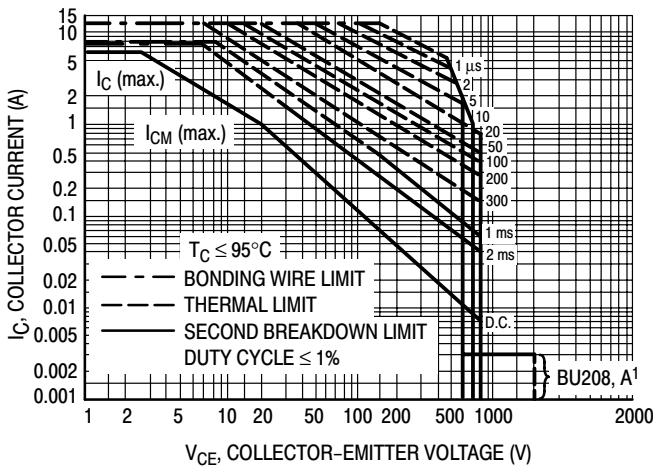


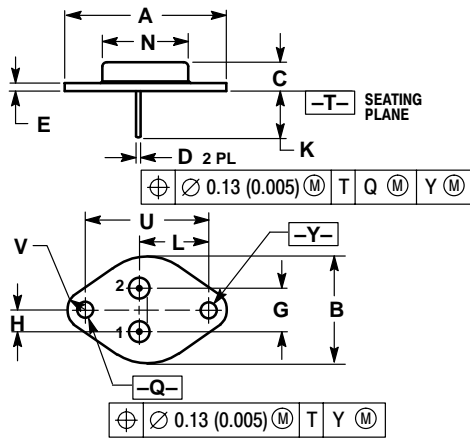
Figure 9. Maximum Forward Bias Safe Operating Area

<sup>1</sup>Pulse width  $\leq 20 \mu\text{s}$ . Duty cycle  $\leq 0.25$ .  $R_{BE} \leq 100 \text{ Ohms}$ .

# BU208A

## PACKAGE DIMENSIONS

### CASE 1-07 TO-204AA (TO-3) ISSUE Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	1.550 REF	---	39.37 REF
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

- STYLE 1:  
PIN 1. BASE  
2. EMITTER  
CASE: COLLECTOR

**Notes**

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