

STRUCTURE: Silicon Monolithic integrated circuit  
 PRODUCT NAME: Servo signal processor for compact disc player  
 TYPE NAME: **BU24545**

FEATURES: The BU24545 is a servo signal processor complete with built-in pre-servo amplifier and 4-bit microcomputer and anti-shock memory controller for application to compact disc player.

○ Absolute maximum ratings (Ta=25°C)

Items	Symbol	Ratings	Unit
Power supply voltage	V <sub>DD</sub>	4.5	V
Internal power supply voltage	V <sub>CORE</sub>	2.5	V
Power dissipation	P <sub>d</sub>	1.0 *1	W
Operating temp. range	T <sub>opr</sub>	-40 ~ +85	°C
Storage temp. range	T <sub>stg</sub>	-55 ~ +125	°C

\*1 Use of this processor at Ta = 25°C and over is subject to reduction of 10mW per 1°C.

\* Operation is not guaranteed.

○ Recommendation Operating range (Ta=-40 ~ +85°C)

Items	Symbol	Ratings	Unit
Power supply voltage	V <sub>DD</sub>	2.7 ~ 3.6	V
Internal power supply voltage	V <sub>CORE</sub>	1.4 ~ 1.65	V

\* This product is not designed for protection against radioactive rays.

○ Electrical characteristics (Digital system)

V<sub>DD</sub>=3.0V, V<sub>CORE</sub>=1.5V (Unless otherwise specified Ta = 25°C)

Items	Symbol	Limit			Unit	Conditions	
		MIN	TYP	MAX			
Input voltage	H-level voltage	V <sub>IH</sub>	2.1	-	-	V	
	L-level voltage	V <sub>IL</sub>	-	-	0.9	V	
Hysteresis input voltage	H-level voltage	V <sub>IH</sub>	2.3	-	-	V	
	L-level voltage	V <sub>IL</sub>	-	-	1.1	V	
Input L current to Pull-up resistor	I <sub>IL</sub>	-35	-75	-115	μA	V <sub>IN</sub> =0V	
Input current	I <sub>I</sub>	-	-	±1	μA	V <sub>IN</sub> =0~3V	
Output voltage	H-level voltage	V <sub>OH</sub>	2.5	-	-	V	I <sub>O</sub> =-0.6mA
	L-level voltage	V <sub>OL</sub>	-	-	0.5	V	I <sub>O</sub> =0.6mA

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).

Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

○ Electrical Characteristics (Analog system 1/2)

$V_{DD}=3.0V$ ,  $V_{CORE}=1.5V$  (Unless otherwise specified  $T_a = 25^{\circ}C$ ,  $R_L=10k\Omega$ , standard  $V_C$ )

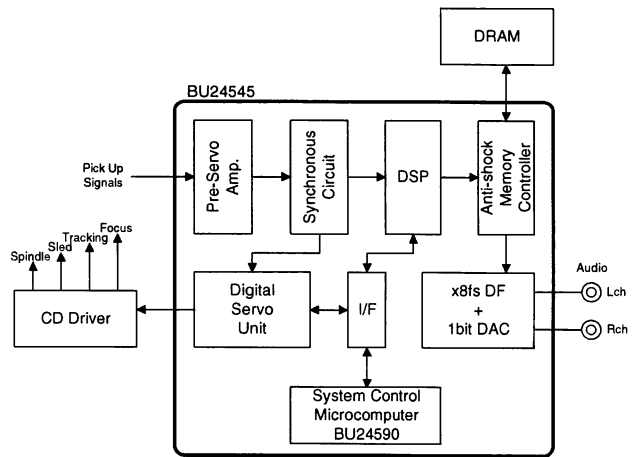
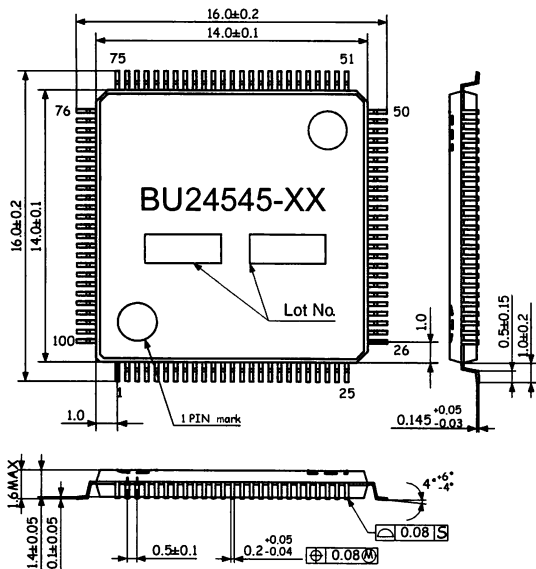
Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
Total						
Circuit current 1	$I_{Q1}$	-	11	28	mA	AVDD1,AVDD2 DVDD1,DVDD2,DVDD3
Circuit current 2	$I_{Q2}$	-	10	20	mA	VDD_CORE1,VDD_CORE2
PLL (VCO)						
Max. oscillation Frequency	$f_{VCOH}$	4.6	6.5	-	MHz	1/4 of A13 and VCO outputs
Min. oscillation Frequency	$f_{VCOL}$	-	1.1	1.7	MHz	1/4 of A13 and VCO outputs
FC DAC						
Offset voltage	$V_{FCOF}$	-50	-	50	mV	FCO
Max. output voltage	$V_{FCH}$	0.2	0.5	-	V	FCO
Min. output voltage	$V_{FCL}$	-	-0.5	-0.2	V	FCO
PCO						
L-level output voltage	$V_{PCH}$	-	-1.0	-0.6	V	PCO
H-level output voltage	$V_{PCL}$	0.6	1.0	-	V	PCO
Audio DAC						
Distortion rate	THD	-	0.01	-	%	LDACO,RDACO,0dB 1kHz sine
Dynamic range	DR	-	90	-	dB	LDACO,RDACO,-60dB 1kHz sine
S/N ratio	S/N	-	96	-	dB	LDACO,RDACO
Max. output level	$V_{SMAX}$	0.75	0.85	0.95	$V_{rms}$	LDACO,RDACO,0dB 1kHz sine
EFM comparator						
Threshold level	$V_{EFM}$	-200	-	200	mV	RFI,ANA_MONI0,A12
Servo ADC						
Offset voltage	$V_{ADOF}$	-140	-	140	mV	ANA_MONI0,ANA_MONI1
Max. conversion level	$V_{ADH}$	1.0	1.2	1.4	V	ANA_MONI0,ANA_MONI1
Min. conversion level	$V_{ADL}$	-1.4	-1.2	-1.0	V	ANA_MONI0,ANA_MONI1
Servo DAC						
Offset voltage	$V_{DAOF}$	-80	-	80	mV	FDOUT,TDOUT,SDOUT,CLVOUT
Max. output voltage	$V_{DAH}$	0.8	1.2	-	V	FDOUT,TDOUT,SDOUT,CLVOUT
Min. output voltage	$V_{DAL}$	-	-1.2	-0.8	V	FDOUT,TDOUT,SDOUT,CLVOUT
Bias amplifier						
Max. output current	$I_{BO}$	-	$\pm 1.5$	-	mA	VBIAS and BIAS fluctuation to be 200mV MAX.

○ Electrical Characteristics (Analog system 2/2)

$V_{DD}=3.0V$ ,  $V_{CORE}=1.5V$  (Unless otherwise specified  $T_a = 25^{\circ}C$ ,  $R_L=10k\Omega$ , standard  $V_C$ )

Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
<b>RF amplifier</b>						
Offset voltage	$V_{RFOF}$	-	0	-	mV	AC,BD,EQO
Max. output voltage	$V_{RFH}$	1.0	1.2	-	V	AC,BD,EQO
Min. output voltage	$V_{RFL}$	-	-1.3	-1.1	V	AC,BD,EQO
<b>FE amplifier</b>						
Offset voltage	$V_{FEOF}$	-	0	-	mV	AC,BD,ANA_MONI0,ANA_MONI1
Max. output voltage	$V_{FEH}$	1.0	1.4	-	V	AC,BD,ANA_MONI0,ANA_MONI1
Min. output voltage	$V_{FEL}$	-	-1.4	-1.0	V	AC,BD,ANA_MONI0,ANA_MONI1
<b>TE amplifier</b>						
Offset voltage	$V_{TEOF}$	-	70	-	mV	E,F,ANA_MONI0,ANA_MONI1
Max. output voltage	$V_{TEH}$	1.0	1.4	-	V	E,F,ANA_MONI0,ANA_MONI1
Min. output voltage	$V_{TEL}$	-	-1.4	-1.0	V	E,F,ANA_MONI0,ANA_MONI1
<b>Asymmetric amplifier</b>						
Offset voltage	$V_{ASYOF}$	-	0	-	mV	ASY= $V_C$ ,RFI,ANA_MONI0(ASY_TEST)
Max. output voltage	$V_{ASYH}$	1.0	1.4	-	V	ASY,RFI,ANA_MONI0(ASY_TEST)
Min. output voltage	$V_{ASYL}$	-	-1.4	-1.1	V	ASY,RFI,ANA_MONI0(ASY_TEST)
<b>APC</b>						
Output voltage1	$V_{APC1}$	2.4	2.8	-	V	PD="H",LD,ANA_MONI0(APCREF)
Output voltage2	$V_{APC2}$	-	0.1	0.5	V	PD="L",LD,ANA_MONI0(APCREF)
Max. reference voltage	$V_{APCH}$	-	220	-	mV	PD,LD,ANA_MONI0(APCREF)
Min. reference voltage	$V_{APCL}$	-	145	-	mV	PD,LD,ANA_MONI0(APCREF)

○ Package Outline, Appearance marking diagram    ○ Block diagram



The address bus and the data bus of CPU are not opened outside.  
 (Can't access the external memory as a CPU)  
 The bit width of ALU is 4 bits.

VQFP100 (UNIT : mm)

○ Description of Terminal

No.	Name	Description of terminals
1	AVDD1	Analog power supply
2	AC	A + C voltage input
3	BD	B + D voltage input
4	VBIAS	Bias level (VDD/2)
5	AGND1	Analog GND
6	E	E voltage input
7	F	F voltage input
8	PD	Photo detector input
9	LD	Laser drive output
10	ASY	Asymmetric correction
11	PCO	PCO output
12	FCO	FCO-DAC output
13	FDOUT	Focus drive output
14	TDOUT	Tracking drive output
15	SDOUT	Sled drive output
16	CLVOUT	CLV drive output
17	CLK88	Clock output for driver IC
18	ADC0	Analog data input
19	ADC1	Analog data input
20	ADC2	Analog data input
21	ADC3	Analog data input
22	COM0	LCD common output
23	COM1	LCD common output
24	COM2	LCD common output
25	DGND1	Digital GND
26	DVDD1	I/O Digital power supply
27	COM3	LCD common output
28	SEG00	LCD segment output
29	SEG01	LCD segment output
30	SEG02	LCD segment output
31	SEG03	LCD segment output
32	SEG04	LCD segment output
33	SEG05	LCD segment output
34	SEG06	LCD segment output
35	SEG07	LCD segment output
36	SEG08	LCD segment output
37	SEG09	LCD segment output
38	SEG10	LCD segment output
39	SEG11	LCD segment output
40	SEG12	LCD segment output
41	SEG13	LCD segment output
42	DVDD_CORE1	Internal digital power supply
43	P00	4-bit parallel output
44	P01	4-bit parallel output
45	P02	4-bit parallel output
46	P03	4-bit parallel output
47	P10	Parallel input
48	P11	Parallel input
49	SEG18	LCD segment output
50	DGND2	Digital GND

No.	Name	Description of terminals
51	DVDD2	I/O Digital power supply
52	RCLK	Reference clock output
53	RCKE	Clock enable output
54	RESETB	"L" → reset condition
55	A13/P20	Address output
56	A12/P21	Address output
57	A11/PWC	Address output
58	A10/AP	Address output
59	A09	Address output
60	A08	Address output
61	A07	Address output
62	A06	Address output
63	A05	Address output
64	A04	Address output
65	A03	Address output
66	A02	Address output
67	A01	Address output
68	A00	Address output
69	RASX	Row address strobe signal
70	CASX	Column address strobe signal
71	WEX	Write enable output
72	LQDM	Lower data mask enable signal
73	UDQM	Upper data mask enable signal
74	DQ07	Data input/output
75	DQ06	Data input/output
76	DQ05	Data input/output
77	DQ04	Data input/output
78	DQ03	Data input/output
79	DQ02	Data input/output
80	DQ01	Data input/output
81	DQ00	Data input/output
82	DVDD_CORE2	Internal digital power supply
83	FLAG0	Various flag output
84	YFLAG	Writing stop signal for DRAM
85	DVDD3	I/O Digital power supply
86	XI	X'tal connecting (input) terminal
87	XO	X'tal connecting terminal
88	DGND3	Digital GND
89	TEST	Test signal input
90	AGND2	Audio system analog GND
91	LDACO	Audio Lch output
92	VCDAC	Audio reference voltage
93	RDACO	Audio Rch output
94	AVDD2	Audio analog power supply
95	AD_MONI0	Monitor signal output
96	AD_MONI1	Monitor signal output
97	ANA_MONI0	Analog monitor signal output
98	ANA_MONI1	Analog monitor signal output
99	RF1	RF data re-input terminal
100	EQO	After-RF-equalizer output

○ Cautions

(1) ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur and break mode (open or short) can not be specified if power supply, operating temperature, and those of ABSOLUTE MAXIMUM RATINGS are exceeded. If such a special condition is expected, components for safety such as fuse must be used.

(2) Power Supply

Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

## Appendix

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