

Structure	Silicon monolithic integrated circuit
Product Name	Camera image processor for home electronics and security devices
Type	BU6582GVW
Feature	Built-in JPEG/MPEG Codec, SXGA Camera Module Interface, and QVGA LCD controller interface

• Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage 1 (IO)	VDDIO1	-0.3~+4.2	V
Supply voltage 2 (IO)	VDDIO2	-0.3~+4.2	V
Supply voltage 3 (CORE)	VDD	-0.3~+1.9	V
Power dissipation	PD	380*1, 1000*2	mW
Input voltage 1	VIN1	-0.3~VDDIO1+0.3	V
Input voltage 2	VIN2	-0.3~VDDIO2+0.3	V
Storage temperature range	Tstg	-40~+150	°C

*1 IC only. If exceeding 25°C, 3.8mW should be reduced at the rating 1°C.

*2 When packaging a glass epoxy board of 70*70*1.6mm. If exceeding 25°C, 10.0 mW should be reduced at the rating 1°C.

* Anti radiation design is not provided.

* Operation is not guaranteed.

• Operating conditions (Ta=-30°C~+85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage 1 (IO)	VDDIO1	1.70	1.80	3.15	V
Supply voltage 2 (IO)	VDDIO2	2.55	2.85	3.15	V
Supply voltage 3 (CORE)	VDD	1.45	1.50	1.55	V
Input "H" voltage 1	VIH1	0.8*VDDIO	-	VDDIO+0.3	V
Input "L" voltage 1	VIL1	-0.3	-	0.2*VDDIO	V
Input "H" voltage 2	VIH2	0.85*VDDIO	-	VDDIO+0.3	V
Input "L" voltage 2	VIL2	-0.3	-	0.15*VDDIO	V
Input voltage range	VIN-VDDIO1,2	-0.3	-	VDDIO+0.3	V

* Supply power in the order of VDD -> VDDIO1 -> VDDIO2.

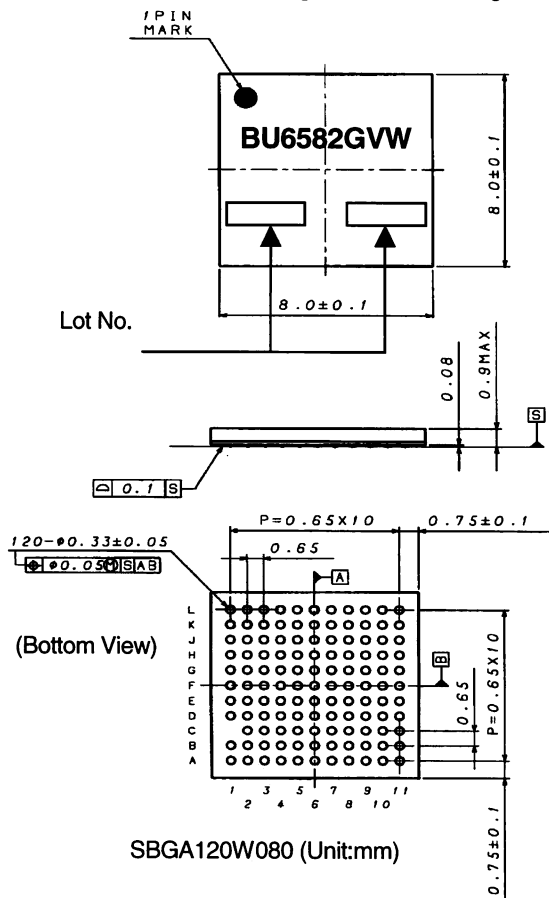
Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

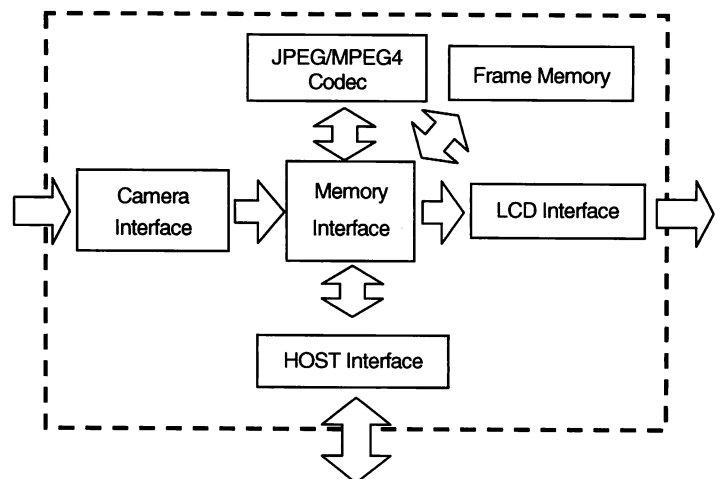
- Electric Characteristics (Unless otherwise specified, VDD=1.50V, VDDIO=2.85V, GND=0.0V, Ta=25°C, F_{IN}=12.0MHz, and F_{SSys} =48.0MHz.)

Parameter	Symbol	Specification			Unit	Conditions
		MIN	TYP	MAX		
Input frequency	F _{IN}	10.0	-	30.0	MHz	XIN(Duty45%~55%)
Internal action frequency 1	F _{HSys}	-	-	66.0	MHz	Internal HCLK, ACLK frequency
Internal action frequency 2	F _{SSys}	-	-	50.0	MHz	Internal SCLK frequency
Internal PLL input frequency	F _{PIN}	2.5	-	7.5	MHz	Internal PLL input frequency
Internal PLL output frequency	F _{POUT}	100	-	200	MHz	Internal PLL output frequency
Action consumption current 1	IDD1	-	15.0	-	mA	At camera ON, LCD display ON In viewer operation
Action consumption current 2	IDD2	-	65.0	-	mA	At camera ON, LCD display ON In MPEG4 encode operation (at HCLK=60MHz)
Static consumption current	IDDst	-	-	150	uA	When suspend mode is set
Input "H" current 1	I _{IH1}	-10	-	10	uA	V _{IH} =VDDIO
Input "H" current 2	I _{IH2}	25	50	100	uA	Pull-down pin, V _{IH} =VDDIO
Input "H" current 3	I _{IH3}	-10	-	10	uA	Pull-up pin, V _{IH} =VDDIO
Input "L" current 1	I _{IL1}	-10	-	10	uA	V _{IL} =GND
Input "L" current 2	I _{IL2}	-10	-	10	uA	Pull-down pin, V _{IL} =GND
Input "L" current 3	I _{IL3}	-160	-80	-25	uA	Pull-up pin, V _{IL} =GND
Input "H" voltage 1	V _{IH1}	VDDIO *0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O pin)
Input "L" voltage 1	V _{IL1}	-0.3	-	VDDIO *0.2	V	Normal input (including input mode of I/O pin)
Input "H" voltage 2	V _{IH2}	VDDIO *0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Input "L" voltage 2	V _{IL2}	-0.3	-	VDDIO *0.15	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Hysteresis voltage width	V _{hys}	-	0.7	-	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Output "H" voltage 1	V _{OH1}	VDDIO -0.4	-	VDDIO	V	I _{OH1} =1.0mA(DC) (Including output mode of I/O pin)
Output "L" voltage 1	V _{OL1}	0.0	-	0.4	V	I _{OL1} =1.0mA(DC) (Including output mode of I/O pin))
Output "H" voltage 2	V _{OH2}	VDDIO -0.4	-	VDDIO	V	I _{OH2} =1.0mA(DC), XOUT pin
Output "L" voltage 2	V _{OL2}	0.0	-	0.4	V	I _{OL2} =1.0mA(DC), XOUT pin

- External Dimensional Drawing and Mark Drawing



- Block Diagram



• Land No. and Pin Name

Land No.	Pin Name
K3	A1
K1	A2
K8	CAMCKI
J7	CAMCKO
K5	CAMD0
L5	CAMD1
K6	CAMD2
L6	CAMD3
K7	CAMD4
J6	CAMD5
F8	CAMD6
G8	CAMD7
L4	CAMHS
J4	CAMVS
H5	CSB
H2	D0
H4	D1
J2	D2
J1	D3
H3	D4
G4	D5
G3	D6
G1	D7
E2	D8
E3	D9
D1	D10
D2	D11
D3	D12
C2	D13
B1	D14
B2	D15
H7	GIO2/KEY2
K4	INT
H11	KEY0
C6	KEY1
D11	LCDA0
H9	LCDCS1B
H10	LCDCS2B
D10	LCDD0
C10	LCDD1

Land No.	Pin Name
B11	LCDD2
E9	LCDD3
E8	LCDD4
D9	LCDD5
C9	LCDD6/SCL
A9	LCDD7/SI
A7	LCDD8
C7	LCDD9
A6	LCDD10
B7	LCDD11
A5	LCDD12
D6	LCDD13
A4	LCDD14
B5	LCDD15
G11	LCDD16
A8	LCDD17
G9	LCDRDB
F10	LCDWRB
K10	LEDCNT/GIO1
C5	PWM0/GIO0
K11	PWM1/GIO3
J8	PWM2/GIO4
J9	PWM3/GIO5
J3	RDB
B3	RESETB
H8	SDA
K9	SDC
H1	SGIO0
F4	SGIO1
F2	SGIO2
E4	SGIO3
E10	SGIO4
D8	SGIO5
B9	SGIO6
E11	SGIO7
F11	SGIO8
G7	SGIO9
G6	SGIO10
F6	SGIO11
C8	TEST

Land No.	Pin Name
J10	VD/GIO6
K2	WRB
D4	XIN
C4	XOUT
A3	VDD
A10	
F1	
G10	
L3	
L10	VDDIO1
B4	
C3	
L2	VDDIO2
C11	
D7	
J5	
L8	GND
A2	
B6	
B8	
B10	
E1	
F7	
F9	
G2	
G5	
H6	N.C.
J11	
L9	
A1	
A11	
D5	
E5	
E6	
E7	
F3	
F5	
L1	
L7	
L11	

• Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.

In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

Appendix

Notes

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