

**Structure** Silicon monolithic integrated circuit  
**Product Name** 3D surround & Audio LSI for cellular phone  
**Product No.** **BU7893GU**  
**Features** 3D surround functionality, Equalizer functionality (3 Band), On-chip audio path.

○Absolute Maximum Ratings(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating	Unit	Remarks
Analog supply voltage	AVDD	-0.3 ~ 4.5	V	AVDD
Digital I/O supply voltage	DVDDIO	-0.3 ~ 4.5	V	DVDD_IO
Digital CORE supply voltage	DVDDCO	-0.3 ~ 2.5	V	DVDD_CORE
Digital input pin 1	Vtdi1	DVSS-0.3 ~ DVDD_IO+0.3	V	
Digital input pin 2	Vtdi2	DVSS-0.3 ~ DVDD_CORE+0.3	V	CLKI (*2)
Input current	Iin	-10 ~ 10	uA	
Voltage applied to analog pin	Vta	AVSS-0.3 ~ AVDD+0.3	V	
Allowable dissipation	Pd	700 (*1)	mW	
Operating temperature range	Topr	-30 ~ 85	°C	
Storage temperature range	Tstg	-50 ~ 125	°C	

(\*1) Note: Reduce to 7.0mW/°C when Ta = 25°C or above

(\*2) Note: Applies only to input via coupling capacitor

○Recommended Operating Power Supply Voltage Range(Unless otherwise noted, Ta = 25°C)

Parameter	Symbol	rating			Unit	Remarks
		Min	Typ	Max		
Analog supply voltage	AVDD	2.6	2.8	3.3	V	AVDD
Digital I/O supply voltage	DVDDIO	DVDDCO	1.8	3.3	V	DVDD_IO
Digital CORE supply voltage	DVDDCO	1.62	1.8	1.98	V	DVDD_CORE
Operating temperature range	Topr	-30	25	85	°C	

This chip is not designed to protect itself against radioactive rays.

Status of this document

The English version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

○Electrical Characteristics

(Unless otherwise noted, Ta = 25°C, DVDD\_CORE=1.8V, DVDD\_IO=1.8V, AVDD=2.8V)

Digital input pins fixed at L or H level of DVDD\_IO. VSS all 0V, audio path volume gain all 0dB, no signal.

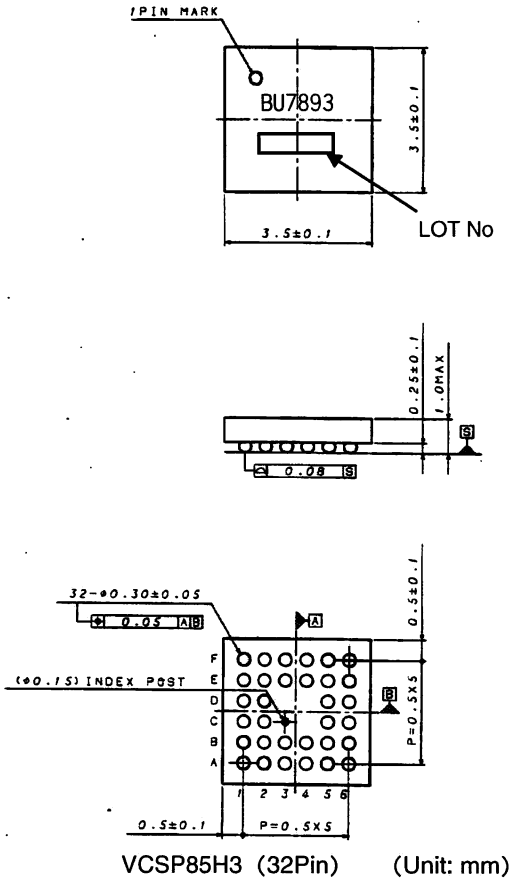
Parameter	Symbol	Rating			Unit	Measurement Conditions
		MIN	TYP	MAX		
DVDD_CORE quiescent current (Core logic block)	ISTCO	-	-	10	μA	standby, CLKI=DVSS
DVDD_IO quiescent current	ISTIO	-	-	5	μA	standby, CLKI=DVSS
AVDD quiescent current	ISTA	-	-	5	μA	standby
DVDD_CORE operating current	IDDCO	-	5	10	mA	
DVDD_IO operating current	IDDIO	-	0.1	1	mA	BCLK, LRCLK = Input mode MCLK = L output
AVDD operating current 1 (Analog melody)	IDDA1	-	1.6	2.8	mA	ANAINL→MIX1→SPOL ANAINR→MIX2→SPOR
AVDD operating current 2 (Digital melody)	IDDA2	-	6.0	10.0	mA	SDI→MIX1→SPOL SDI→MIX2→SPOR TCXOI=19.8MHz, fs=44.1kHz

○Digital block DC Characteristics

Parameter	Symbol	Pins	Measurement Conditions	Rating			Unit
				MIN	TYP	MAX	
L Output Voltage	Vold	All output	Iol=+3mA	0	-	0.30	V
H Output Voltage	Vohd	All output	Ioh=-3mA	DVDD_IO -0.30	-	DVDD	V
L Level Input Voltage 1	Vild1	All input		-0.3	-	DVSS +0.5	V
L Level Input Voltage 2	Vild2	CLKI (*3)		-0.3	-	(*3)	V
H Level Input Voltage 1	Vihd1	All input		DVDD_IO -0.5	-	DVDD_IO +0.3	V
H Level Input Voltage 2	Vihd2	CLKI(*3)		(*3)	-	DVDD_CORE +0.3	V
L Level Input Current	Iild	All input	Pin input voltage is DVSS	-1	-	1	uA
H Level Input Current 1	Iihd1	All input	Pin input voltage is DVDD_IO	-1	-	1	uA
H Level Input Current 2	Iihd2	CLKI(*3)	Pin input voltage is DVDD_CORE	-1	-	1	uA
Output OFF Current	Iozd	Hi-Z pin		-10	-	10	uA

(\*3) Note: When input is via a coupling capacitor, make the coupling capacitor 100 pF and the input amplitude at least 0.5 Vp-p.

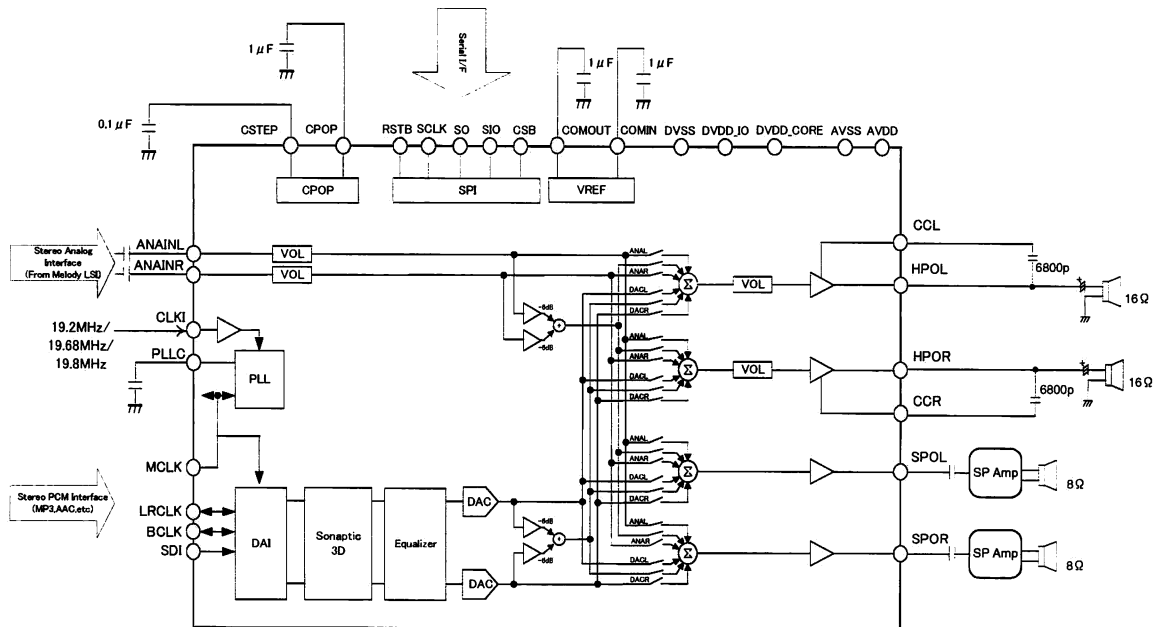
○ External measure and View



○ Pin layout diagram

Pin No.	Pin name	Pin No.	Pin name
E3	AVDD	F3	DVDD_IO
C6	AVSS	B3	DVSS
E6	ANAINL	F2	CLKI
D6	ANAINR	B2	RSTB
A3	HPOL	E1	CSB
A2	HPOR	C1	SCLK
B4	CCL	D1	SIO
B1	CCR	C2	SO
A5	SPOL	E5	SDI
B5	SPOR	F4	BCLK
D5	COMOUT	F5	LRCLK
B6	COMIN	D2	MCLK
A4	CPOP	F6	TEST1
C5	CSTEP	F1	TEST2
E2	PLLCC	A1	TEST3
E4	DVDD_CORE	A6	TEST4

○ Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies have the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents, we called , Technical note, Functional description, Application note.

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