MSDL (Mobile Shrink Data Link) Transceivers for Mobile Phones

Data rate 1350Mbps RGB Interface

BU7963GUW

No.10058EAT05

●Description

BU7963GUW is a differential serial interface connecting mobile phone LCD modules to the host CPU. Unique technology is utilized for lower power consumption and EMI. MSDL minimizes the number of wires required - an important consideration in hinge phones - resulting in greater reliability and design flexibility.

●Features

1) MSDL3 high-speed differential interface with a maximum transfer rate of 1350 Mbps.
2) Compatible with24-bit RGB video mode for LCD controller-to-LCD interface.
3) Pixel clock frequency range from 4 to 45MHz.
4) Depending on the data transfer rate, one, two or three differential data channels can be selected.

●Applications

Serial Interface for LCD Display Interface of Mobile Devices Application.

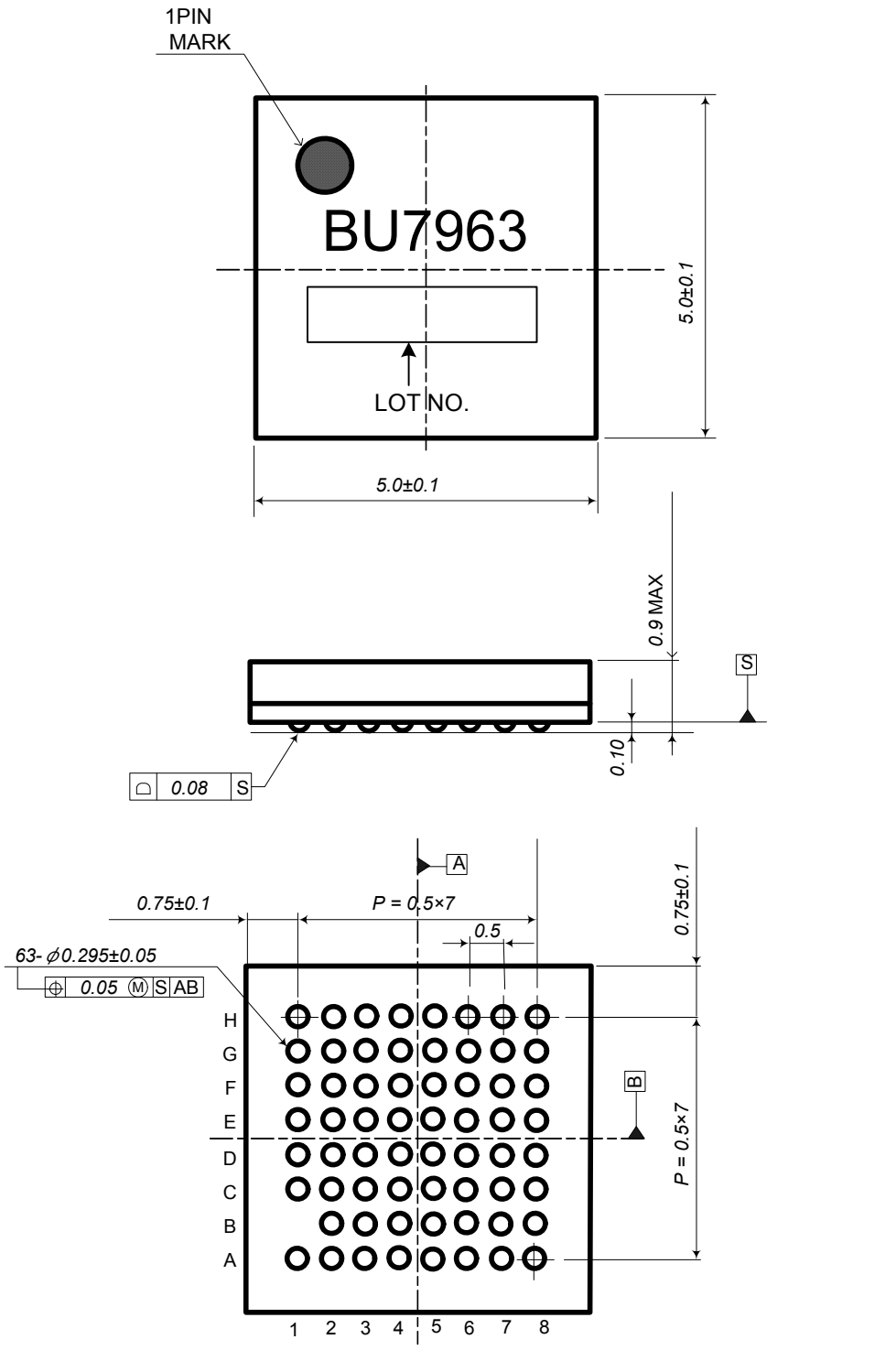
●Absolute Maximum Ratings:

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage	DVDD	-0.3 ~ +2.5	V	-
	MSVDD	-0.3 ~ +2.5	V	-
Input Voltage	VIN	-0.3 ~ MSVDD+0.3	V	I/O terminals of MSVDD line
		-0.3 ~ DVDD+0.3	V	I/O terminals of DVDD line
Output Voltage	VOUT	-0.3 ~ MSVDD+0.3	V	I/O terminals of MSVDD line
		-0.3 ~ DVDD+0.3	V	I/O terminals of DVDD line
Input Current	IIN	-10 ~ +10	mA	-
Output Current	IOUT	-70 ~ +70	mA	-
Preservation Temperature	Tstg	-55 ~ +125	℃	-

●Operating Conditions:

Parameter	Symbol	Ratings			Unit	Conditions
		Min	Typ	Max		
Supply Voltage for DVDD	V_{DVDD}	1.65	1.80	1.95	V	$V_{DVDD} = V_{MSVDD}$
Supply Voltage for MSVDD	V_{MSVDD}	1.65	1.80	1.95	V	
Data Transmission Rate	DR	120	-	450	Mbps/ch	-
Operating Temperature Range	T_{opr}	-30	25	85	℃	-

●Package View



(UNIT:mm)

Fig.1. Package View (VBGA063W050)

●**Block Diagram**

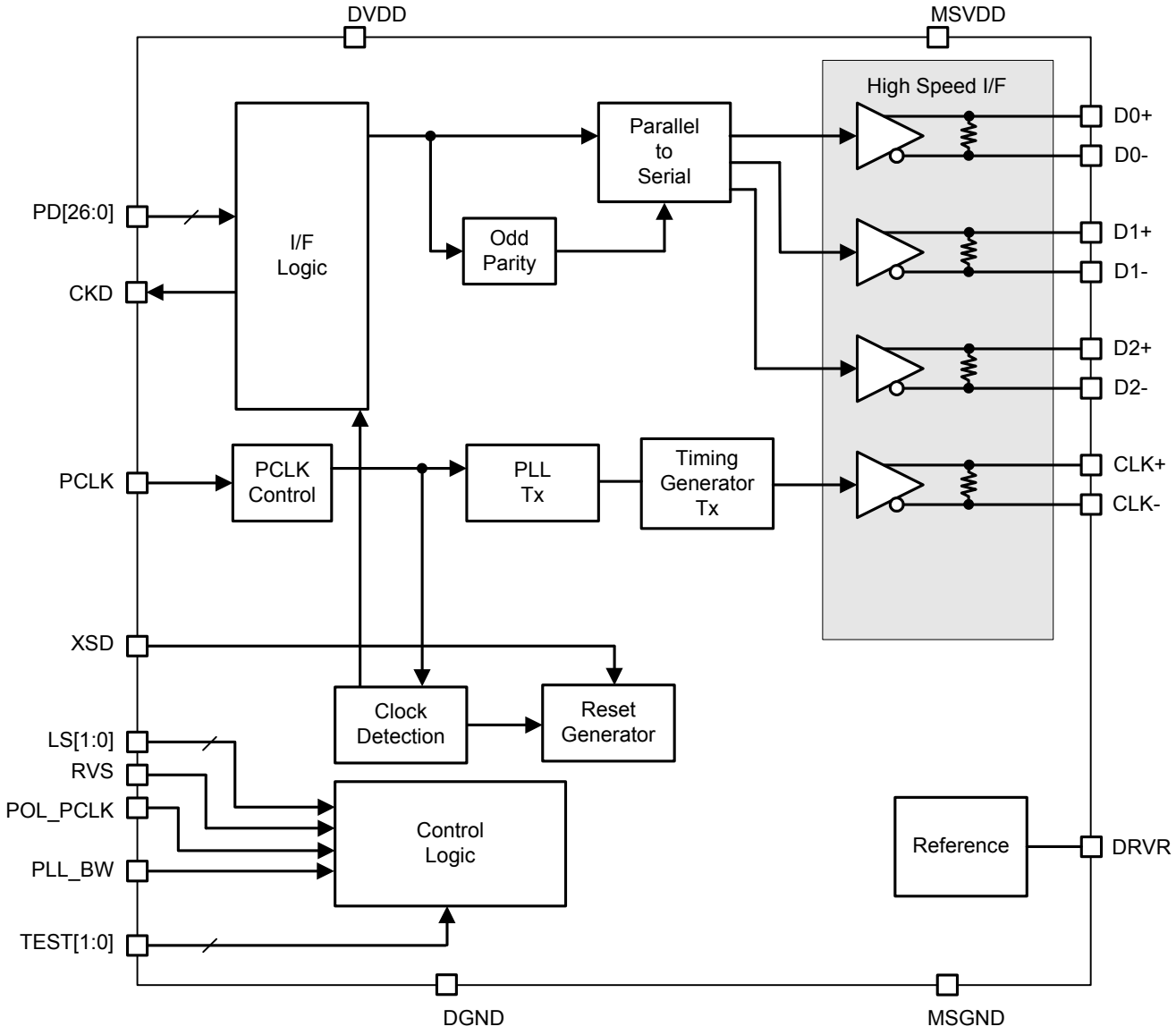


Fig.2. Block Diagram

●**Pin Layout**

	1	2	3	4	5	6	7	8
A	TEST0	PD19	PD17	PD16	PD14	PD13	PD10	CKD
B		PCLK	PD18	PD15	PD12	PD11	PD9	PD8
C	PD22	PD20	PLL_BW	DVDD	N.C.	RVS	PD7	PD6
D	PD23	PD21	N.C.	DGND	DGND	DVDD	PD4	PD5
E	PD25	PD24	DVDD	DGND	MSGND	N.C.	PD1	PD3
F	PD26	LS0	MSVDD	MSGND	MSVDD	N.C.	XSD	PD2
G	LS1	POL_ PCLK	D2+ (D0+)	D1+ (CLK+)	CLK+ (D1+)	D0+ (D2+)	N.C.	PD0
H	N.C.	N.C.	D2- (D0-)	D1- (CLK-)	CLK- (D1-)	D0- (D2-)	DRVR	TEST1

Fig.3. Pin Layout (Top View)

●Pin Functions

Table 1. Power Supply and Ground

Power Supply / Ground : 10-pin		
Name	Width	Functions
DVDD	3	CMOS I/O and logic core power supply.
MSVDD	2	Analog core power supply.
DGND	3	CMOS I/O and logic core ground.
MSGND	2	Analog core ground.

Table 2. MSDL3

High-Speed Serial Interface 8-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
CLK+	1	Analog	O	CLK+ pin When RVS = 'L' : CLK+ When RVS = 'H' : D1+	Hi-Z	D
CLK-	1	Analog	O	CLK- pin When RVS = 'L' : CLK- When RVS = 'H' : D1-	Hi-Z	D
D0+	1	Analog	O	D0+ pin When RVS = 'L' : D0+ When RVS = 'H' : D2+	Hi-Z	D
D0-	1	Analog	O	D0- pin When RVS = 'L' : D0- When RVS = 'H' : D2-	Hi-Z	D
D1+	1	Analog	O	D1+ pin When RVS = 'L' : D1+ When RVS = 'H' : CLK+	Hi-Z	D
D1-	1	Analog	O	D1- pin When RVS = 'L' : D1- When RVS = 'H' : CLK-	Hi-Z	D
D2+	1	Analog	O	D2+ pin When RVS = 'L' : D2+ When RVS = 'H' : D0+	Hi-Z	D
D2-	1	Analog	O	D2- pin When RVS = 'L' : D2- When RVS = 'H' : D0-	Hi-Z	D

Table 3. Analog

Analog 1-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
DRVR	1	Analog	-	10kΩ±5% register should be connected between DRVR and MSGND.	-	D

Table 4. Parallel Data Interface

Parallel Data Interface 29-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
PCLK	1	CMOS	I	PCLK interface.	Input	A
PD[26:0]	27	CMOS	I	Parallel data interface.	Input	A
CKD	1	CMOS	O	Output of PCLK detection result. 'L': clock stop. 'H': clock detect.	'L'	C

Table 5. Control

Control 8-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
XSD	1	CMOS	I	Shutdown pin. 'L': shutdown. 'H': normal operation.	Input	A
LS0	1	CMOS	I	Selection of the number of data channel and the data format. ∗ Refer to "Selection of the number of MSDL3 channels". ∗ Set the same number of data channel between the TX device and the RX device.	Input	A
LS1	1					
RVS	1	CMOS	I	Selection of MSDL3 pins assignment. 'L': Default matrix. 'H': Flipped matrix.	Input	A
PLL_BW	1	CMOS	I	Selection of PLL bandwidth.	Input	A
POL_PCLK	1	CMOS	I	Selection of input clock polarity. 'L': sample parallel data at falling. 'H': sample parallel data at rising.	Input	A
TEST0	1	Pull down	I	Test mode pin. 'L': normal mode. 'H': test mode. Must be 'L.'	Input	B
TEST1	1					B

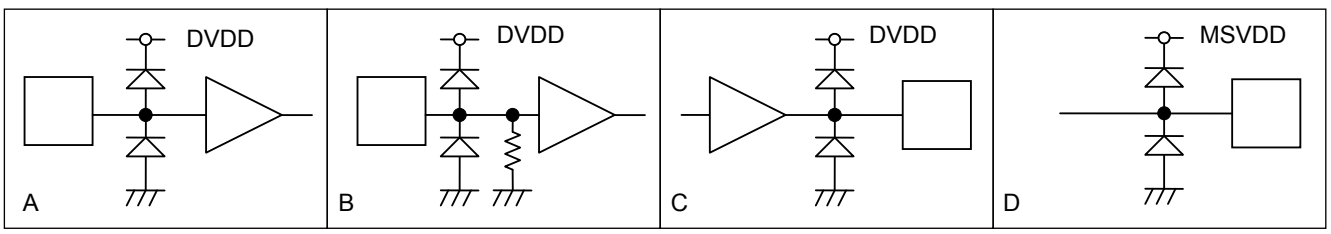


Fig.4. Equivalent Schematics

●Operation Control

MSDL3 Channel Count Selection

Pin LS is used to control the high-speed data channel count and data format. The LS pin settings (i.e., high-speed data channel count, data format) should be the same between the transmitting and receiving devices (the BU7963GUW and BU7964GUW, respectively). Table 6 shows the PCLK input frequency ranges and transmission data rate ranges for the LS pin settings.

Table 6. The Range of The Transmission Data rate

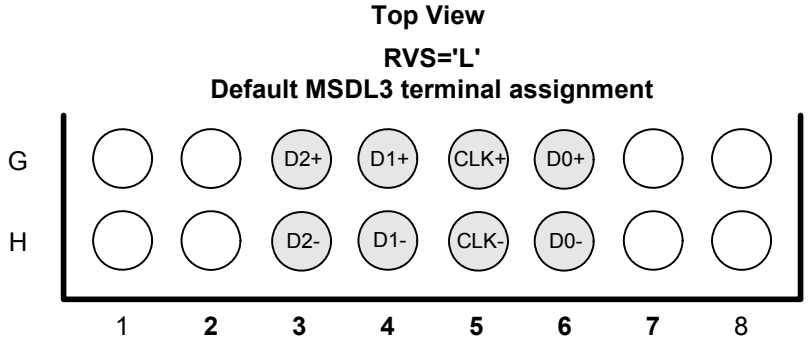
LS1	LS0	The Number of Data Channel	The Range of PCLK Input Frequency [MHz]	The Range of The Data Transmission Rate [Mbits/sec]
'L'	'L'	1-channel	4.0-15.0	120-450
'L'	'H'	2-channel	8.0-30.0	240-900
'H'	'L'	3-channel	12.0-45.0	360-1350
'H'	'H'	Inhibit setting.		

MSDL3 Pin Assignment

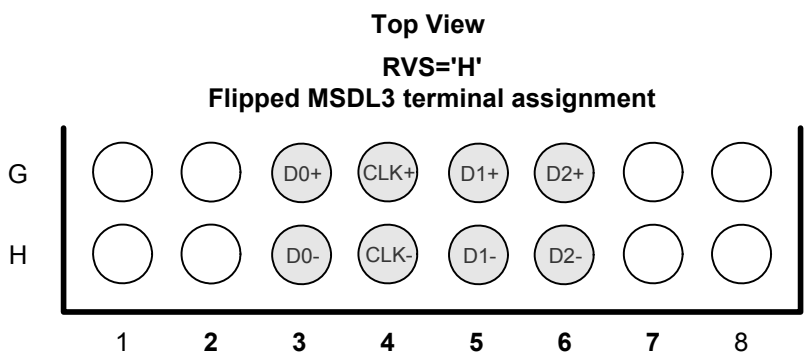
RVS determines the assignment of MSDL3 pins, CLK+ / CLK−, D0+ / D0−, D1+ / D1− and D2+ / D2-. Only the MSDL3 high-speed signaling pins are affected by RVS, while pin assignment of other functions does not change. User can select the assignment from 'straight' (default) and 'flipped' assignment in order to minimize channel-to-channel skew in PWB design. Table 7 shows the MSDL3 pin assignment, and Fig.5 shows the 'straight' and 'flipped'

Table 7. MSDL3 Pin Assignment

RVS	MSDL3 Pin Assignment
'L'	'Straight' (default matrix)
'H'	'Flipped'



(a) 'Straight' Pin Assignment



(b) 'Flipped' Pin Assignment

Fig.5. MSDL3 Pin Assignment

PCLK Polarity Selection

BU7963GUW controls PCLK input polarity by POL_PCLK setting. Table 8 shows PCLK input polarity.

Table 8. PCLK Polarity Selection

POL_PCLK	Parallel Data Capturing Polarity
'L'	Capture parallel data at falling edge.
'H' (default)	Capture parallel data at rising edge.

PLL Bandwidth Selection

BU7963GUW controls the range of the CLK+ / CLK− input frequency (= PCLK output frequency) by the setting of the data format (LS1, and LS0) of the high-speed data channel and the bandwidth setting of PLL_BW.

Table 9. PLL_BW Setting

LS1	LS0	PLL_BW	CLK+ / CLK− Frequency Range [MHz] (PCLK Input Frequency)	
			Min	Max
'L'	'L'	'L'	4	8
'L'	'L'	'H'	7	15
'L'	'H'	'L'	8	16
'L'	'H'	'H'	14	30
'H'	'L'	'L'	12	24
'H'	'L'	'H'	21	45

●Power Modes

BU7963GUW has three power modes.

1) Shutdown Mode
BU7963GUW goes to Shutdown Mode when XSD = 'L'. All logic circuits are initialized in the Shutdown Mode. All high-speed signaling channels are disabled, and the outputs keep Hi-Z status.

2) Standby Mode
BU7963GUW goes to Standby Mode when XSD = 'H' and PCLK is not provided. All high-speed signaling channel outputs keep Hi-Z status. BU7963GUW is monitoring whether PCLK input is running or not and the link switches to Active Mode when PCLK running is detected.

3) Active Mode
BU7963GUW goes to Active Mode when XSD = 'H' and PCLK is running. All high-speed signaling channels are enabled.

Table 10. Power Modes

Power Mode	Input		Operation	
	XSD	PCLK	Functions	MSDL3 Terminals
Shutdown	'L'	Static ('L' or 'H')	Initialized	Disabled (Hi-Z)
Standby	'H'	Static ('L' or 'H')	PCLK detection	Disabled (Hi-Z)
Active	'H'	Clock input is active	PCLK detection Normal operation (P2S conv)	Enabled

4) Power Modes Transition
Fig.6 shows the transition of power modes.

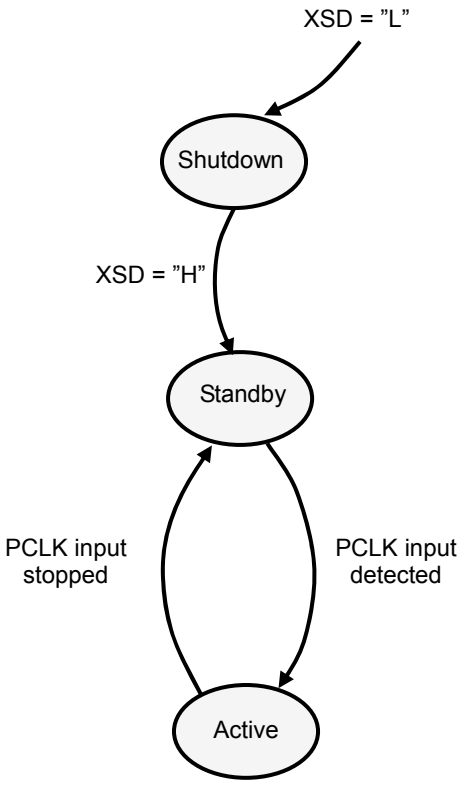


Fig.6. Power Modes Transition

●**High-Speed Data Channel Protocols**

Fig.7, Fig.8 and Fig.9 show high-speed data channel protocols.

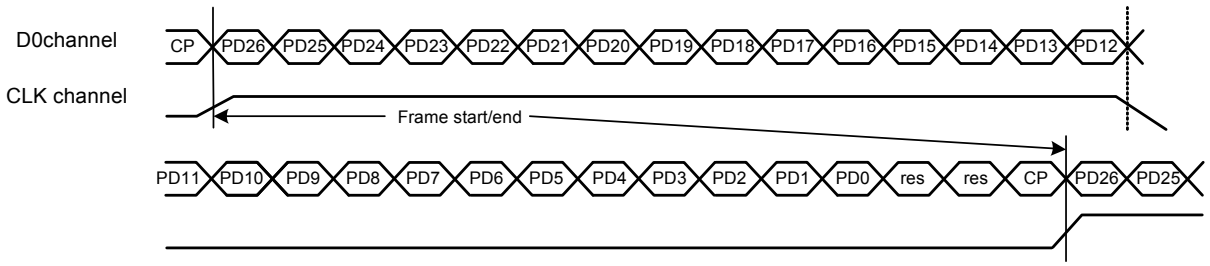


Fig.7. MSDL3 Protocol for 1-channel Data (27-bit)

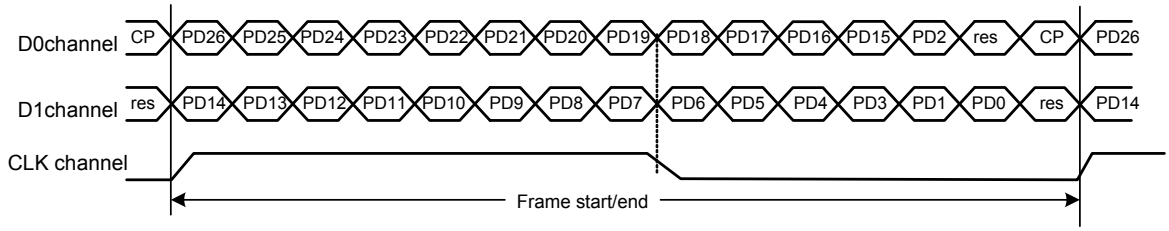


Fig.8. MSDL3 Protocol for 2-channel Data (27-bit)

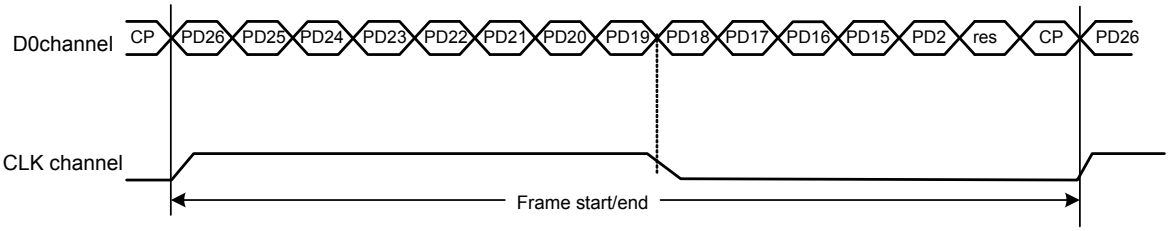


Fig.9. MSDL3 Protocol for 1-channel Data (13-bit)

“res” is reserved bit for the future use, the default state of those is ‘0.’
CP is the parity bit of data payload. BU7961GUW adds an odd parity on CP of the high-speed channel data.

- When the number of ‘H’ bits in parallel data is even, CP bit is ‘H.’
- When the number of ‘H’ bits in parallel data is odd, CP bits is ‘L.’

●Electrical Characteristics

1) DC Characteristics

Table 11. Digital Input / Output DC Characteristics

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
'L' Input Voltage 1	VIL1	DGND	-	0.3 x DVDD	V	PCLK, PD[26:0], LS[1:0], RVS, POL_PCLK, XSD, PLL_BW, TEST[1:0] pin
'H' Input Voltage 1	VIH1	0.7 x DVDD	-	DVDD	V	PCLK, PD[26:0], LS[1:0], RVS, POL_PCLK, PLL_BW, TEST[1:0] pin
'L' Input Current 1	IIL1	-5	-	+5	μA	VIN = DGND
'H' Input Current 1	IIH1	-5	-	+5	μA	VIN = DVDD
'L' Input Current 2	IIL2	-5	-	+5	μA	VIN = MSGND
'H' Input Current 2	IIH2	-5	-	+5	μA	VIN = MSVDD
'L' Output Voltage 1	VOL1	DGND	-	0.3 x DVDD	V	IO = 1mA,CKD pin
'H' Output Voltage 1	VOH1	0.7 x DVDD	-	DVDD	V	IO = -1mA,CKD pin

Table 12 Current Consumption

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	$I_{op\_sht\_rx}$	-	0.2	10	μA	XSD = 'L', IDVDD + IMSVDD
Standby Current	$I_{op\_stb\_rx}$	-	0.2	10	μA	XSD = 'H', IDVDD + IMSVDD
Active Current 1-channel / 27-bit Format	$I_{op\_act\_rx1}$	-	14.0	18.5	mA	LS[1:0] = 'LL,' PLL_BW[1:0] = 'H' DVDD = MSVDD PCLK=15MHz,XSD='H CL=10pF Total operating current (IDVDD + IMSVDD) with PD[26:0] inputs to ggling 0x2AAAAAA and 0x5555555
Active Current 2-channel / 27-bit Format	$I_{op\_act\_rx2}$	-	19.7	25.7	mA	LS[1:0] = 'LH,' PLL_BW[1:0] = 'H' DVDD = MSVDD PCLK=30MHz,XSD='H' CL=10pF Total operating current (IDVDD + IMSVDD) with PD[26:0] inputs to ggling 0x2AAAAAA and 0x5555555
Active Current 3-channel/ 27-bit Format	$I_{op\_act\_rx3}$	-	25.4	32.9	mA	LS[1:0] = 'HL,' PLL_BW[1:0] = 'H' DVDD = MSVDD PCLK=45MHz,XSD='H' CL=10pF Total operating current (IDVDD + IMSVDD) with PD[26:0] inputs to ggling 0x2AAAAAA and 0x5555555

2) AC Characteristics
Parallel Data Input Timing

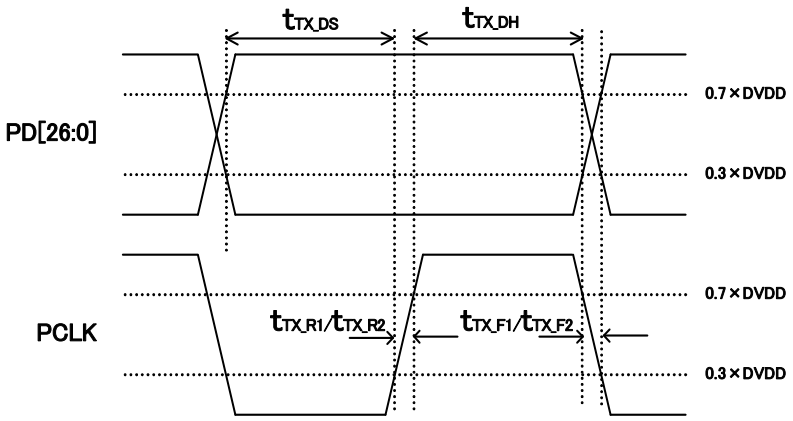


Fig.10 Parallel Data Input AC Timing

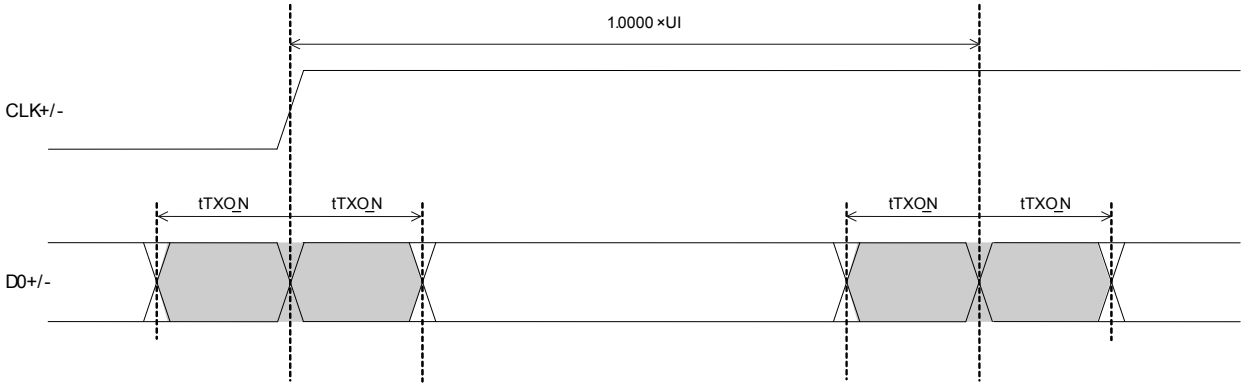
Table 13. Parallel Data Input AC Timing

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
PCLK Input Frequency	f_{TX_PCLK1}	4	-	15	MHz	LS0=L, LS1=L
	f_{TX_PCLK2}	8	-	30	MHz	LS0=H, LS1=L
	f_{TX_PCLK3}	12	-	45	MHz	LS0=L, LS1=H
PCLK Input Duty Cycle	t_{TX_DUTY}	33	-	67	%	
Input Data Setup Time	t_{TX_DS}	5.0	-	-	ns	POL_PCLK=H
Input Data Hold Time	t_{TX_DH}	5.0	-	-	ns	POL_PCLK=H
Input Signal Rise Time 1	t_{TX_R1}	-	-	10	ns	PCLK Frequency≦30MHz
Input Signal Rise Time 2	t_{TX_R2}	-	-	5	ns	PCLK Frequency＞30MHz
Input Signal Fall Time 1	t_{TX_F1}	-	-	10	ns	PCLK Frequency≦30MHz
Input Signal Fall Time 2	t_{TX_F2}	-	-	5	ns	PCLK Frequency＞30MHz

3) Serial Data Input Timing

Fig.11 and Table 14 shows Serial Data Input Timing of BU7963GUW.



UI = (1 cycle time of CLK+/-) / 30
N = Bit position (0 ≦ N ≦ 30)

Fig.11. Serial Data input AC Timing

Table 14. Serial Data input AC Timing

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Output location CLKL+/- of N bit	t_{TXO_N}	-0.1845×UI + UI×N	UI×N	0.1845×UI + UI×N	sec	

4) Power-On / Off Sequence

Power-On Sequence

Fig.12 shows power-on sequence of BU7963GUW.

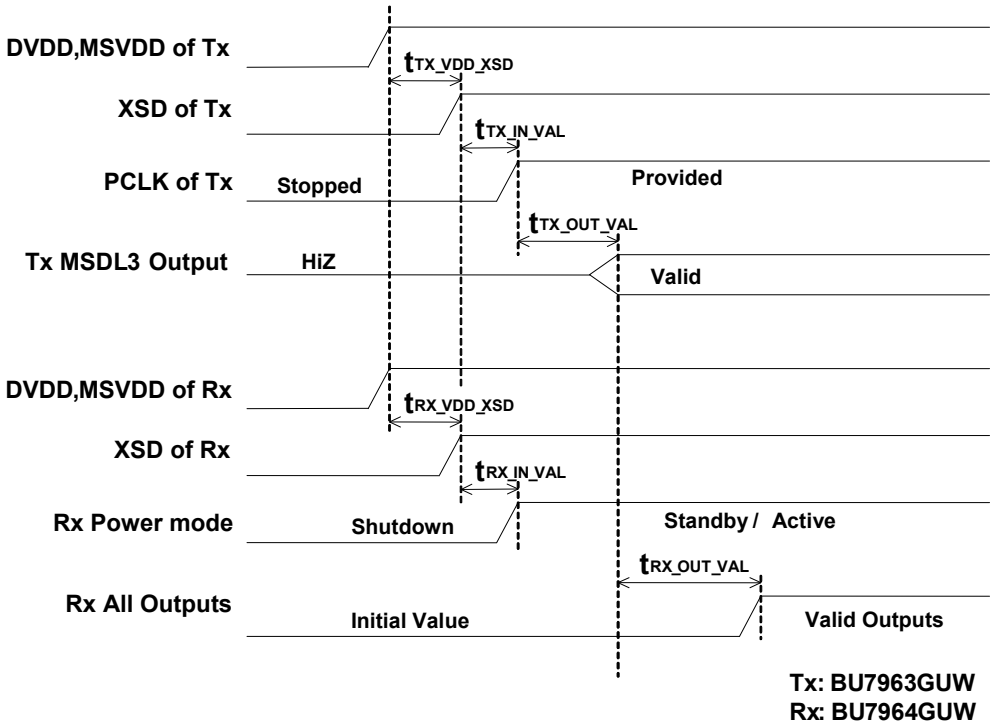


Fig.12. Power-On / Off Sequence

Table 15. Power-On Sequence Timing

Ta=25°C, DVDD=MS VDD=1.80V, and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Core power supply startup time	$t_{TX\_VDD\_IOV}$	0.0	-	2	ms	
Reset Valid After Power Supplied	$t_{TX\_VDD\_XSD}$	10	-	-	µs	
PCLK clock input startup time	$t_{TX\_IN\_VAL}$	10	-	-	µs	
MSDL3 output delay time	$t_{TX\_OUT\_VAL}$	-	-	2	ms	

Power-Off Sequence

Fig.13 shows the power-off sequence of BU7963GUW.

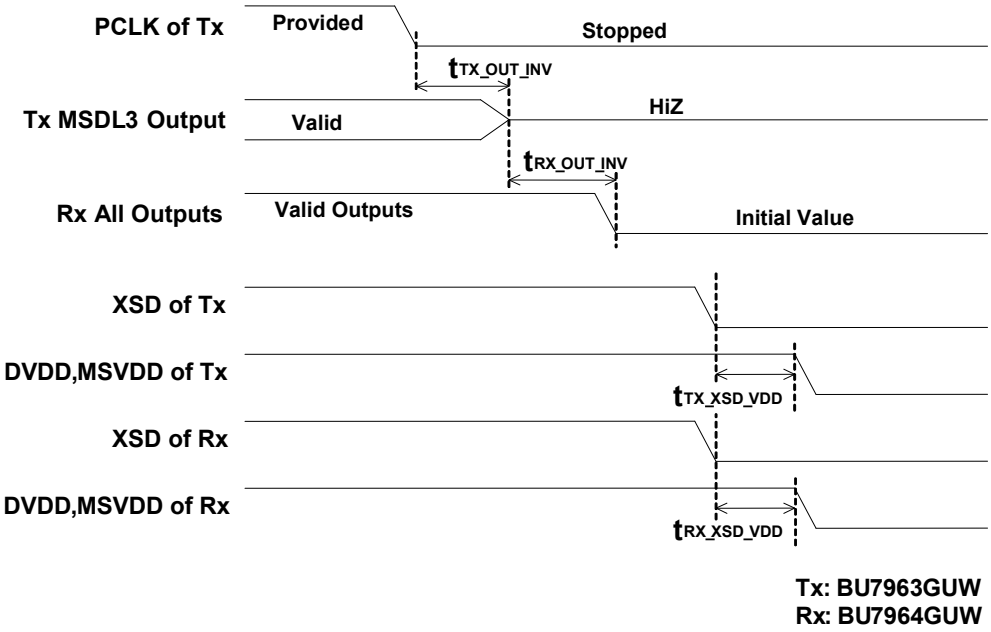


Fig.13. Power-Off Sequence

Table 16. Power-Off Sequence Timing

Ta=25°C, DVDD=MSVDD=1.80V, and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
MSDL3 output delay time	$t_{TX\_OUT\_INV}$	-	-	100	μs	
XSD hold time	$t_{TX\_XSD\_VDD}$	10	-	-	μs	
Core power off time	$t_{TX\_VDD\_IOV}$	0.0	-	2	ms	

Frequency Change Sequence

Fig.14 shows the frequency change sequence of BU7963GUW.

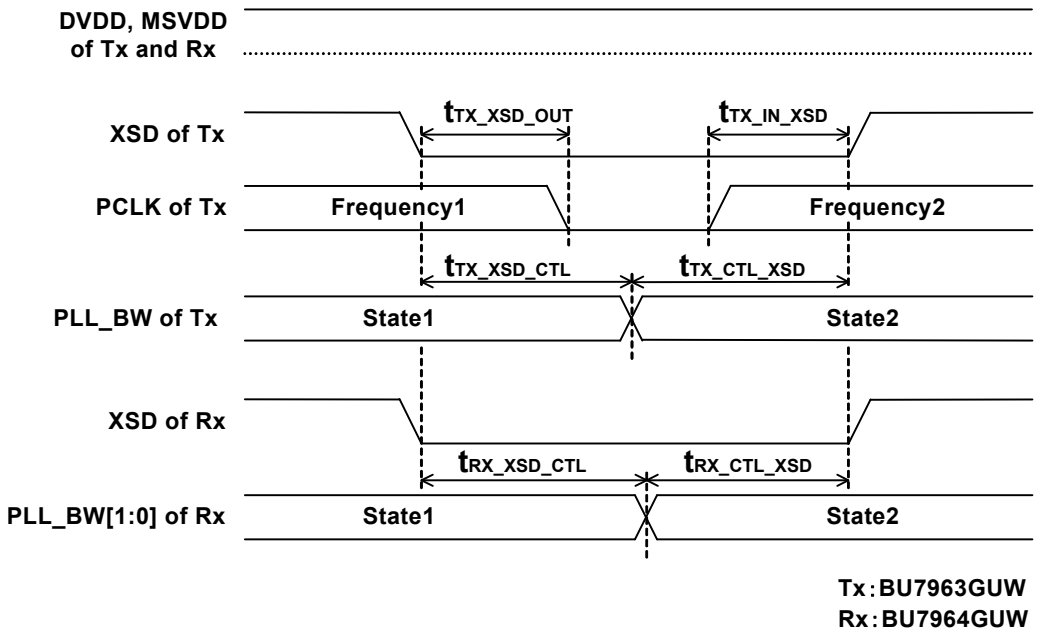


Fig.14. Frequency Change Sequence

Table 17. Frequency Change Sequence

Ta=25°C, DVDD=MSVDD=1.80V, and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
PCLK Clock Input Suspend Time	$t_{TX\_XSD\_OUT}$	1.0	-	-	µs	
PCLK Clock Input Restart Time	$t_{TX\_IN\_XSD}$	1.0	-	-	µs	
Control Signal Hold Time	$t_{TX\_XSD\_CTL}$	2.0	-	-	µs	
Control Signal Setup Time	$t_{TX\_CTL\_XSD}$	2.0	-	-	µs	

●High-speed Channel Characteristic

Table 18. High-speed channel characteristic

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Differential Voltage Range	V_{diff_tx}	100	150	200	mVpp	
Common Mode Voltage Range	V_{cm_tx}	0.8	0.9	1.0	V	
Vdiff_tx Rise Time	t_{r_tx}	200	-	500	ps	
Vdiff_tx Fall Time	t_{f_tx}	200	-	500	ps	
Operating Frequency	f_{opr_tx}	-	-	225	MHz	
TX Hi-Z State Leak Current	I_{LEAK_TX}	-3	-	3	μA	Shutdown mode or standby mode

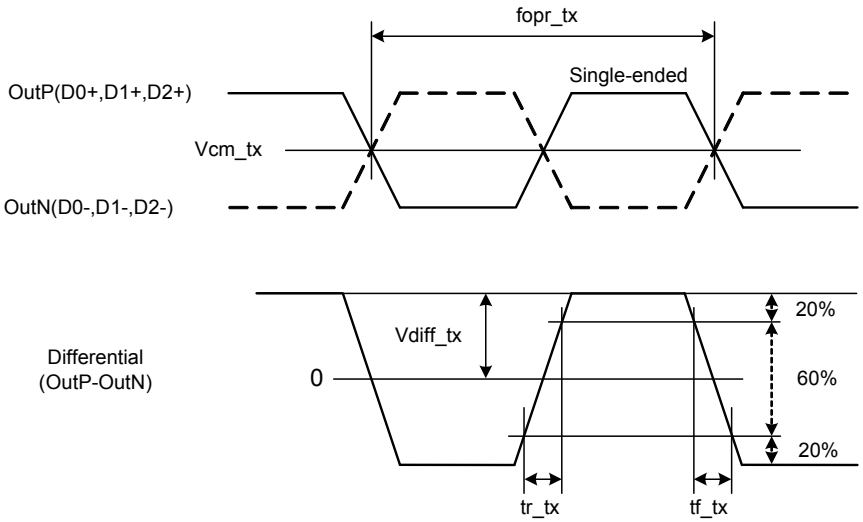


Fig.15. High-Speed Channel Electrical Characteristics

Fig.16 shows high-speed channel equivalent schematic.

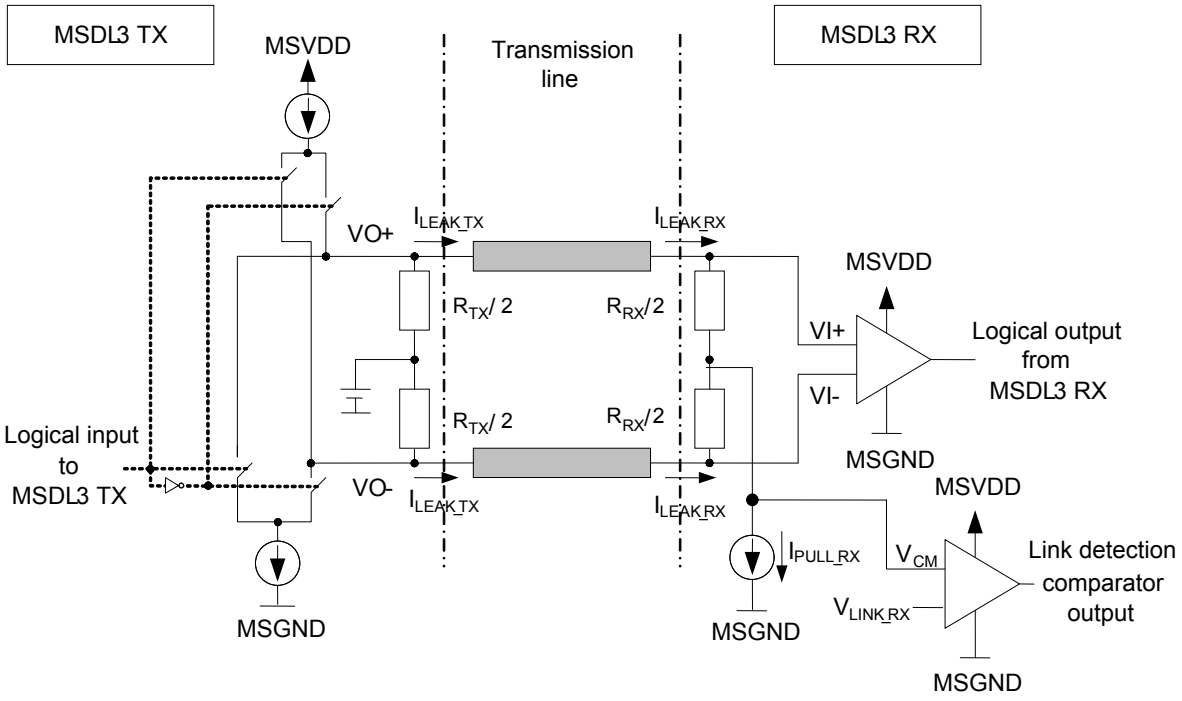


Fig.16. high-speed channel equivalent schematic.

●Application Circuit Example

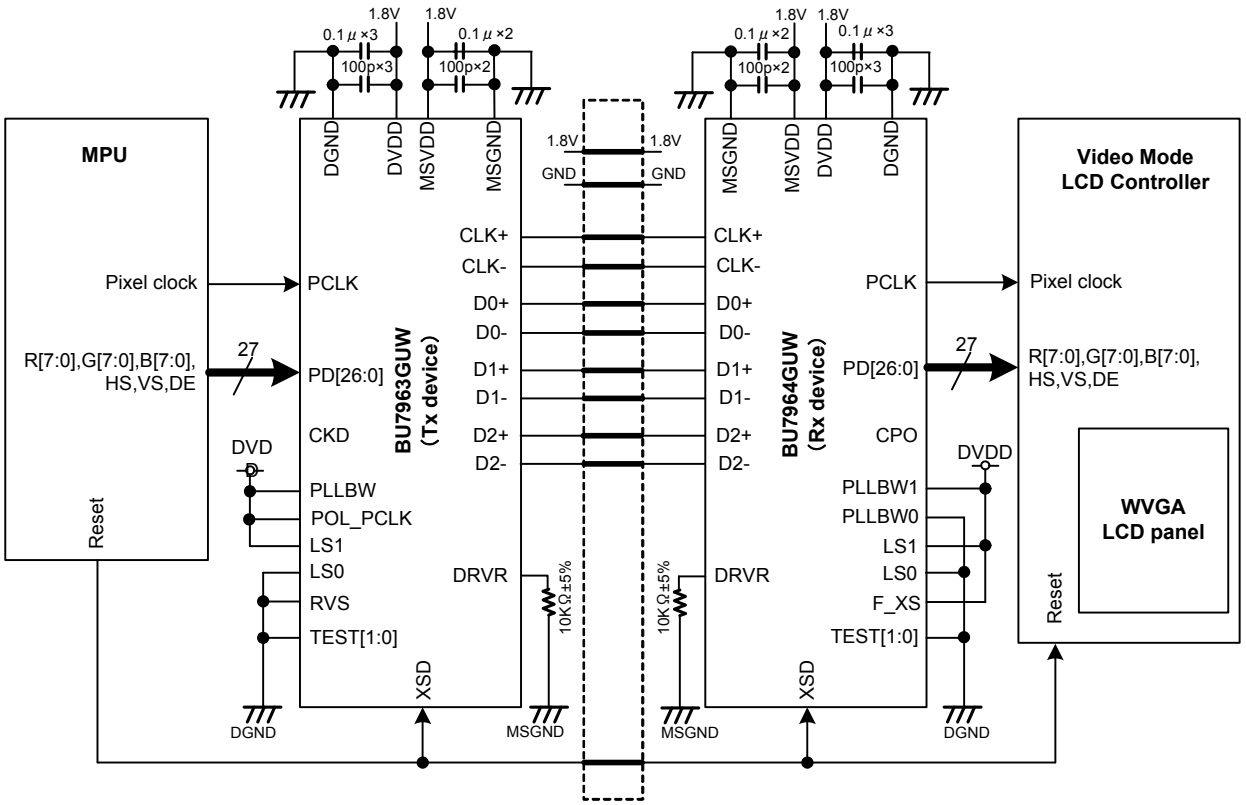


Fig.17. Application circuit

●PCB Layout for MSDL3

The following points should be considered about the wiring for PCB of MSDL3.

- Wire for the PCB wiring pattern of high-speed channel (CLK, D0+/-, D1+/-, D2+/-) as short as possible.
- The PCB wiring for high-speed channel must not use the through-hole.
- Do not bend the wiring for high-speed channel squarely.
- Make the wiring length of each high-speed channel the same length (within 0.5mm).

●Ordering Part Number

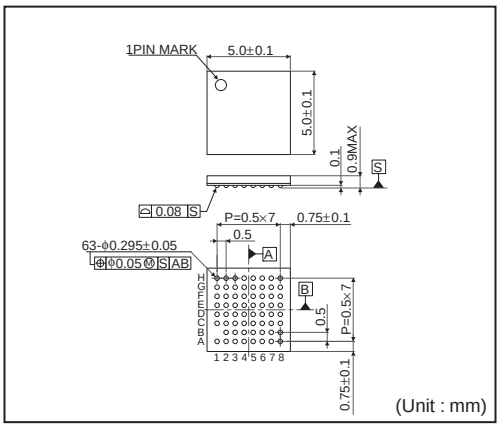
B	U	7	9	6	3	G	U	W	-	E	2

Part No. Part No.

Package
GUW: VBGA063W050

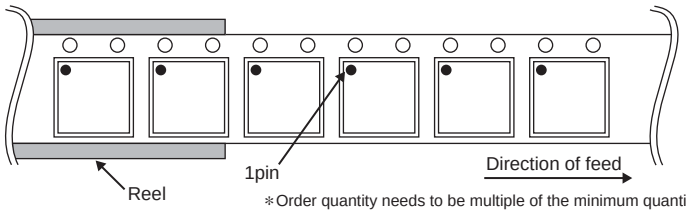
Packaging and forming specification
E2: Embossed tape and reel

VBGA063W050



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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