MSDL (Mobile Shrink Data Link) Transceivers for Mobile Phones

Data rate 1350Mbps RGB Interface

BU7964GUW

No.10058EAT04

●Description

BU7964GUW is a differential serial interface connecting mobile phone LCD modules to the host CPU. Unique technology is utilized for lower power consumption and EMI. MSDL minimizes the number of wires required - an important consideration in hinge phones - resulting in greater reliability and design flexibility.

●Features

1) MSDL3 high-speed differential interface with a maximum transfer rate of 1350 Mbps.
2) Compatible with24-bit RGB video mode for LCD controller-to-LCD interface.
3) Pixel clock frequency range from 4 to 45MHz.
4) Depending on the data transfer rate, either, two or three differential data channels can be selected.

●Applications

Serial Interface for LCD Display Interface of Mobile Devices Application.

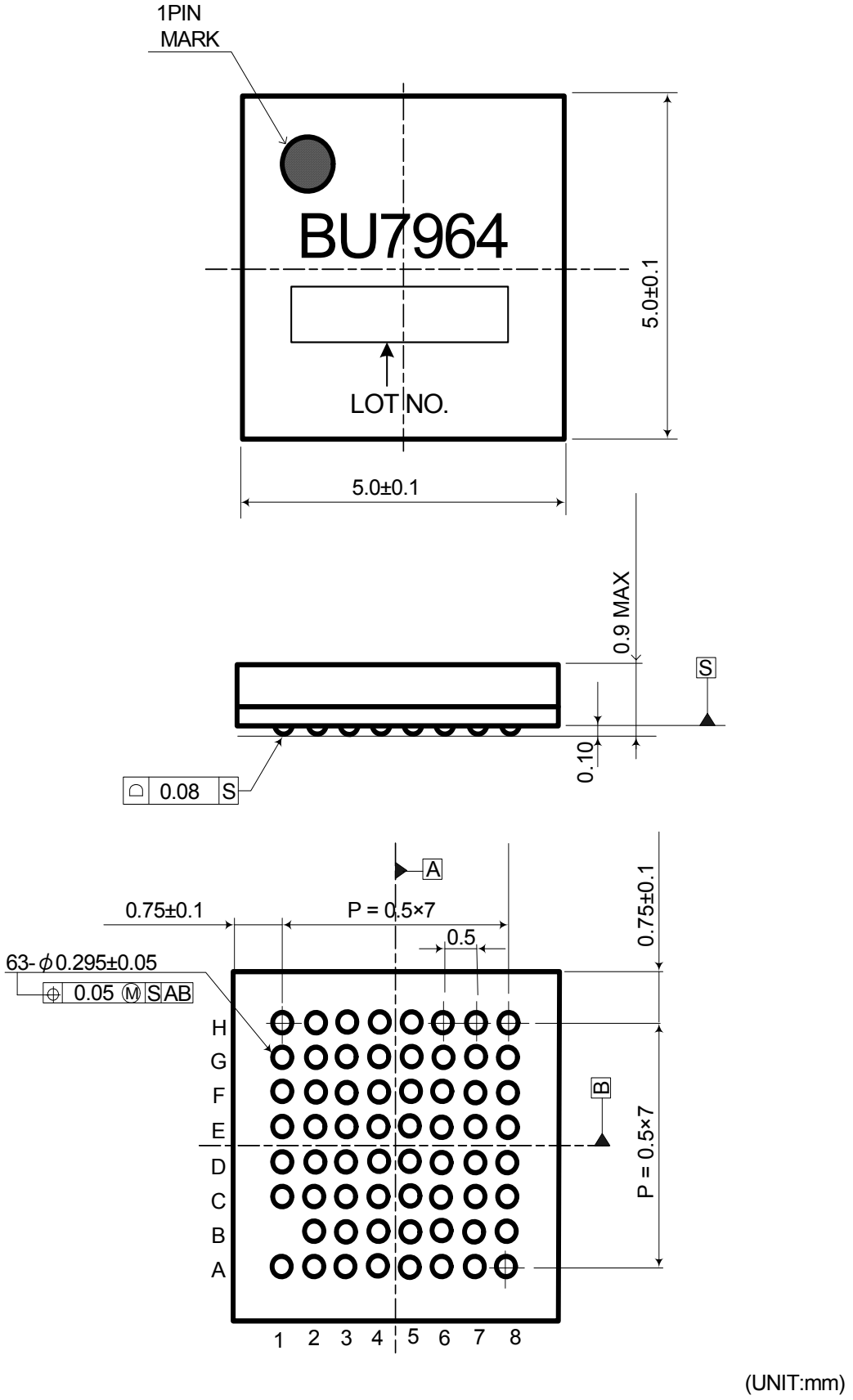
●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage	DVDD	-0.3 ~ +2.5	V	-
	MSVDD	-0.3 ~ +2.5	V	-
Input Voltage	VIN	-0.3 ~ MSVDD+0.3	V	I/O terminals of MSVDD line
		-0.3 ~ DVDD+0.3	V	I/O terminals of DVDD line
Output Voltage	VOUT	-0.3 ~ MSVDD+0.3	V	I/O terminals of MSVDD line
		-0.3 ~ DVDD+0.3	V	I/O terminals of DVDD line
Input Current	IIN	-10 ~ +10	mA	-
Output Current	IOUT	-70 ~ +70	mA	-
Preservation Temperature	Tstg	-55 ~ +125	℃	-

●Operating Conditions

Parameter	Symbol	Ratings			Unit	Conditions
		Min	Typ	Max		
Supply Voltage for DVDD	V_{DVDD}	1.65	1.80	1.95	V	$V_{DVDD} = V_{MSVDD}$
Supply Voltage for MSVDD	V_{MSVDD}	1.65	1.80	1.95	V	
Data Transmission Rate	DR	120	-	450	Mbps/ch	-
Operating Temperature Range	T_{opr}	-30	25	85	℃	-

●Package View



(UNIT:mm)

Fig.1. Package View (VBGA063W50)

●**Block Diagram**

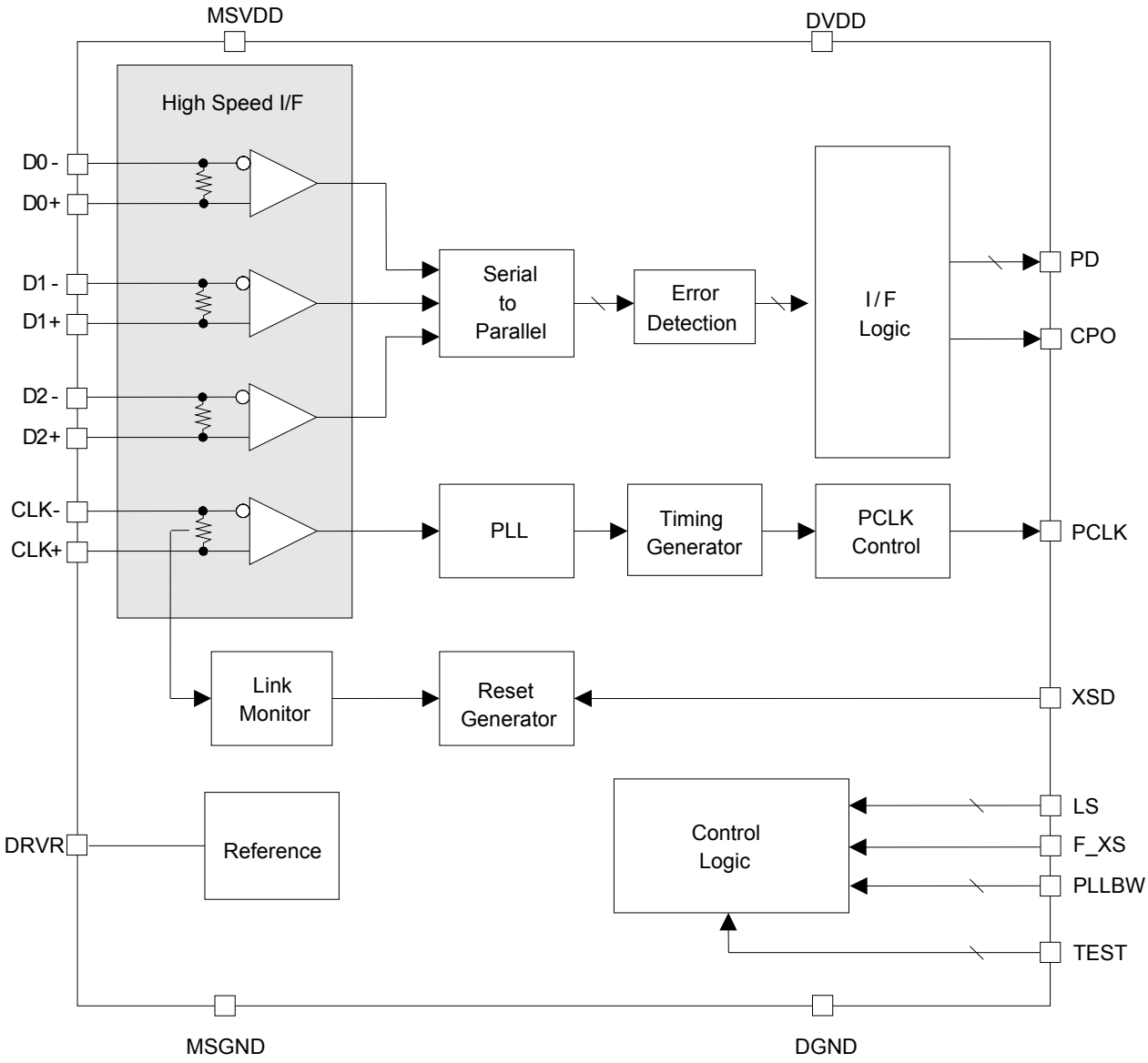


Fig.2. Block Diagram

●**Pin Layout**

	1	2	3	4	5	6	7	8
A	TEST0	PD19	PD17	PD16	PD14	PD13	PD10	CPO
B		PCLK	PD18	PD15	PD12	PD11	PD9	PD8
C	PD22	PD20	PLL_BW0	DVDD	N.C.	F_XS	PD7	PD6
D	PD23	PD21	N.C.	DGND	DGND	DVDD	PD4	PD5
E	PD25	PD24	DVDD	DGND	MSGND	N.C.	PD1	PD3
F	PD26	LS0	MSVDD	MSGND	MSVDD	N.C.	XSD	PD2
G	LS1	PLL_BW1	D2-	D1-	CLK-	D0-	N.C.	PD0
H	N.C.	N.C.	D2+	D1+	CLK+	D0+	DRVR	TEST1

Fig.3. Pin Layout (Top View)

●Pin Functions

Table 1. Power Supply and Ground

Power Supply / Ground: 10-pin		
Name	Width	Functions
DVDD	3	Logic core, CMOS I/O power supply.
MSVDD	2	Analog core power supply.
DGND	3	CMOS I/O and logic core ground.
MSGND	2	Analog core ground.

Table 2. MSDL3

High-Speed Serial Interface: 8-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
CLK+	1	Analog	I	CLK+pin.	Pull Down	D
CLK-	1	Analog	I	CLK-pin.	Pull Down	D
D0+	1	Analog	I	D0+pin.	Pull Down	D
D0-	1	Analog	I	D0-pin.	Pull Down	D
D1+	1	Analog	I	D1+pin.	Pull Down	D
D1-	1	Analog	I	D1-pin.	Pull Down	D
D2+	1	Analog	I	D2+pin.	Pull Down	D
D2-	1	Analog	I	D2-pin.	Pull Down	D

Table 3. Analog

Analog: 1-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
DRVR	1	Analog	-	10kΩ ± 5% register should be connected between DRVR and MSGND.	-	D

Table 4. Parallel Data Interface

Parallel Data Interface: 29-pin						
Name	Width	Level	I/O	Functions	Shutdown	Equivalent Schematic
PCLK	1	CMOS	O	PCLK interface.	‘L’	C
PD[26:0]	27	CMOS	O	Parallel data interface.	‘L’	C
CPO	1	CMOS	O	Parity error toggled output, normally ‘L,’ output is toggled during one PCLK period when a parity error is detected	‘L’	C

Table 5. Control

Control: 8-pin						
Name	**Width**	**Level**	**I/O**	**Functions**	**Shutdown**	**Equivalent Schematic**
XSD	1	CMOS	I	Shutdown pin. 'L': shutdown. 'H': normal operation.	Input	A
LS0	1	CMOS	I	Selection of the number of data channel and the data format. Refer to section 0. * Set the same number of data channel bet wean the TX device and the RX device.	Input	A
LS1	1					
F_XS	1	CMOS	I	Selection of CMOS output rising and falling slope 'L': slow 'H': fast	Input	A
PLL_BW0	1	CMOS	I	Selection of PLL bandwidth.	Input	A
PLL_BW1	1					
TEST0	1	Pull down	I	Test mode pins. 'L': normal mode. 'H': test mode. Must be open or 'L.'	Input	B
TEST1	1					B

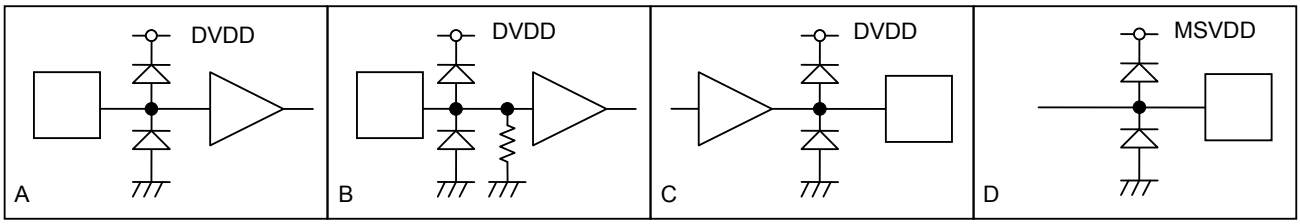


Fig.4. Equivalent Schematics

●Operation Control

MSDL3 Channel Count Selection

Pins LS0 and LS1 are used to control the high-speed data channel count and data format. High-speed data channel count, data format should be the same between the transmitting and receiving devices (the BU7963GUW and BU7964GUW, respectively). Table 6 shows and Receipt Data rate ranges for the LS pin settings.

Table 6. The Range of The Receipt Data rate

LS1	LS0	The Number of Data Channel	The Range of PCLK Input Frequency [MHz]	The Range of The Data Receipt Rate [Mbits/sec]
'L'	'L'	1-channel (27-bit format).	4.0-15.0	120-450
'L'	'H'	2-channel (27-bit format).	8.0-30.0	240-900
'H'	'L'	3-channel (27-bit format).	12.0-45.0	360-1350

CMOS Output Drivability Selection

F_XS determines output drivability of the parallel data interface. Table 7 shows output drivability.

Table 7. Output Drivability

F_XS	Output Drivability
'L'	1mA Type
'H'	3mA Type

PLL Bandwidth Selection

BU7964GUW controls the range of the CLK+ / CLK− input frequency (= PCLK output frequency) by the setting of the data format (LS1, and LS0) of the high-speed data channel and the bandwidth setting of PLL_BW0 and PLL_BW1.

Table 8. PLL Bandwidth Selection

LS1	LS0	PLL_BW1	PLL_BW0	CLK+/CLK- Frequency Range [MHz] (PCLK Input Frequency)	
				Min	Max
'L'	'L'	'L'	'L'	4	7
'L'	'L'	'L'	'H'	6	11
'L'	'L'	'H'	'L'	10	15
'L'	'H'	'L'	'L'	8	14
'L'	'H'	'L'	'H'	12	22
'L'	'H'	'H'	'L'	20	30
'H'	'L'	'L'	'L'	12	21
'H'	'L'	'L'	'H'	18	33
'H'	'L'	'H'	'L'	30	45

●Power Modes

BU7964UW has three power modes.

1) Shutdown Mode
BU7964GUW goes to Shutdown Mode when XSD = 'L.' AII logic circuits are initialized in the Shutdown Mode. All high-speed signaling are pulled down to MSGND. All parallel data interface output 'L'.

2) Standby Mode
BU7964GUW goes to a Standby Mode when XSD = 'H' and CLK+ / CLK− is Hi-Z. All high-speed signaling inputs sink DC current in order to pull the pins down to MSGND. BU7964GUW is monitoring V_{CM} of CLK+ / CLK−. When TX device starts driving high-speed signaling outputs, BU7964GUW detects its V_{CM} and switches to Active Mode. In Standby Mode, All parallel data interface output 'L'.

3) Active Mode
BU7964UW goes to Active Mode when XSD = 'H' and VCM is running.

Table 9. Power Modes

Power Mode	Input		Operation		
	XSD	Vcm of CLK+/CLK-	Functions	MSDL3 Terminals	Parallel output
Shutdown	'L'	MSGND	Initialized	Disabled(Pull-down)	Initial value
Standby	'H'	MSGND	MSDL3 Vcm detection	MSDL3 Vcm detection (Pull-down)	Initial value
Active	'H'	Clock input is active	MSDL3 V_{CM} monitor. Normal operation. (S2P conv)	MSDL3 V_{CM} monitor. Enabled.	Normal operation

4) Power Modes Transition

Fig.5.shows the Transition of power modes.

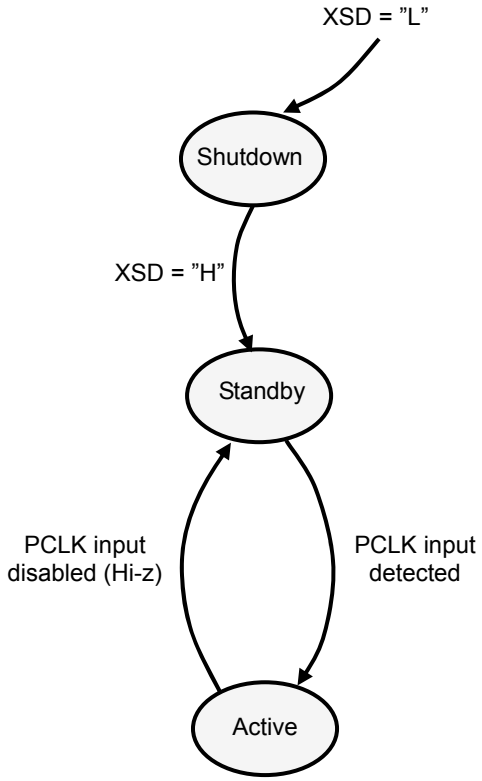


Fig.5. Power Modes Transition

●Link Error Detection

Detection of Parity Error

BU7964GUW counts the number of 'H' bits in PD[26:0] and CP in every pixel information received and detects parity error as follows:

- There is no parity error occurred if the number of 'H' bits in PD[26:0] and CP is odd.
- There is parity error occurred if the number of 'H' bits in PD[26:0] and CP is even.

If parity error is detected, BU7964GUW outputs the previous error-free pixel information and discards the invalid pixel information. At the same time, BU7964GUW toggles CPO during one PCLK period. BU7964GUW outputs initial value, if the parity error is detected when there is no previous pixel information. Otherwise, BU7964GUW outputs the received pixel information from the high-speed data channel(s) and CPO keeps 'L.'
Error correction is not supported in BU7964GUW.

●High-Speed Data Channel Protocols

Fig.6 Fig.7 and Fig.8 show high-speed data channel protocols.

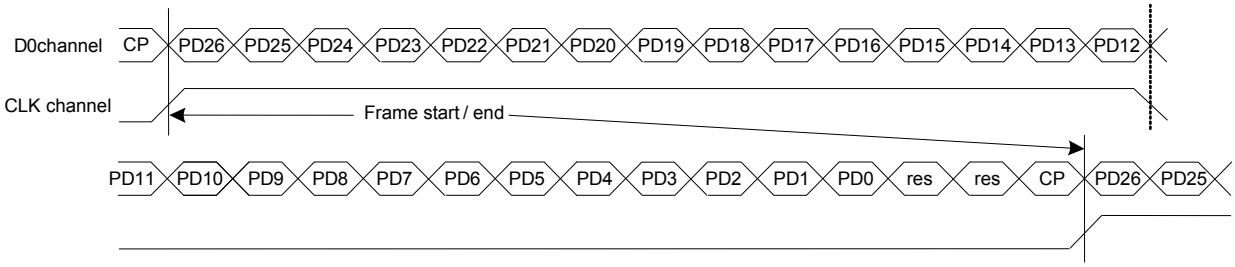


Fig.6. MSDL3 Protocol for 1-channel Data (27-bit)

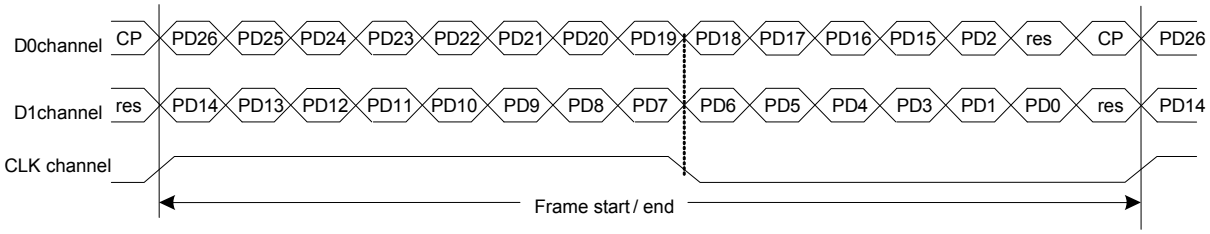


Fig.7. MSDL3 Protocol for 2-channel Data (27-bit)

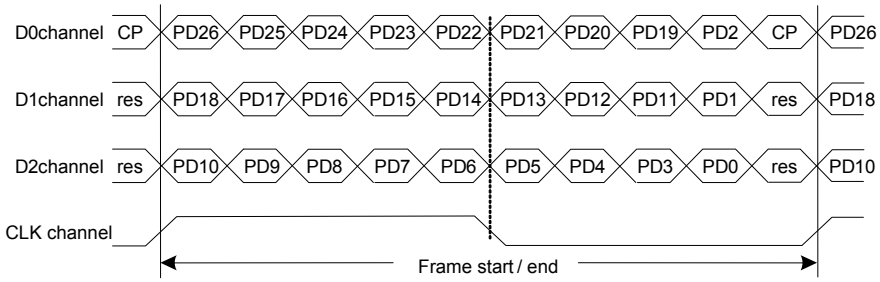


Fig.8. MSDL3 Protocol for 3-channel Data (27-bit)

"res" is reserved bit for the future use, the default state of those is '0.'

CP is the parity bit of data payload.
BU7964GUW adds an odd parity on CP of the high-speed channel data.

- When the number of 'H' bits in parallel data is even, CP bit is 'H.'
- When the number of 'H' bits in parallel data is odd, CP bit is 'L.'

●Electrical Characteristics

1) DC Characteristics

Table 10. Digital Input / Output DC Characteristics

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
'L' Input Voltage 1	VIL1	DGND	-	0.3 x DVDD	V	XSD, F_XS PLL_BW[1:0], LS[1:0]Pin
'H' Input Voltage 1	VIH1	0.7 x DVDD	-	DVDD	V	XSD, F_XS PLL_BW[1:0], LS[1:0]Pin
Output 'L' Voltage1	VOL1	DGND	-	0.3 x DVDD	V	F_XS='L', IO = 1mA, PCLK, CPO, PD[26:0]Pin
Output 'H' Voltage1	VOH1	0.7 x DVDD	-	DVDD	V	F_XS='L', IO = -1mA, PCLK, CPO, PD[26:0]Pin
Output 'L' Voltage2	VOL2	DGND	-	0.3 x DVDD	V	F_XS='H', IO = 3mA, PCLK, CPO, PD[26:0]Pin
Output 'H' Voltage2	VOH2	0.7 x DVDD	-	DVDD	V	F_XS='H', IO = -3mA, PCLK, CPO, PD[26:0]Pin
Output 'L' Voltage3	VOL3	DGND	-	0.15 x DVDD	V	IO = 100μA, PCLK, CPO, PD[26:0]Pin
Output 'H' Voltage3	VOH3	0.85 x DVDD	-	DVDD	V	IO = -100μA, PCLK, CPO, PD[26:0]Pin

Table 11. Current Consumption

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	$I_{op\_sht\_rx}$	-	0.2	10	μA	XSD = 'L', IDVDD + IMSVDD
Standby Current	$I_{op\_stb\_rx}$	-	41.8	90	μA	XSD = 'H', IDVDD + IMSVDD
Active Current 1-channel / 27-bit Format	$I_{op\_act\_rx1}$	-	17.6	24.0	mA	LS[1:0] = "LL", PLL_BW[1:0] = "HL", DVDD = MSVDD, PCLK = 15MHz, XSD = 'H', CL = 10pF, Total operating current (IDVDD + IMSVDD) with PD[26:0] outputs toggling 0x2AAAAAA and 0x5555555
Active Current 2-channel / 27-bit Format	$I_{op\_act\_rx2}$	-	28.0	36.8	mA	LS[1:0] = "LH", PLL_BW[1:0] = "HL" , DVDD = MSVDD, PCLK = 30MHz, XSD = 'H', CL = 10pF, Total operating current (IDVDD + IMSVDD) with PD[26:0] outputs toggling 0x2AAAAAA and 0x5555555
Active Current 3-channel / 27- bit Format	$I_{op\_act\_rx3}$	-	36.0	48.6	mA	LS[1:0] = "HL", PLL_BW[1:0] = "HL" , DVDD = MSVDD, PCLK = 45MHz, XSD = 'H', CL = 10pF, Total operating current (IDVDD + IMSVDD) with PD[26:0] outputs toggling 0x2AAAAAA and 0x5555555

2) AC Characteristics

Parallel Data Output Timing

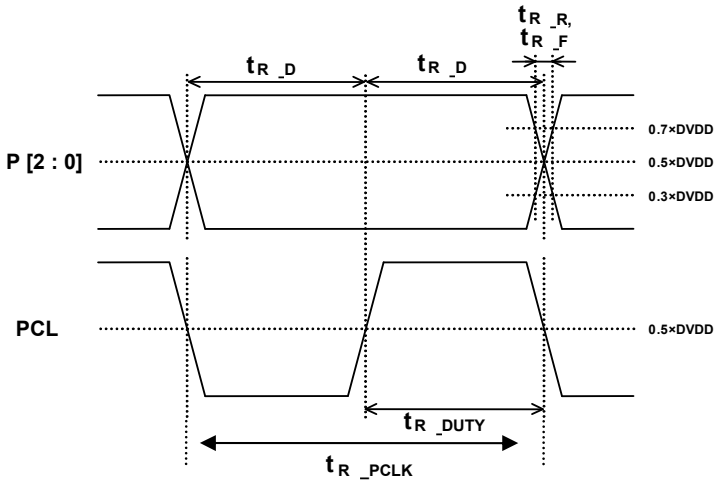


Fig.9. Parallel Data Output Timing

Table 12. Parallel Data Output AC Timing

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
PCLK Output Duty Cycle	t_{RX_DUTY}	45	50	55	%	CL=10pF
Output Data Setup Time	t_{RX_DS}	0.41X t_{Rx_PCLK}	-	-	ns	CL=10pF
Output Data Hold Time	t_{RX_DH}	0.41X t_{Rx_PCLK}	-	-	ns	CL=10pF
Output Data Rise Time/Fall time	t_{RX_R}	-	9	-	ns	F_XS=0, CL=10pF
	t_{RX_F}	-	3	-	ns	F_XS=1, CL=10pF

3) Power-On / Off Sequence

Power-On Sequence

Fig.10 shows power-on sequence of BU7964GUW.

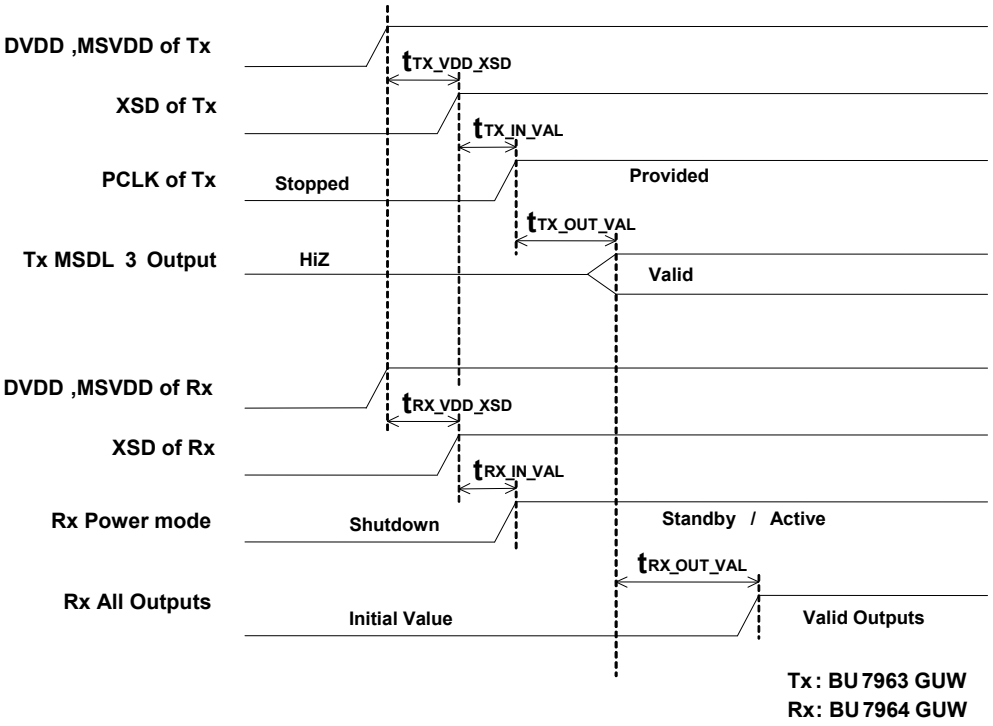


Fig.10. Power-On Sequence

Table 13. Power-On Sequence Timing

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Reset Valid After Power Supplied	$t_{RX\_VDD\_XSD}$	10	-	-	µs	
PCLK Valid After XSD Released	$t_{RX\_IN\_VAL}$	-	-	10	µs	
Parallel Data Valid After TX High-Speed Signals Valid	$t_{RX\_OUT\_VAL}$	-	-	2	ms	

Power-Off Sequence

Fig.11 shows the power-off sequence of BU7964GUW.

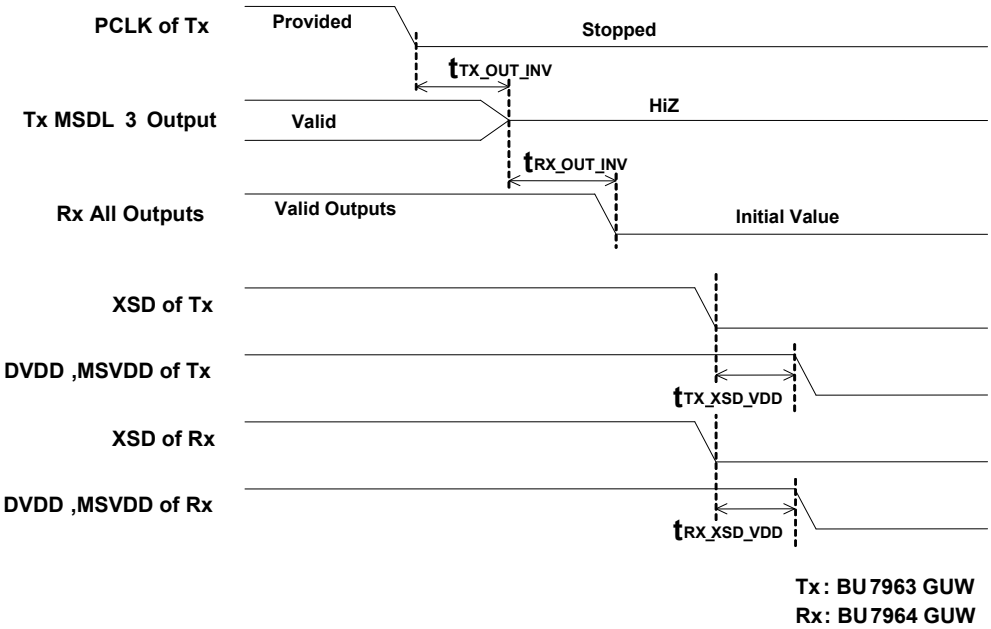


Fig.11. Power-Off Sequence Timing

Table 14. Power-Off Sequence Timing

Ta=25°C, DVDD=MSVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Parallel output delay time	$t_{RX\_OUT\_INV}$	-	-	100	μs	
XSD hold time	$t_{RX\_XSD\_VDD}$	10	-	-	μs	

●Frequency Change Sequence

Fig.12 shows the frequency change sequence of BU7964GUW.

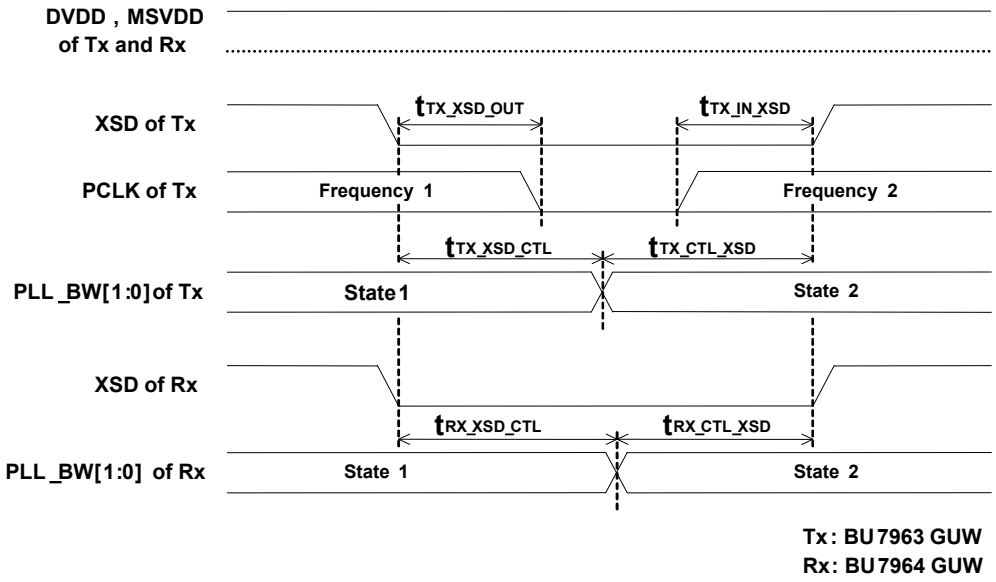


Fig.12. Frequency Change Sequence

Table 15. Frequency Change Sequence Timing

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Control Signal Hold Time	$t_{RX\_XSD\_CTL}$	2.0	-	-	µs	
Control Signal Setup Time	$t_{RX\_CTL\_XSD}$	2.0	-	-	µs	

●High-Speed Channel Characteristic

Table 16. High-speed channel characteristic

Ta=25°C, DVDD=MSVDD=1.80V and DGND=MSGND=0.00V, unless otherwise noted.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Differential Voltage Range	V_{diff_rx}	70	100	200	mVpp	
LOW-level threshold voltage	V_{thl}	-40	-	-	mV	
HIGH-level threshold voltage	V_{thh}	-	-	40	mV	
Common Mode Voltage Range	V_{cm_rx}	0.6	0.9	1.2	V	
Internal termination resistance	$R_{\_rx}$	75	100	125	Ω	
Operating Frequency	f_{opr_rx}	-	-	225	MHz	
RX sink current	I_{PULL_RX}	12	30	90	μA	
Link detection threshold voltage	V_{LINK_RX}	0.2	0.3	0.4	V	

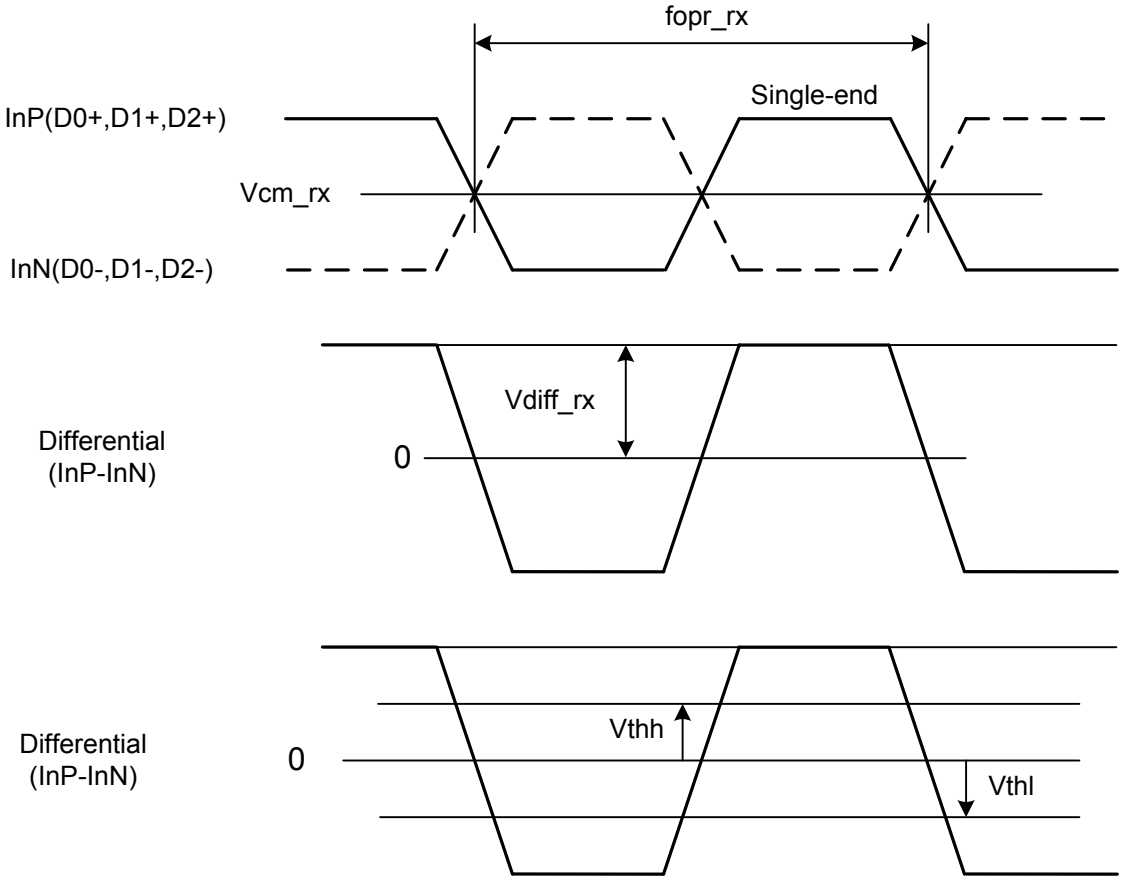


Fig.13. High-Speed Channel Characteristic

Fig.14 shows high-speed channel equivalent schematic.

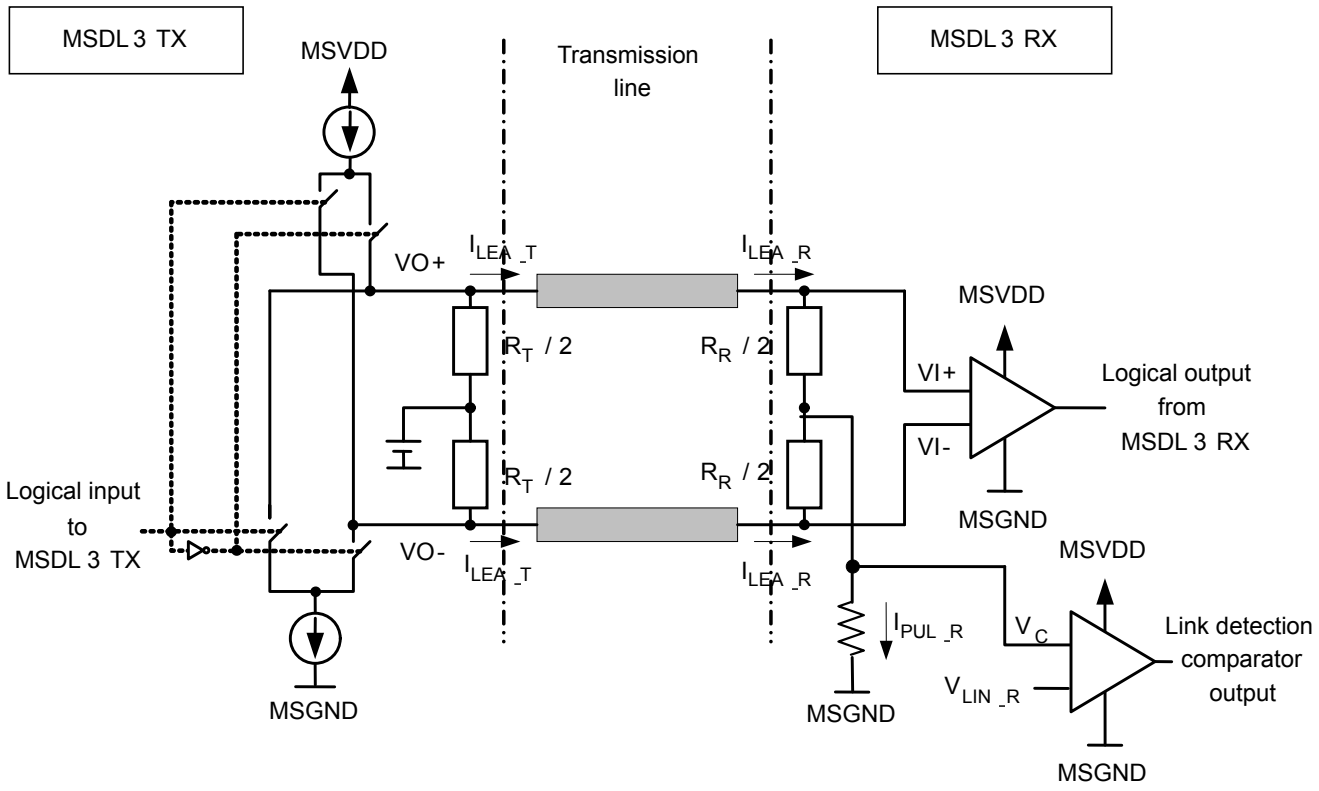


Fig.14. High-Speed Channel Equivalent Schematic.

●Application Circuit Example

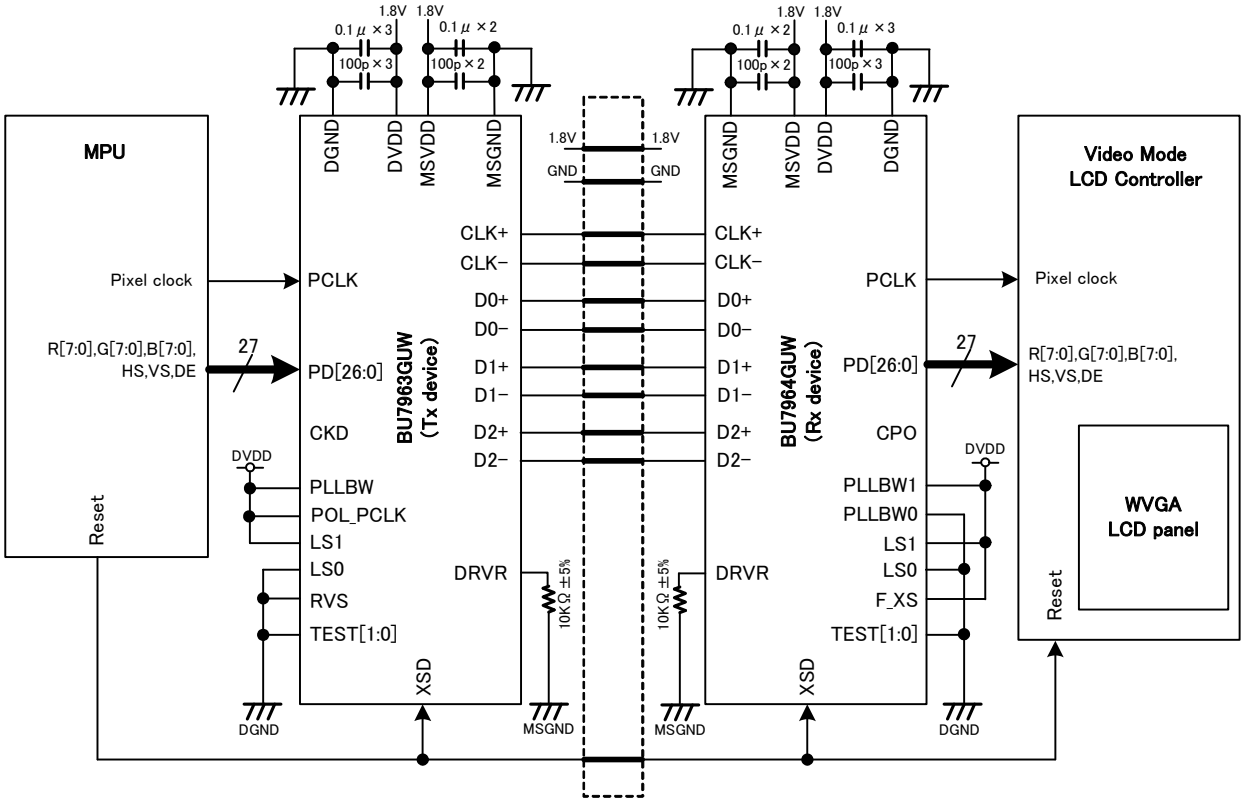


Fig.15. Application Circuit

●Ordering Part Number

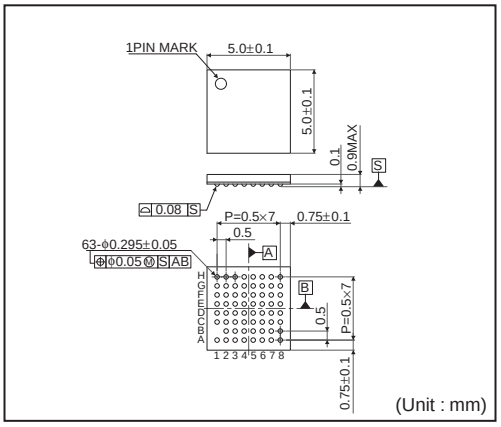
B	U	7	9	6	4	G	U	W	-	E	2

Part No. Part No.

Package
GUW: VBGA063W050

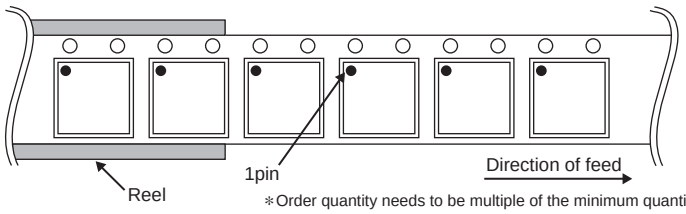
Packaging and forming specification
E2: Embossed tape and reel

VBGA063W050



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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