

LVDS Interface ICs

4bit LVDS Transceiver


BU90LV049A

No.09057EAT01

●Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

Driver and Receiver of 4 bits operate to 250MHz. It can be used for a variety of purposes, home appliances such as LCD-TV, business machines such as decoders, instruments, and medical equipment.

●Features

- 1) >500 Mbps (250 MHz) switching rates
- 2) Flow-through pinout simplifies PCB layout.
- 3) 400 ps typical driver channel-to-channel skew
- 4) 150 ps typical receiver channel-to-channel skew
- 5) 3.3V single power supply design
- 6) $\pm 200\text{mV}$ and $\pm 350\text{mV}$ selectable differential signaling (driver)
- 7) 6mA and 8mA selectable output drive strength (receiver)
- 8) 3-STATE output control
- 9) Internal fail-safe biasing of receiver inputs
- 10) High impedance on LVDS outputs on power down
- 11) Conforms to TIA/EIA-644-A LVDS Standard
- 12) Industrial operating temperature range (-40°C to +85°C)

●Applications

Car Navigation System
 Copier
 Digital TV (Signal System)
 FA equipment
 Medical equipment
 Vending machine, Ticket vending machine

●Precaution

- This chip is not designed to protect from radioactivity.

● Absolute maximum ratings

Item	Symbol	Value		Unit
		Min.	Max.	
Supply voltage	V_{CC}	-0.3	4.0	V
Input voltage	V_{IN}	-0.3	$V_{CC}+0.3$	V
Output voltage	V_{OUT}	-0.3	$V_{CC}+0.3$	V
Storage temperature range	Tstg	-55	150	°C

● Package Power

Package	PD(mW)	DERATING(mW/°C) ※1
SSOP-B16	400	4.0
	450 ^{*2}	4.5 ^{*2}

※1 At temperature $T_a > 25^{\circ}\text{C}$

※2 Package power when mounting on the PCB board.

The size of PCB board :70 × 70 × 1.6 (mm³)

The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area)

● Operating conditions

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Supply voltage	Vcc	3.0	3.3	3.6	V	
Operating temperature range	Topr	-40	25	85	°C	

●Electrical characteristics

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
LVC MOS Input DC Specification (Driver Inputs, ENABLE Pins)							
V_{IH}	Input High Voltage		D _{IN} EN SL	$V_{CC} \times 0.8$	–	V_{CC}	V
V_{IL}	Input Low Voltage			GND	–	$V_{CC} \times 0.2$	V
I_I	Input Current	$V_{IN} = 0V$ or V_{CC}		–10	–	+10	μA
V_{CL}	Input Clamp Voltage	$V_{CL} = -18mA$		–1.5	–0.8	–	V
LVDS Output DC Specification (Driver Output)							
$ V_{OD1} $	Differential Output Voltage	SL= GND, $R_L = 100\Omega$ (Figure 4)	D _{OUT-}	250	350	450	mV
$ V_{OD2} $	Differential Output Voltage	SL= V_{CC} , $R_L = 100\Omega$ (Figure 4)	D _{OUT+}	120	200	300	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States			–	1	35	mV
V_{OS}	Offset Voltage	SL = V_{CC} or GND, $R_L = 100\Omega$ (Figure 4)		1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States			–	1	25	mV
I_{OS}	Output Short Circuit Current	ENABLED, $D_{IN} = V_{CC}$, $D_{OUT+} = 0V$ or $D_{IN} = GND$, $D_{OUT-} = 0V$		–	–5.4	–9.0	mA
I_{OSD}	Differential Output Short Circuit Current	ENABLED, $V_{OD} = 0V$		–	–5.4	–9.0	mA
I_{OZ}	Output 3-STATE Current	EN = 0V and SL = V_{CC} $V_{OUT} = 0V$ or V_{CC}		–10	1	+10	μA
LVDS Input DC Specification (Receiver Inputs)							
V_{TH}	Differential Input High Threshold	$V_{CM} = 1.2V, 0.05V, 2.35V$	R _{IN+}	–	–	100	mV
V_{TL}	Differential Input Low Threshold		R _{IN-}	–100	–	–	mV
V_{CMR}	Common-Mode Voltage Range	$V_{ID} = 200mV$ pk to pk		0.1	–	2.3	V
I_{IN}	Input Current	$V_{IN} = 0$ or V_{CC}		–20	–	+20	μA
LVC MOS Output DC Specification (Receiver Outputs)							
V_{OH1}	Output High Voltage	$I_{OH} = -8 mA$, $V_{ID} = +200 mV$, SL=GND	R _{OUT}	$V_{CC} - 0.4$	–	–	V
V_{OH2}	Output High Voltage	$I_{OH} = -6 mA$, $V_{ID} = +200 mV$, SL = V_{CC}		$V_{CC} - 0.4$	–	–	
V_{OL1}	Output Low Voltage	$I_{OL} = 8 mA$, $V_{ID} = -200 mV$, SL=GND		–	–	0.4	V
V_{OL2}	Output Low Voltage	$I_{OL} = 6 mA$, $V_{ID} = -200 mV$, SL = V_{CC}		–	–	0.4	
I_{OZ}	Output 3-STATE Current	Disabled, $V_{OUT} = 0V$ or V_{CC}		–10	1	+10	μA
General DC Specifications							
I_{CC}	Power Supply Current	EN = V_{CC} and SL = 0V	V_{CC}	–	12	–	mA
I_{CCZ}	TRI-State Supply Current	EN = 0V and SL = 0V		–	2	–	mA

● Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS Outputs (Driver Outputs)						
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 15pF$ (Figure 5 and Figure 6)	0.5	1.7	2.8	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	1.7	2.8	ns
t_{SKD1}	Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $		0	0.3	0.4	ns
t_{SKD2}	Differential Channel-to-Channel Skew		0	0.4	0.5	ns
t_{SKD3}	Differential Part to Part Skew		0	-	1.0	ns
t_{TLH}	Rise Time		-	0.5	1.5	ns
t_{THL}	Fall Time		-	0.5	1.5	ns
t_{PHZ}	Disable Time High to Z	$R_L = 100\Omega$, $C_L = 15pF$ (Figure 7 and Figure 8)	-	2	5	ns
t_{PLZ}	Disable Time Low to Z		-	2	5	ns
t_{PZH}	Enable Time Z to High		-	3	7	ns
t_{PZL}	Enable Time Z to Low		-	3	7	ns
f_{Max}	Maximum Operating Frequency		250	-	-	MHz
LVCMOS Outputs (Receiver Outputs)						
t_{PHL}	Propagation Delay High to Low	$C_L = 15pF$ $V_{ID} = 200mV$ (Figure 9 and Figure 10)	1.2	2.0	3.7	ns
t_{PLH}	Propagation Delay Low to High		1.2	1.9	3.7	ns
t_{SK1}	Pulse Skew $ t_{PHLD} - t_{PLHD} $		0	0.1	0.4	ns
t_{SK2}	Channel-to-Channel Skew		0	0.15	0.5	ns
t_{SK3}	Part to Part Skew		-	-	1.0	ns
t_{TLH}	Rise Time		-	0.5	1.5	ns
t_{THL}	Fall Time		-	0.5	1.5	ns
t_{PHZ}	Disable Time High to Z	$R_L = 2k\Omega$ $C_L = 15pF$ (Figure 11 and Figure 12)	-	8	14	ns
t_{PLZ}	Disable Time Low to Z		-	8	14	ns
t_{PZH}	Enable Time Z to High		-	3	14	ns
t_{PZL}	Enable Time Z to Low		-	9	14	ns
f_{Max}	Maximum Operating Frequency		250	-	-	MHz

●Block diagram

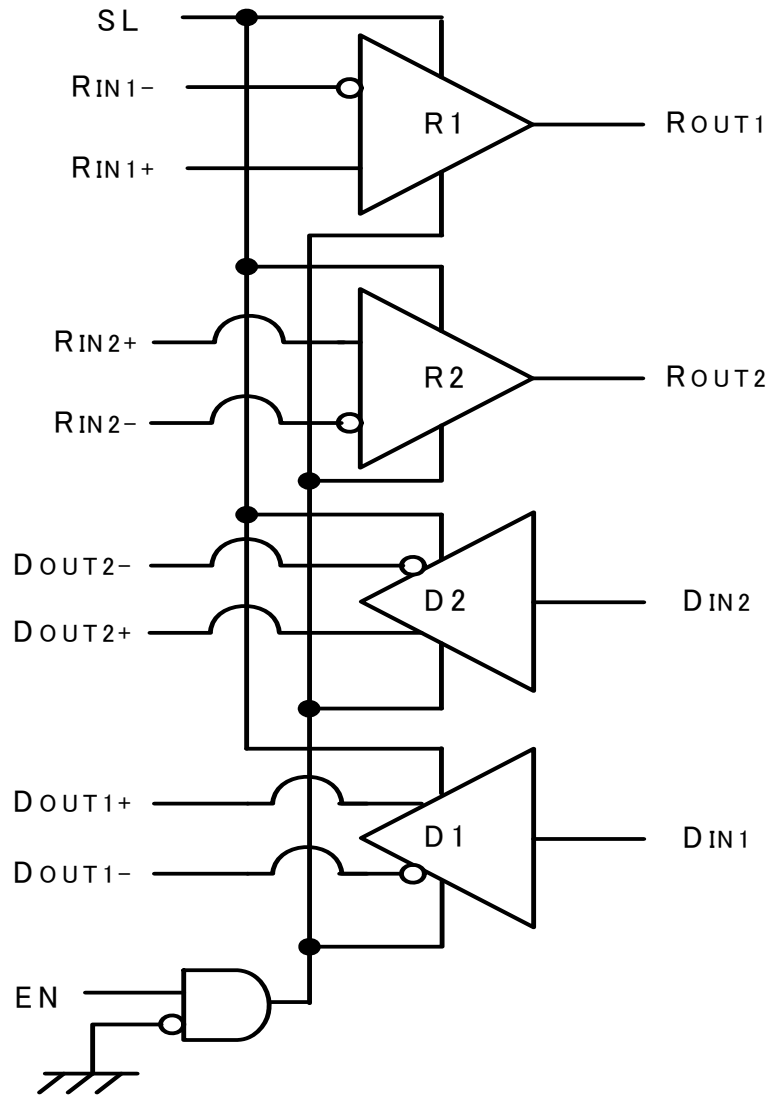


Figure 1. Block Diagram

●SSOP-B16 Package Outline and Specification

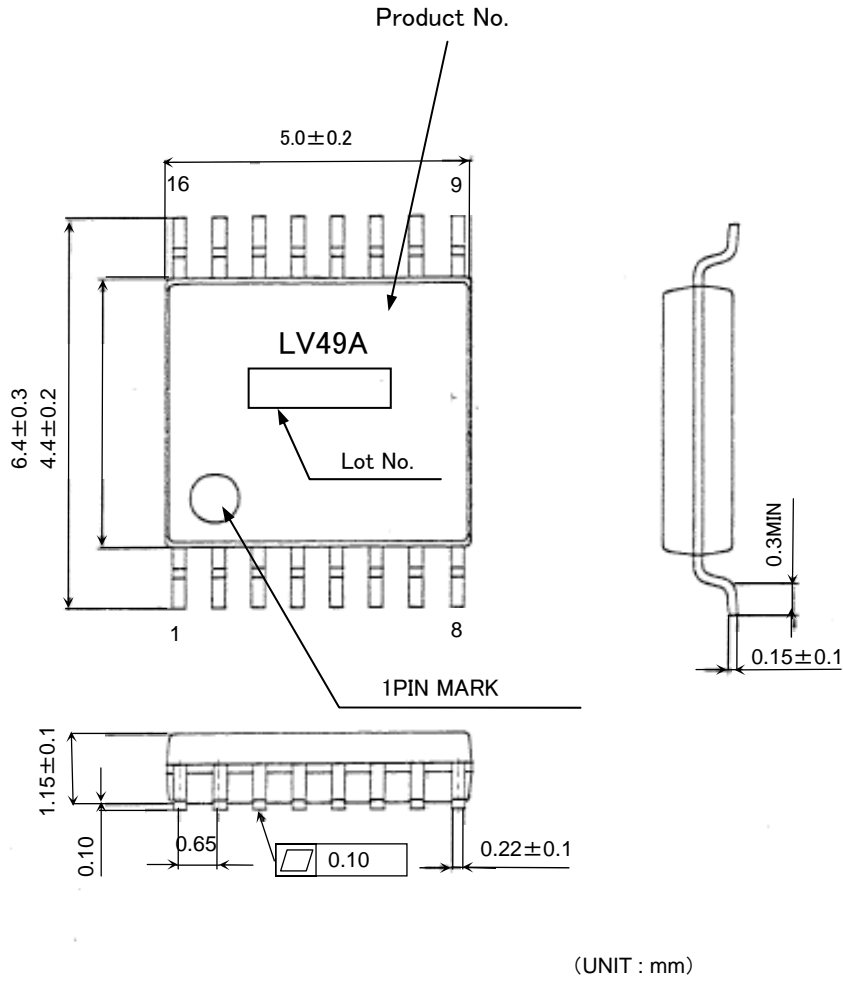


Figure 2. SSOP-B16 Package Outline and Specification

● Pin Configuration

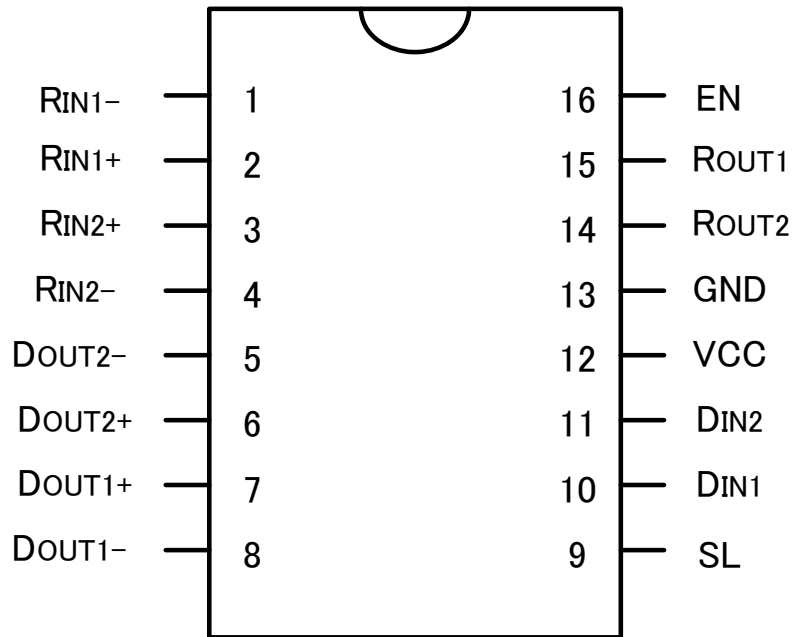


Figure 3. Pin Diagram (Top View)

● Pin Description

Table 1 : Pin Description

Pin Name	Pin No.	Type	Descriptions
DIN	10, 11	LVC MOS In	Driver input pin, LVC MOS levels.
DOUT+	6, 7	LVDS Out	Non-inverting driver output pin, LVDS levels.
DOUT-	5, 8	LVDS Out	Inverting driver output pin, LVDS levels.
RIN+	2, 3	LVDS In	Non-inverting receiver input pin, LVDS levels.
RIN-	1, 4	LVDS In	Inverting receiver input pin, LVDS levels.
ROUT	14, 15	LVC MOS Out	Receiver output pin, LVC MOS levels.
SL	9	LVC MOS In	Drive strength and Swing Level select pin : When SL is low or open, Rout set 8mA mode and the driver is normal swing level (350mV). When SL is high, Rout set 6mA mode and the driver is reduce swing level (200mV).
EN	16	LVC MOS In	Enable pin: When EN is Low or open, the receiver and driver are disabled. When EN is high, the receiver and driver are enabled.
VCC	12	Power	Power supply pin, +3.3V±0.3V.
GND	13	GND	Ground pin.

●Function Description

■Driver Truth Table

		INPUT	OUTPUTS		Swing Level
EN	SL	DIN	DOUT+	DOUT-	
H	L or Open	L	L	H	350mV
		H	H	L	
H	H	L	L	H	200mV
		H	H	L	
All other combinations of EN, SL inputs		X	Z	Z	

■Receiver Truth Table

		INPUT	OUTPUTS	Drive Strength
EN	SL	$R_{IN+} - R_{IN-}$	R_{OUT}	
H	L or Open	$VID \geq 0V$	H	8mA
		$VID \leq -0.1V$	L	
		Full Fail-safe OPEN/SHORT or Terminated	H	
H	H	$VID \geq 0V$	H	6mA
		$VID \leq -0.1V$	L	
		Full Fail-safe OPEN/SHORT or Terminated	H	
All other combinations of EN, SL inputs		X	Z	

●Parameter Measurement Information

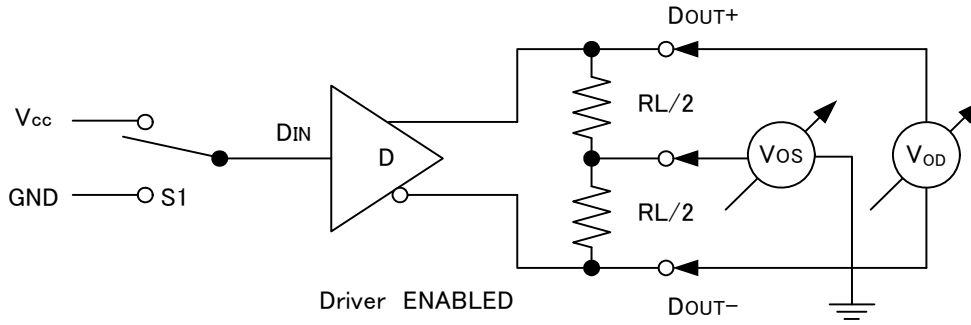


Figure 4. Driver VOD and VOS Test Circuit

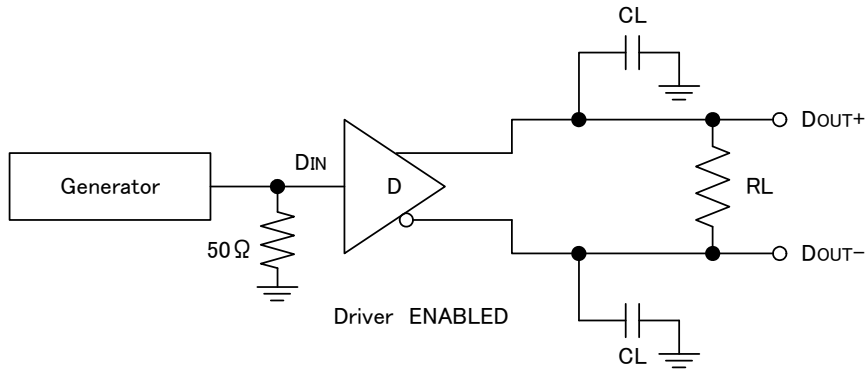


Figure 5. Driver Propagation Delay and Transition Time Test Circuit

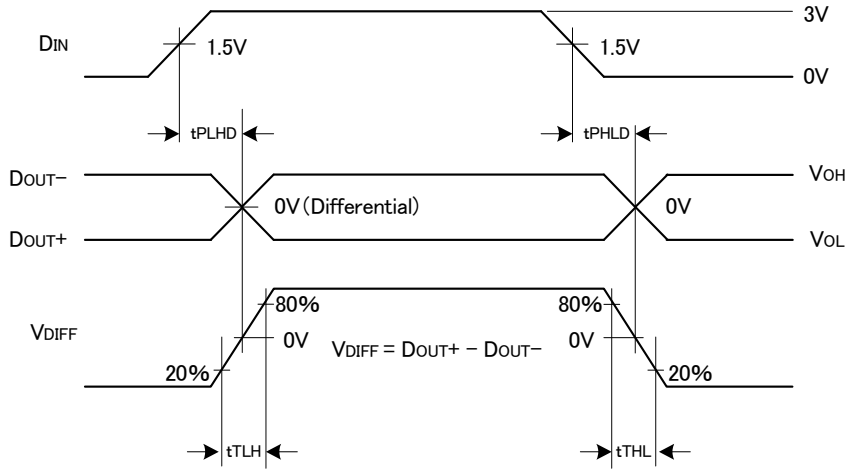


Figure 6. Driver Propagation Delay and Transition Time Waveforms

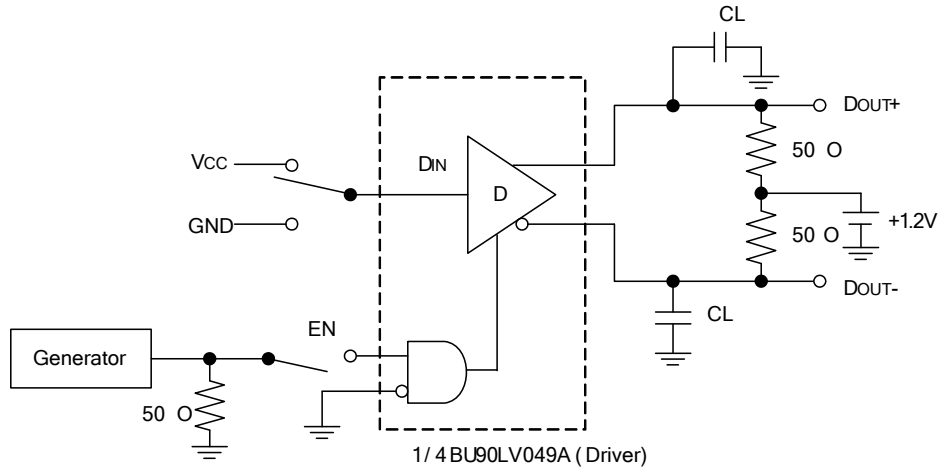


Figure 7. Driver 3-STATE Delay Test Circuit

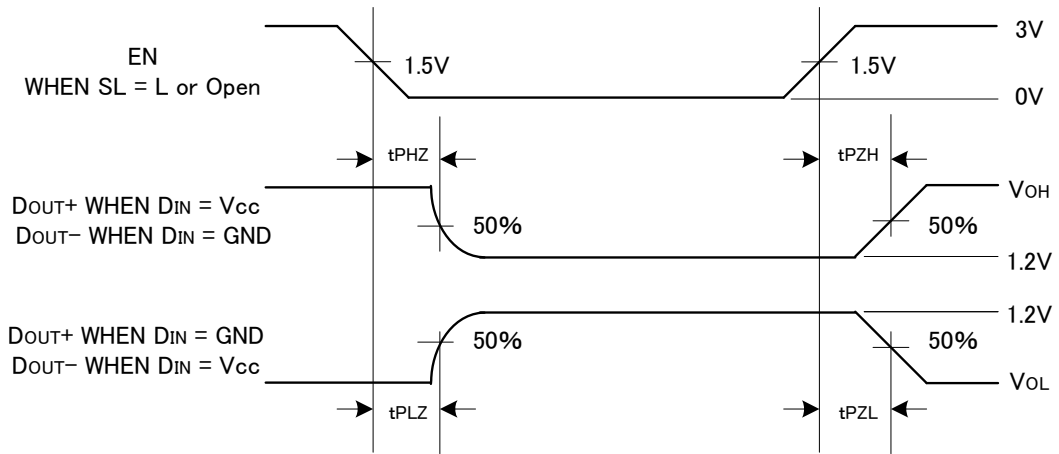


Figure 8. Driver 3-STATE Delay Waveform

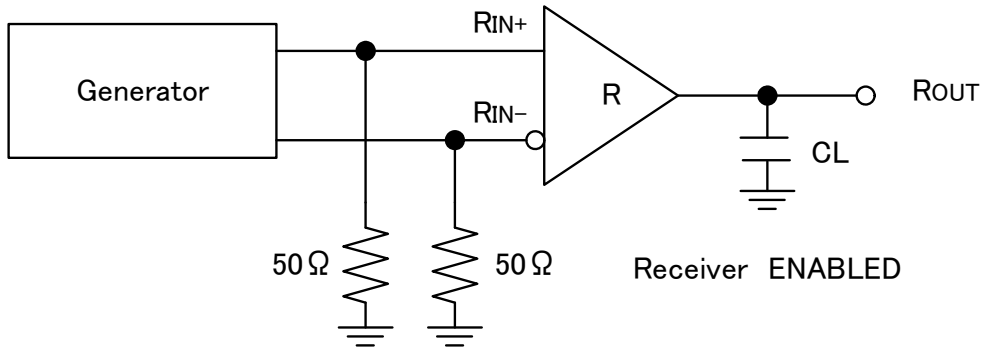


Figure 9. Receiver Propagation Delay and Transition Time Test Circuit

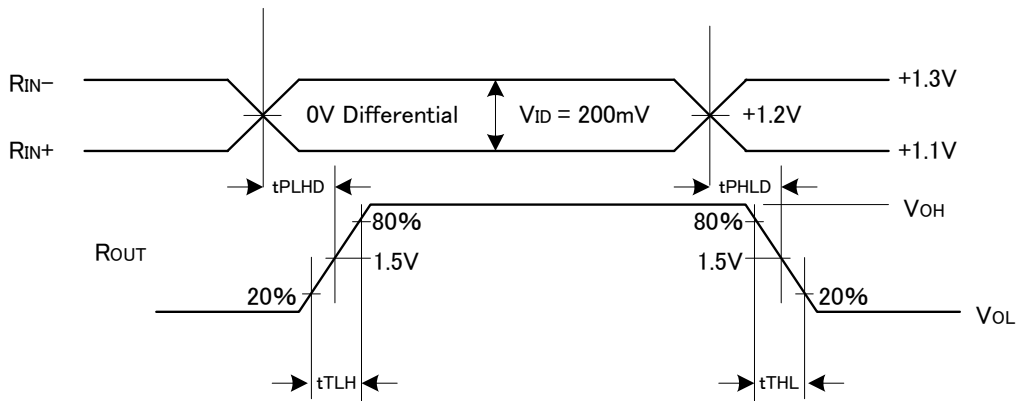


Figure 10. Receiver Propagation Delay and Transition Time Waveforms

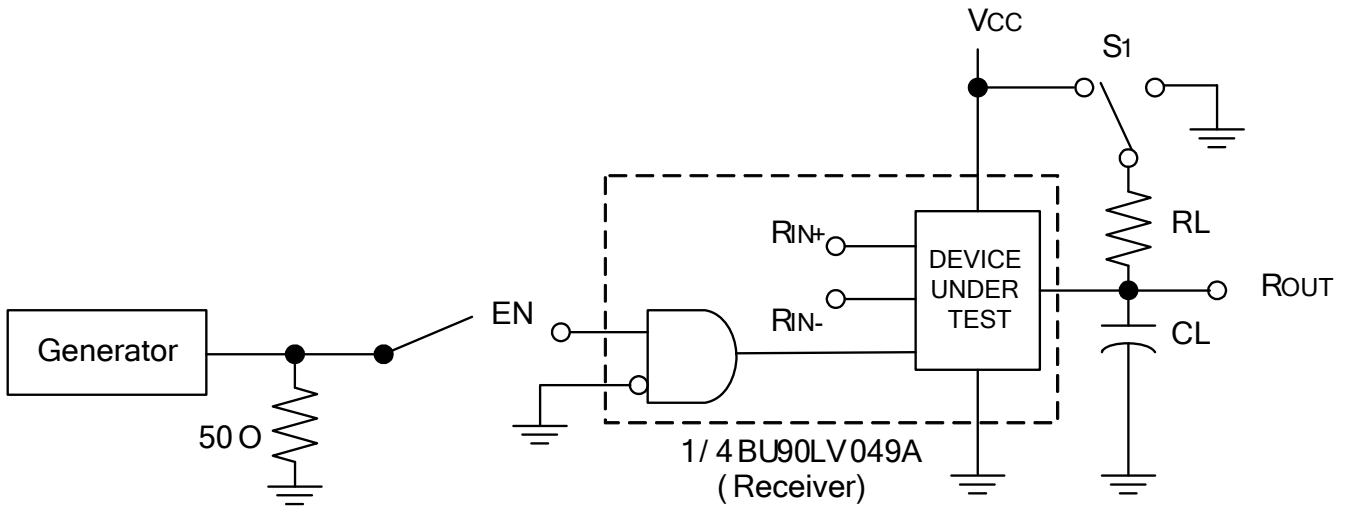


Figure 11. Receiver 3-STATE Delay Test Circuit

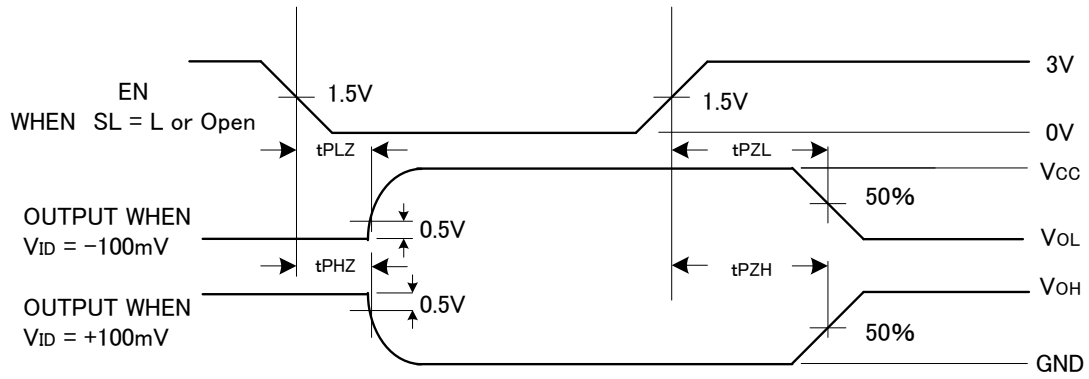


Figure12. Receiver 3-STATE Delay Waveforms

● Typical Application

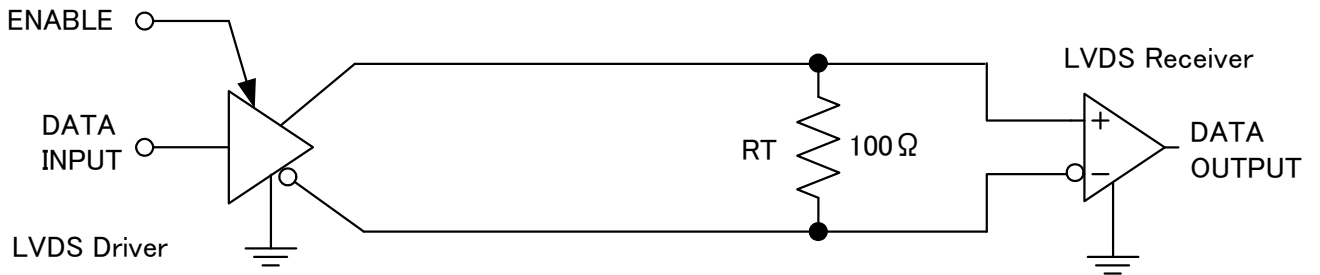


Figure 13. Point-to-Point Application

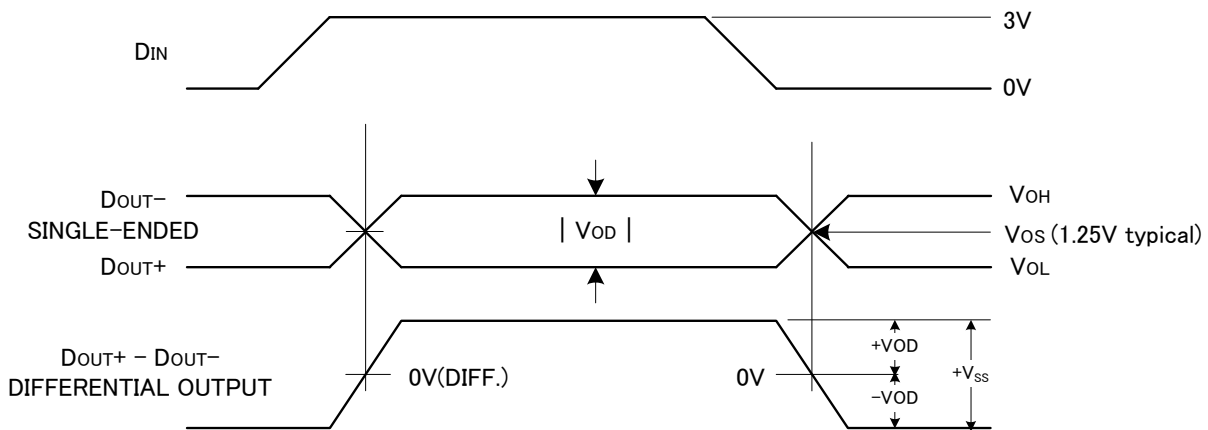


Figure 14. Driver Output Levels

●Ordering part number

B	U
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Part No.

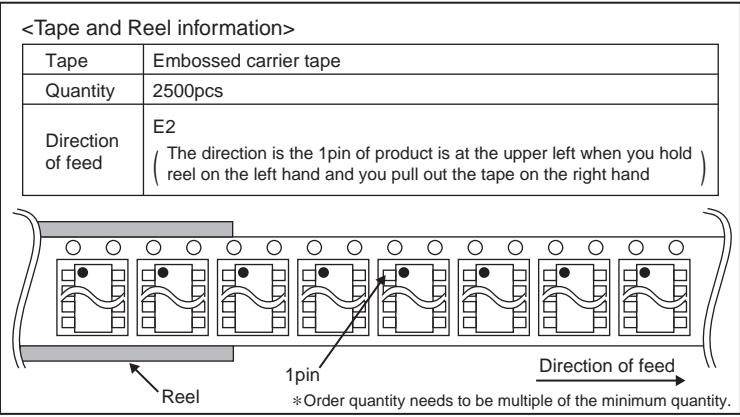
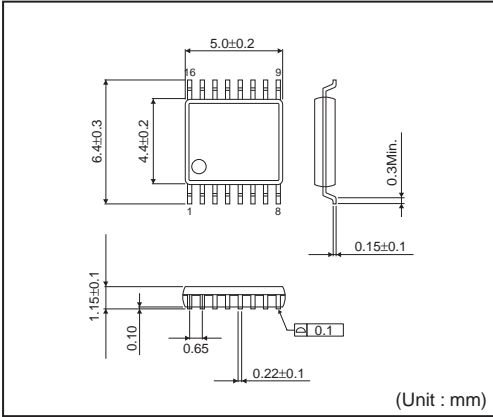
9	0	L	V	0	4	9	A
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Part No.

E	2
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Packaging and forming specification
E2: Embossed tape and reel

SSOP-B16



Notes

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