Low Duty LCD Segment Driver For Automotive COG Application

BU91R63CH-M3BW Max 176 segments (SEG44 x COM4)

General Description

BU91R63CH-M3BW is a 1/4, 1/3, 1/2 duty or Static COG type LCD driver that can be used for automotive applications and can drive up to 176 LCD segments.
It can support operating temperature of up to +105°C and compliant for AEC-Q100, as required for Automotive Application. It has integrated display RAM for reducing CPU load. Also, it is designed with low power consumption and no external component needed. It includes read function for display RAM and command register, wherein it is possible to detect malfunction due to noise. Also a defective mounting of COG can easily be controlled by using pins to measure ITO resistance.

Features

- AEC-Q100 compliant (Note1)
- 1/4, 1/3, 1/2 duty or Static setting selectable
  1/4 duty drive: Max 176 segments
  1/3 duty drive: Max 132 segments
  1/2 duty drive: Max 88 segments
  Static drive: Max 44 segments
- Integrated Buffer AMP for LCD driving
- Support Read Register and Display RAM Function
- Support ITO Resistance Measurement
- Integrated Oscillator Circuit
- Integrated EVR function to adjust LCD contrast
- Integrated Power-on Reset Circuit
- No External Components
- Low Power Consumption Design

(Note1) Quality Information:
There is data when LSI was put on a temporary package.
Please use it as reference data.

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- LCD Drive Power Supply Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 176 Segments
- Display Duty: 1/4, 1/3, 1/2, Static selectable
- Bias: 1/2, 1/3 selectable
- Interface: 2 wire serial interface

Special Characteristics

- ESD(HBM): ±2000V
- Latch-up current: ±100mA

Applications

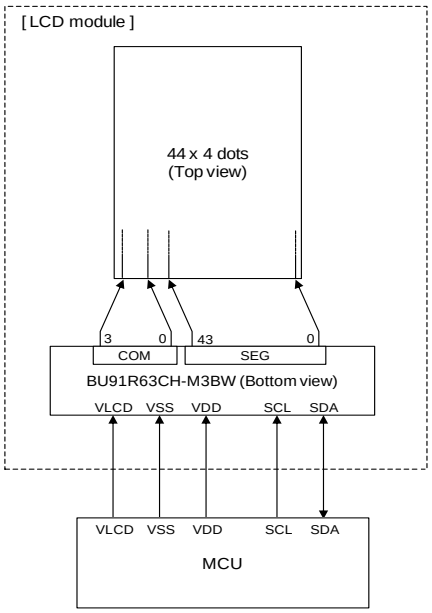
- Instrument Clusters
- Climate Controls
- Car Audios / Radios
- Metering
- White Goods
- Healthcare Products
- Battery Operated Applications

etc.

Package

Au BUMP chip

Typical Application Circuit



(Note) SDA of BU91R63CH-M3BW needs pull-up resistor due to open-drain output.
In case that SCL of MCU has open-drain structure, it also needs pull-up resistor.

Figure 1. Typical Application Circuit

Block Diagram / Pin Description

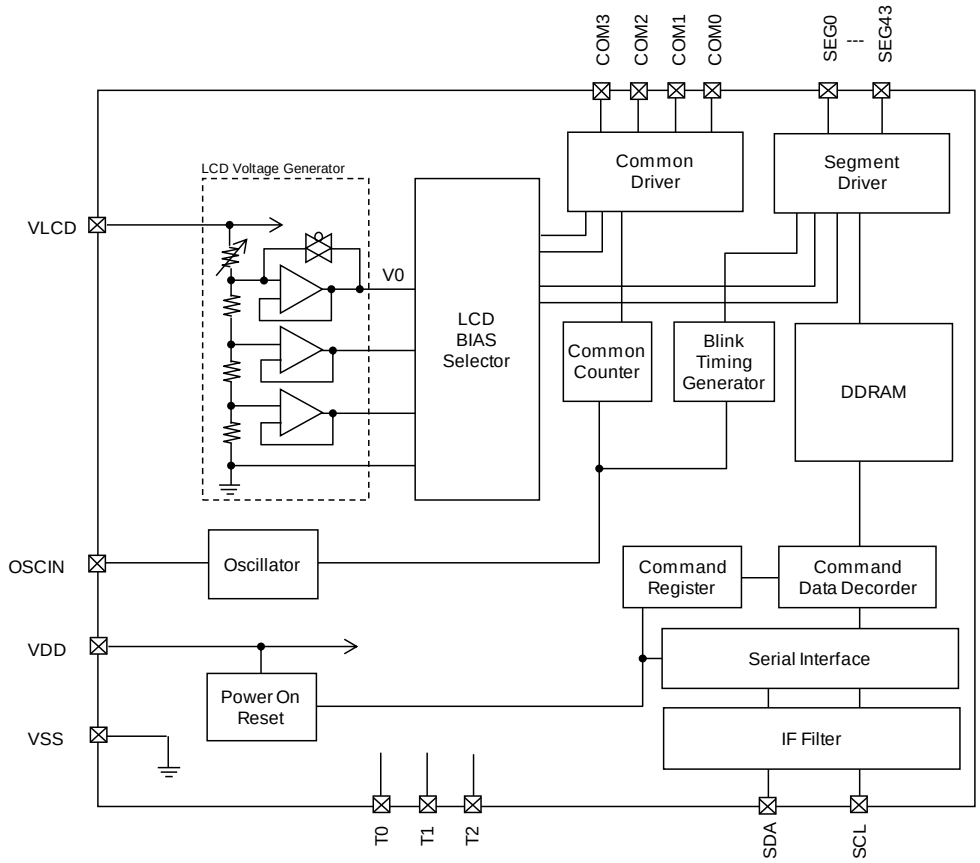


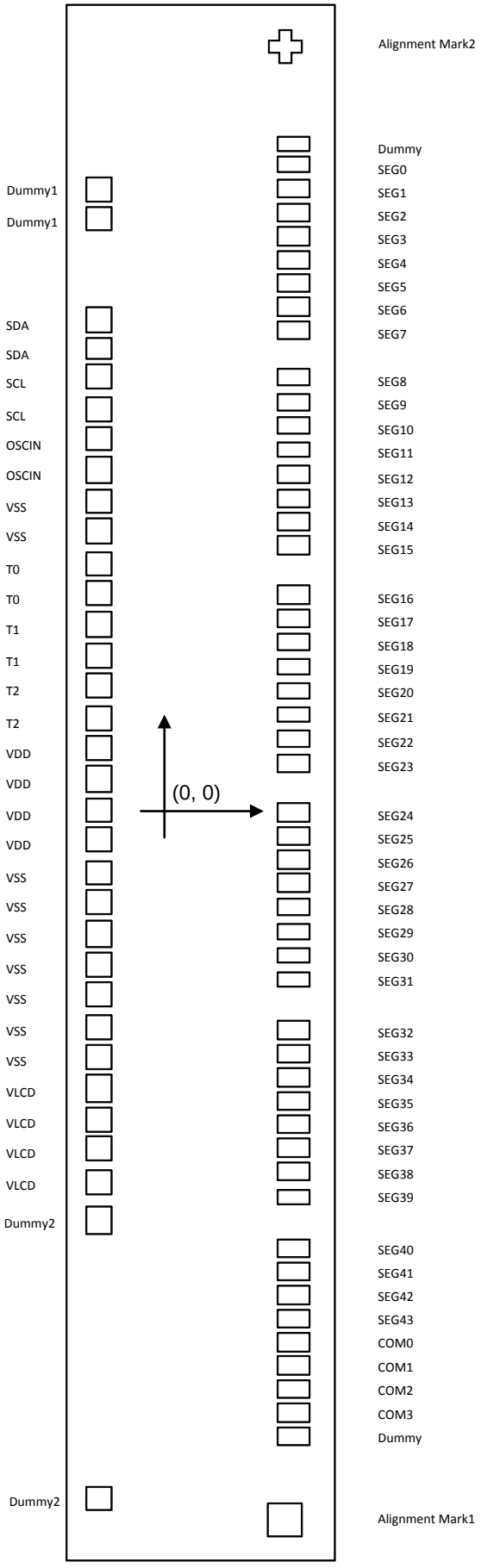
Figure 2. Block Diagram

Table 1. Pin Description

Terminal name	I/O	Function	Handling when unused
T0	I	POR enable setting VDD: POR disable (Note) VSS: POR enable	VSS
T1	I	Test input (ROHM use only) Must be connected to VSS.	VSS
T2	I	Test input (ROHM use only) Must be connected to VSS.	VSS
DUMMY	-	Open	OPEN
DUMMY1, 2	-	Can be used for COG resistance measurement.	OPEN
OSCIN	I	External clock input External clock and Internal clock can be selected by command Must be connected to VSS when using internal oscillator	VSS
SDA	I/O	Serial data in-out terminal	-
SCL	I	Serial clock terminal	-
VSS	I	GND	-
VDD	I	Power supply for logic	-
VLCD	I	Power supply for LCD driving circuit	-
SEG0 to 43	O	SEGMENT output for LCD driving	OPEN
COM0 to 3	O	COMMON output for LCD driving	OPEN

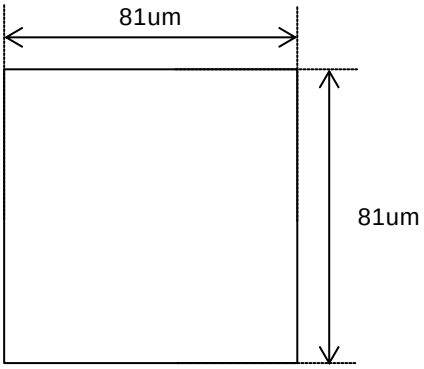
(Note) This function is guaranteed by design, not tested in production process. Software Reset is necessary to initialize IC in case of T0=VDD.

PAD Arrangement (Top view)



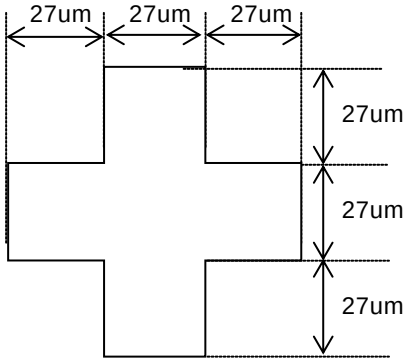
Item	Size		Unit
	X	Y	
Chip size	650	3560	µm
Chip thickness	230		µm
Bump height	15 ± 3		µm
Bump hardness	50 ± 20		Hv

Alignment Mark 1



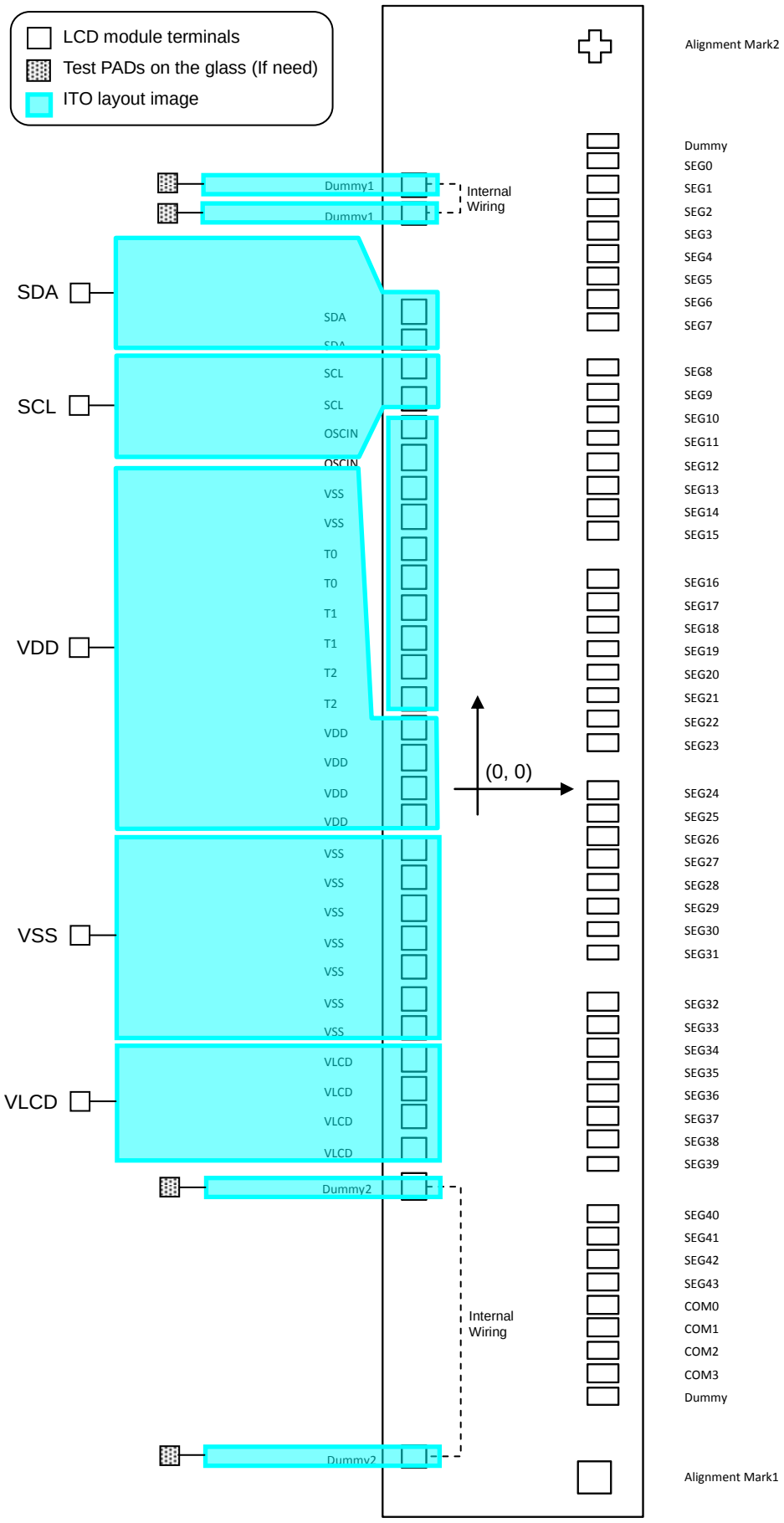
Mark center coodinates
(X, Y) = (206.6, -1685.0)

Alignment Mark 2



Mark center coodinates
(X, Y) = (206.6, 1685.0)

Recommended ITO Layout (Top view)



(Note) Design ITO layout to minimize its resistance.

PAD Coordinates

No	Terminal Name	BUMP Center		BUMP Size	
		X	Y	X	Y
1	Dummy1	-248.00	1340.00	60	55
2	Dummy1	-248.00	1270.00	60	55
3	SDA	-248.00	1045.00	60	55
4	SDA	-248.00	975.00	60	55
5	SCL	-248.00	905.00	60	55
6	SCL	-248.00	835.00	60	55
7	OSCIN	-248.00	765.00	60	55
8	OSCIN	-248.00	695.00	60	55
9	VSS	-248.00	625.00	60	55
10	VSS	-248.00	555.00	60	55
11	T0	-248.00	485.00	60	55
12	T0	-248.00	415.00	60	55
13	T1	-248.00	345.00	60	55
14	T1	-248.00	275.00	60	55
15	T2	-248.00	205.00	60	55
16	T2	-248.00	135.00	60	55
17	VDD	-248.00	65.00	60	55
18	VDD	-248.00	-5.00	60	55
19	VDD	-248.00	-75.00	60	55
20	VDD	-248.00	-145.00	60	55
21	VSS	-248.00	-215.00	60	55
22	VSS	-248.00	-285.00	60	55
23	VSS	-248.00	-355.00	60	55
24	VSS	-248.00	-425.00	60	55
25	VSS	-248.00	-495.00	60	55
26	VSS	-248.00	-565.00	60	55
27	VSS	-248.00	-635.00	60	55
28	VLCD	-248.00	-705.00	60	55
29	VLCD	-248.00	-775.00	60	55
30	VLCD	-248.00	-845.00	60	55
31	VLCD	-248.00	-915.00	60	55
32	Dummy2	-248.00	-1005.00	60	55
33	Dummy2	-248.00	-1636.00	60	55
34	Dummy	227.00	-1496.55	75	39
35	COM3	227.00	-1442.55	75	39
36	COM2	227.00	-1388.55	75	39
37	COM1	227.00	-1334.55	75	39
38	COM0	227.00	-1280.55	75	39
39	SEG43	227.00	-1226.55	75	39
40	SEG42	227.00	-1172.55	75	39
41	SEG41	227.00	-1118.55	75	39
42	SEG40	227.00	-1064.55	75	39
43	SEG39	227.00	-950.90	75	39
44	SEG38	227.00	-896.90	75	39
45	SEG37	227.00	-842.90	75	39
46	SEG36	227.00	-788.90	75	39
47	SEG35	227.00	-734.90	75	39
48	SEG34	227.00	-680.90	75	39
49	SEG33	227.00	-626.90	75	39
50	SEG32	227.00	-572.90	75	39
51	SEG31	227.00	-458.85	75	39
52	SEG30	227.00	-404.85	75	39
53	SEG29	227.00	-350.85	75	39
54	SEG28	227.00	-296.85	75	39
55	SEG27	227.00	-242.85	75	39
56	SEG26	227.00	-188.85	75	39
57	SEG25	227.00	-134.85	75	39
58	SEG24	227.00	-80.85	75	39
59	SEG23	227.00	33.20	75	39
60	SEG22	227.00	87.20	75	39
61	SEG21	227.00	141.20	75	39
62	SEG20	227.00	195.20	75	39
63	SEG19	227.00	249.20	75	39
64	SEG18	227.00	303.20	75	39
65	SEG17	227.00	357.20	75	39
66	SEG16	227.00	411.20	75	39
67	SEG15	227.00	525.25	75	39
68	SEG14	227.00	579.25	75	39
69	SEG13	227.00	633.25	75	39
70	SEG12	227.00	687.25	75	39
71	SEG11	227.00	741.25	75	39
72	SEG10	227.00	795.25	75	39
73	SEG9	227.00	849.25	75	39
74	SEG8	227.00	903.25	75	39
75	SEG7	227.00	1017.30	75	39
76	SEG6	227.00	1071.30	75	39
77	SEG5	227.00	1125.30	75	39
78	SEG4	227.00	1179.30	75	39
79	SEG3	227.00	1233.30	75	39
80	SEG2	227.00	1287.30	75	39
81	SEG1	227.00	1341.30	75	39
82	SEG0	227.00	1395.30	75	39
83	Dummy	227.00	1449.30	75	39

Absolute Maximum Ratings (VSS = 0 V)

Parameter	Symbol	Ratings			Unit	Remarks
		MIN	TYP	MAX		
Maximum Voltage1	VDD	-0.5	-	+7.0	V	Power Supply
Maximum Voltage2	VLCD	-0.5	-	+7.0	V	LCD Drive Voltage
Input Voltage Range	VIN	-0.5	-	+7.0	V	
Human Body Model (HBM)(Note1), (Note2)	VESD	-	±2000	-	V	
Latch-up current(Note1), (note3)	ILU	-	±100	-	mA	
Operational Temperature Range	Topr	-40	-	+105	°C	
Storage Temperature Range	Tstg	-55	-	+125	°C	

(Note1) Please use as reference data.
(Note2) Testing standards: JESD22-A114E
(Note3) Testing standards: JESD78
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommend Operating Conditions (Ta = -40°C to 105°C, VSS = 0 V)

Parameter	Symbol	Ratings			Unit	Remarks
		MIN	TYP	MAX		
Power Supply Voltage 1	VDD	2.7	-	6.0	V	Power Supply
Power Supply Voltage 2	VLCD	2.7	-	6.0	V	LCD Drive Voltage

Electrical Characteristics

DC Characteristics (Ta = -40°C to 105°C, VDD = 2.7V to 6.0V, VSS = 0.0V, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Condition
			MIN	TYP	MAX		
“H” Level Input Voltage		VIH	0.7VDD	-	VDD	V	SDA, SCL, OSCIN
“L” Level Input Voltage		VIL	VSS	-	0.3VDD	V	SDA, SCL, OSCIN
“H” Level Input Current		IIH	-	-	1	µA	SDA, SCL, OSCIN, T0, T1, T2
“L” Level Input Current		IIL	-1	-	-	µA	SDA, SCL, OSCIN, T0, T1, T2
SDA “L” Level Output Voltage		VOLSDA	0	-	0.4	V	Iload=-3mA
LCD Driver On Resistance	SEG	RON	-	3	-	kΩ	Iload=±10uA
	COM	RON	-	3	-	kΩ	
Standby Current		IVDD1	-	-	5	µA	Display off, Oscillation off
		IVLCD1	-	-	5	µA	
Operating Current		IVDD2	-	2.0	10	µA	VDD = 3.3V, VLCD = 3.3V, Ta = 25°C, Power save mode1, 1/3 bias, Frame inversion Frame Frequency = 80Hz setting
		IVLCD2	-	5.5	20	µA	

Electrical Characteristics – continued

Oscillation Characteristics (Ta = -40°C to 105°C, VDD = 2.7V to 6.0V, VSS = 0 V, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Frame Frequency 1	fCLK1	56	80	104	Hz	FR = 80Hz setting, VDD=2.7V to 6.0V, Ta=-40°C to +105°C
Frame Frequency 2	fCLK2	72	80	88	Hz	FR = 80Hz setting, VDD=3.5V, Ta=-40°C to +105°C
External Clock Rise Time	trCLK	-	-	0.3	µs	External Clock Setting(Note)
External Clock Fall Time	tfCLK	-	-	0.3	µs	
External Clock Frequency	fCLK3	30	-	300	kHz	
External Clock Duty	Tdty	30	50	70	%	

(Note) <Frame frequency calculation at external clock mode>
DISCTL 80HZ setting: Frame frequency [Hz] = external clock [Hz] / 512
DISCTL 130HZ setting: Frame frequency [Hz] = external clock [Hz] / 315
DISCTL 64HZ setting: Frame frequency [Hz] = external clock [Hz] / 648
DISCTL 200HZ setting: Frame frequency [Hz] = external clock [Hz] / 205

[Reference Data]

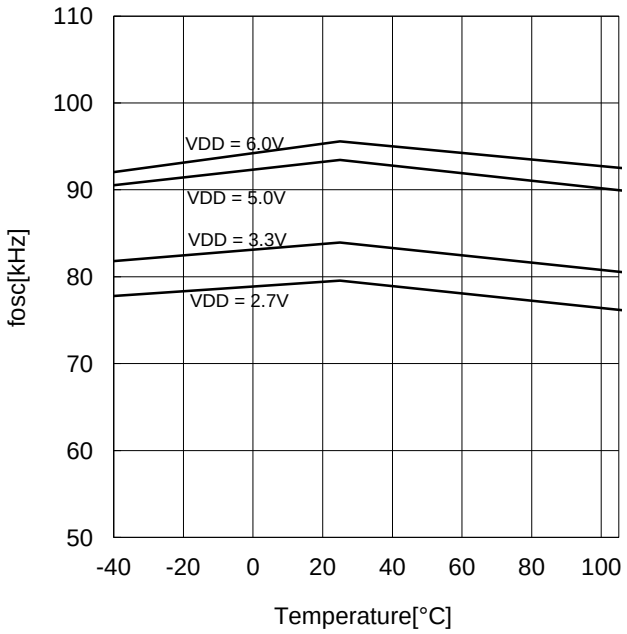


Figure 3. Typical Temperature Characteristics

Electrical Characteristics - continued

MPU Interface Characteristics (Ta = -40°C to 105°C, VDD = 2.7V to 6.0V, VSS = 0V, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Input Rise Time	tr	-	-	0.3	µs	
Input Fall Time	tf	-	-	0.3	µs	
SCL Cycle Time	tCYC	2.5	-	-	µs	
“H” Level SCL Pulse Width	tHW	0.6	-	-	µs	
“L” Level SCL Pulse Width	tLW	1.3	-	-	µs	
SDA Setup Time	tSDS	100	-	-	ns	
SDA Hold Time	tSDH	100	-	-	ns	
Bus Free Time	tBUF	1.3	-	-	µs	
START Condition Hold Time	tHD;STA	0.6	-	-	µs	
START Condition Setup Time	tSU;STA	0.6	-	-	µs	
STOP Condition Setup Time	tSU;STO	0.6	-	-	µs	

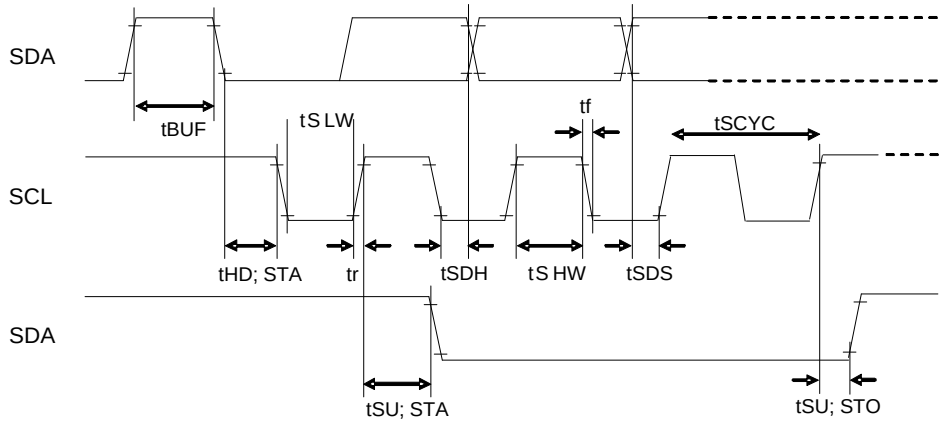


Figure 4. Interface Timing

I/O Terminal Equivalence Circuit Diagrams

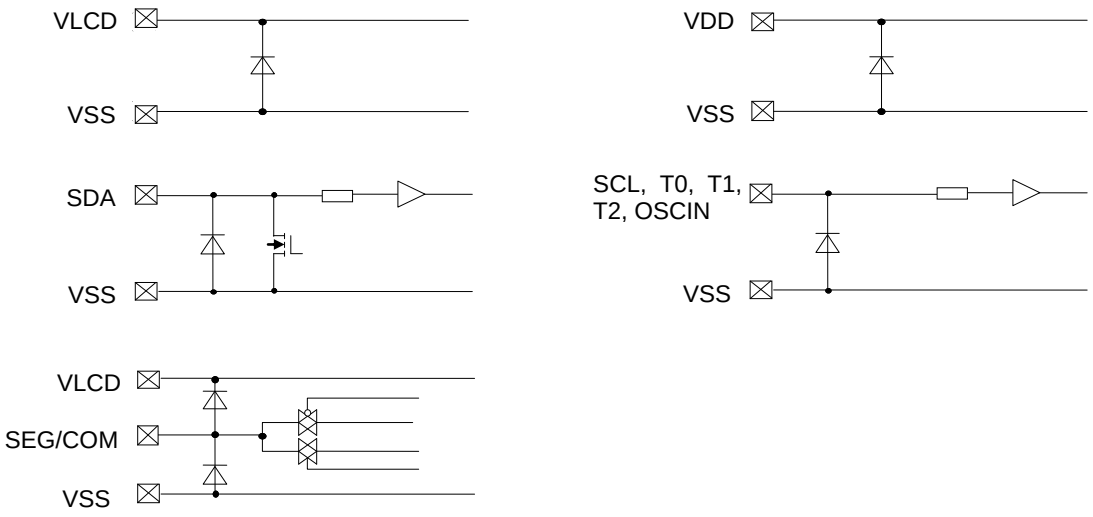


Figure 5. I/O Equivalence Circuit

Functional Descriptions
Command / Data Transfer Method

BU91R63CH-M3BW is controlled by 2-wire signal (SDA, SCL).

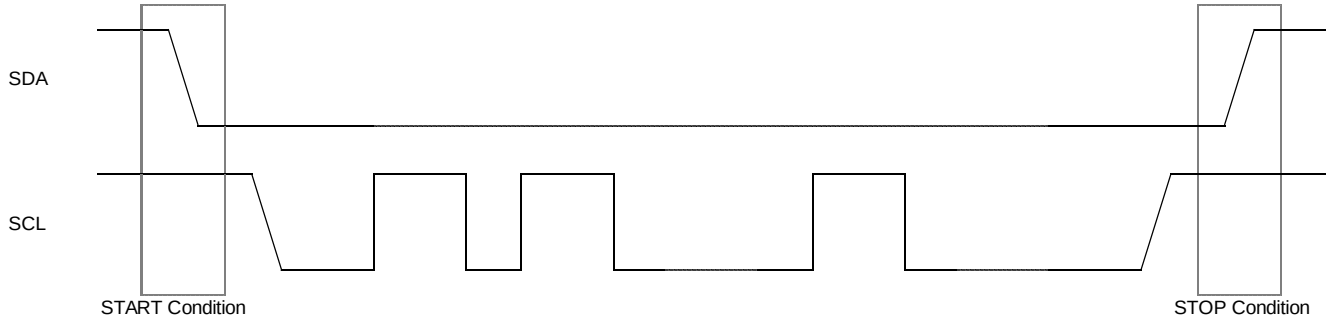


Figure 6. 2 wire Command/Data Transfer Format

It is necessary to generate START and STOP condition when sending command or display data through the 2 wire serial interface.

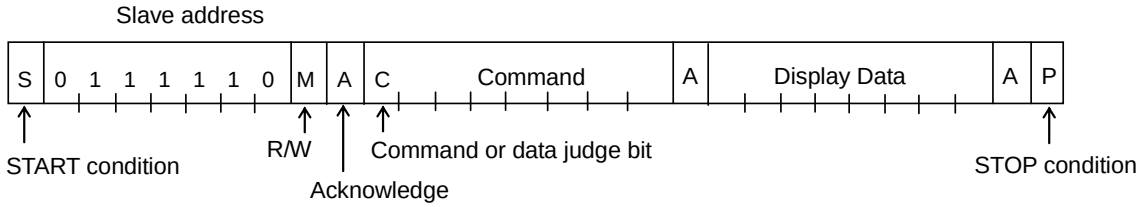


Figure 7. Interface Protcol

The following procedure shows how to transfer command and display data.
(1) Generate “START condition”.
(2) Issue Slave address.
(3) Transfer command and display data.
(4) Generate “STOP condition”

Acknowledge (ACK)

Data format is comprised of 8 bits, Acknowledge bit is returned after sending 8-bit data.
After the transfer of 8-bit data (Slave Address, Command, Display Data), release the SDA line at the falling edge of the 8th clock. The SDA line is then pulled “Low” until the falling edge of the 9th clock SCL.
(Output cannot be pulled “High” because of open drain NMOS).
If acknowledge function is not required, keep SDA line at “Low” level from 8th falling edge to 9th falling edge of SCL.

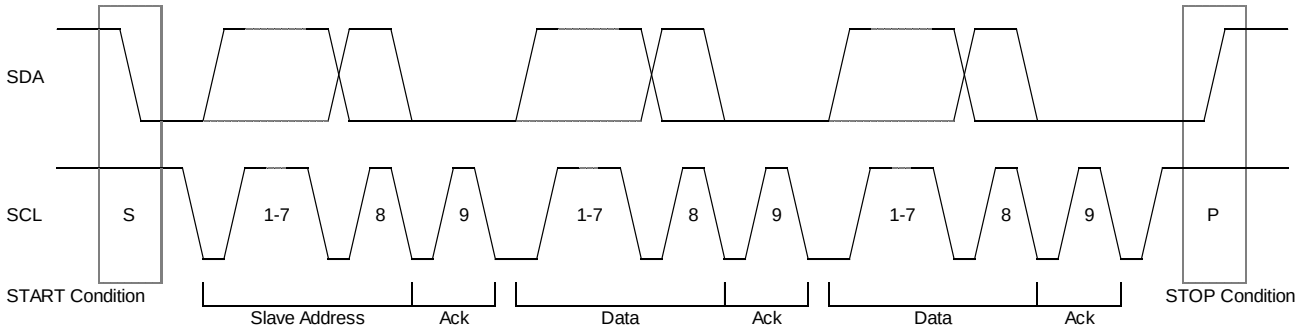
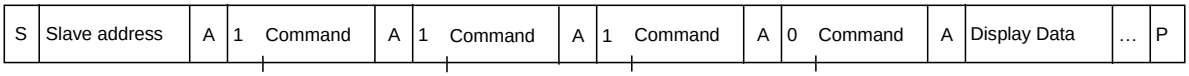


Figure 8. Acknowledge Timing

Command Transfer Method

Issue Slave Address (“01111100”) after generating “START condition”.
The 1st byte after Slave Address always becomes command input.
MSB (“command or data judge bit”) of command decide to next data is command or display data.
When set “command or data judge bit”=‘1’, next byte will be command.
When set “command or data judge bit”=‘0’, next byte data is display data.

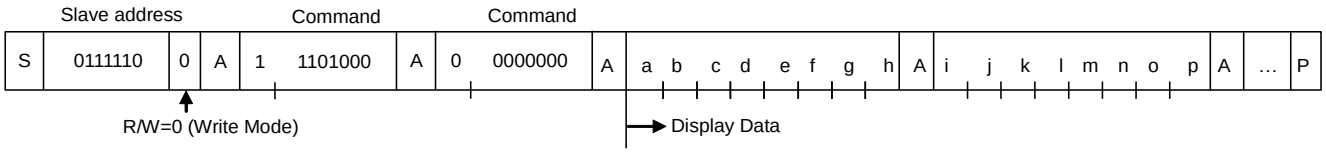


It cannot accept input command once it enters into display data transfer state.
In order to input command again it is necessary to generate “START condition”.
If “START condition” or “STOP condition” is sent in the middle of command transmission, command will be cancelled.
If Slave address is continuously sent following “START condition”, it remains in command input state.
“Slave address” must be sent right after the “START condition”.
When Slave Address cannot be recognized in the first data transmission, no Acknowledge bit is generated and next transmission will be invalid. When data is invalid status, if “START condition” is transmitted again, it will return to valid status.

Consider the MPU interface characteristic such as Input rise time and Setup/Hold time when transferring command and data (Refer to MPU Interface).

Write Display Data and Transfer Method

For Write Mode set R/W bit to “0”.
BU91R63CH-M3BW has Display Data RAM (DDRAM) of 44×4=176bit.
The relationship between data input and display data, DDRAM data and address are as follows.



8-bit data is stored in DDRAM. ADSET command specifies the address to be written, and address is automatically incremented in every 4-bit data.
Data can be continuously written in DDRAM by transmitting data continuously.
When RAM data is written successively, after writing RAM data to 2Bh (SEG43), the address is returned to 00h (SEG0) by the auto-increment function

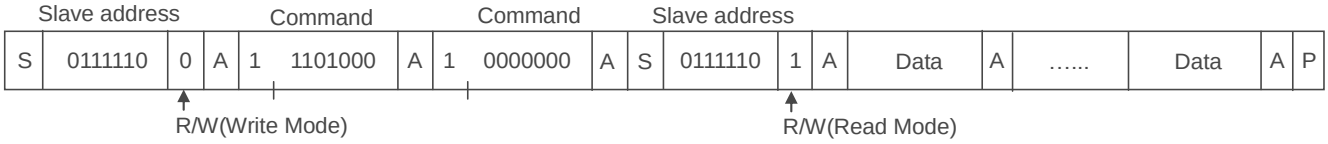
DDRAM address

BIT	00h	01h	02h	03h	04h	05h	06h	07h	···	29h	2Ah	2Bh	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7		SEG 41	SEG 42	SEG 43	

Display data is written to DDRAM every 4-bit data.
No need to wait for ACK bit to complete data transfer.

Read Display and Transfer Method

For Read Mode set R/W bit to '1'.
The display data and command register value can be read during Read Mode.
The Read Mode sequence is shown below.



During Read Mode, the display data can be read from the DDRAM through the SDA line.
The data will output synchronously to SCL clock input.
First set address by Write Mode ADSET command to read display data.
If DDRAM address is not specified before DDRAM read, the read address will start from the current DDRAM address.
Address will increment automatically by +2 addresses after 8bit data output.
Master side should output ACK signal after each 8bit data output.
BU91R63CH-M3BW is kept at Read Mode and address increment after receiving ACK signal from master side.
If there is no ACK response, BU91R63CH-M3BW will not keep above read operation, transmit "STOP condition".
Read Mode will be stopped by sending "STOP condition".
Address will be set to 00h automatically after 2Bh. (It does not increment to 2Ch or 2Dh address)

Shown below is an example of the display data read sequence.

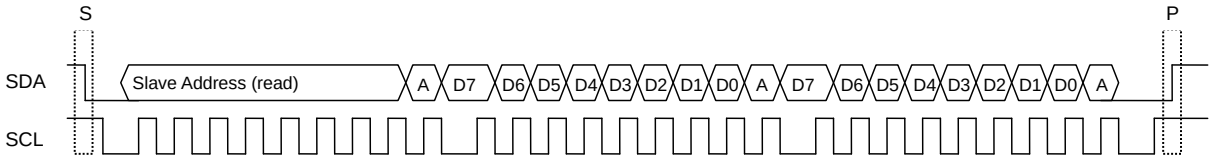
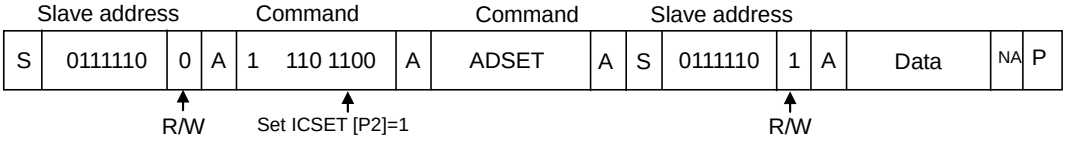


Figure 9. Read Sequence

Read Command Register and Transfer Method

The command registers can be read during Read Mode. The sequence for the command register read is shown below and is similar to the display data read sequence.



Regarding address setting, refer to ADSET command.
The following register settings can be read in this mode by setting address to 2Ch, 2Dh, and 2Eh.
Address does not increment automatically after command register value read.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	P7	P6	P5	P4	P3	P2	P1	P0	2Ch
REG2	P7	P6	P5	P4	P3	P2	P1	P0	2Dh
REG3	0	0	0	0	P3	P2	P1	P0	2Eh

REG1: P7 = Duty setting
P6 = Duty setting
P5 = 1/2Bias/1/3Bias setting
P4 = Internal/External clock setting
P3 = Software Reset setting
P2 to P0 = Blink setting

REG2: P7 to P6 = Frame Frequency setting
P5 to P4 = Power Save Mode setting
P3 = Frame/Line inversion setting
P2 = Display ON/OFF setting
P1 = All Pixels ON setting
P0 = All Pixels OFF setting

REG3: P3 = Contrast setting
P2 = Contrast setting
P1 = Contrast setting
P0 = Contrast Setting

The ADSET and ICSET setting address map is shown below.

Write Mode	ADSET				ICSET							
RAM Address	D7	D6	D5	D[4:0]	*P7*	*P6*	*P5*	*P4*	*P3*	*P2*(Note)	*P1*	*P0*
0000 0000 to 0001 1111	0	0	0	*0 0000* to *1 1111*	*1*	*1*	*1*	*0*	*1*	*0*	*0*	*0*
0010 0000 to 0010 1011	0	0	0	*0 0000* to *0 1011*	*1*	*1*	*1*	*0*	*1*	*1*	*0*	*0*
Read Mode	ADSET				ICSET							
RAM Address	D7	D6	D5	D[4:0]	*P7*	*P6*	*P5*	*P4*	*P3*	*P2*(Note)	*P1*	*P0*
0000 0000 to 0001 1111	1	0	0	*0 0000 to 1 1111*	*1*	*1*	*1*	*0*	*1*	*0*	*0*	*0*
0010 0000 to 0010 1110	1	0	0	*0 0000 to 0 1110*	*1*	*1*	*1*	*0*	*1*	*1*	*0*	*0*

(Note) Please take care of ICSET [P2] setting.

Oscillator

The clock signals for logic and analog circuit can be generated from internal oscillator or external clock.
If internal oscillator circuit is used, OSCIN must be connected to VSS level.
When using external clock mode, input external clock from OSCIN terminal after ICSET command setting.

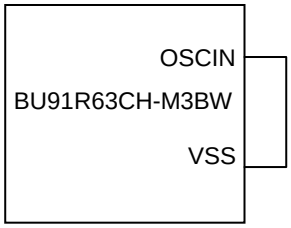


Figure 10. Internal Clock Mode

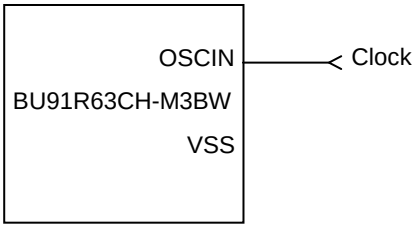


Figure 11. External Clock Mode

LCD Driver Bias Circuit

BU91R63CH-M3BW generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
1/3 or 1/2 Bias can be set by MODESET command.
Line or frame inversion can be set by DISCTL command.
Refer to the “LCD driving waveform” for each LCD bias setting.

Blinker Timing Generator

BU91R63CH-M3BW has Blink function.
Blink mode is asserted by BLKCTL command.
The Blink frequency varies depending on fCLK characteristics at internal clock mode.
Refer to Oscillation Characteristics for fCLK.

Reset Initialize Condition

Initial condition after executing Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Command Description for initial value of registers.

Command / Function List

Description List of Command / Function

No.	Command	Function
1	Set IC Operation (ICSET)	Software reset, internal/external clock setting (P2 is MSB data of DDRAM address)
2	Display Control (DISCTL)	Frame Frequency, Power Save Mode setting
3	Address Set (ADSET)	DRAM address setting Register address setting
4	Mode Set (MODESET)	Display ON/OFF, Bias, Duty
5	Blink Control (BLKCTL)	Blink off/0.5s/1s/2s/0.3s/0.2s blink setting
6	All Pixels Control (APCTL)	All Pixels ON/OFF during DISPON
7	Contrast Setting (EVRSET)	Contrast Setting

Detailed Command Description

D7 (MSB) is a command or data judgment bit.
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

Set IC Operation (ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2: MSB data of DDRAM address. Please refer to “ADSET” command.

Set software reset execution.

Setup	P1
No operation	0
Software Reset Execute	1

When “Software Reset” is executed, BU91R63CH-M3BW is reset to initial condition.
(Refer to Reset initialize condition)
Don’t set Software Reset (P1) with P2, P0 at the same time.

Set oscillator mode

Setup	P0	Reset initialize condition
Internal clock	0	○
External clock	1	

Internal clock mode: OSCIN must be connected to VSS level.
External clock mode: Input external clock from OSCIN terminal.

<Frame frequency Calculation at external clock mode>
DISCTL 80Hz setting: Frame frequency [Hz] = external clock [Hz] / 512
DISCTL 130Hz setting: Frame frequency [Hz] = external clock [Hz] / 315
DISCTL 64Hz setting: Frame frequency [Hz] = external clock [Hz] / 648
DISCTL 200Hz setting: Frame frequency [Hz] = external clock [Hz] / 205

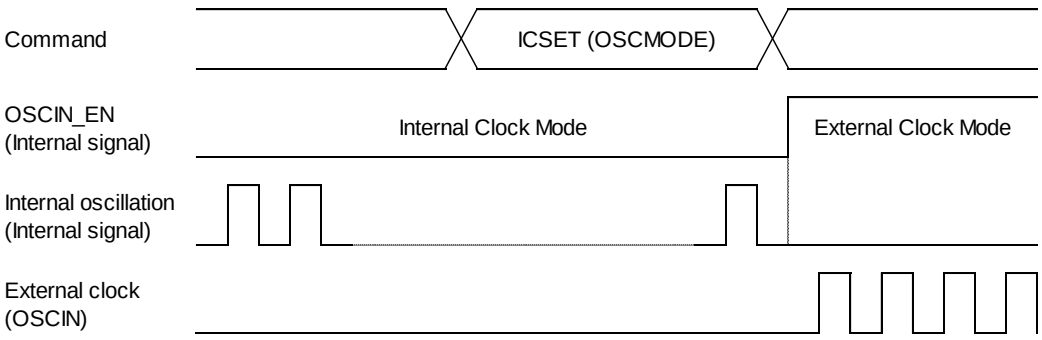


Figure 12. OSC MODE Switch Timing

Display Control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Frame Frequency.

Setup	P4	P3	Reset initialize condition
80Hz	0	0	○
130Hz	0	1	
64Hz	1	0	
200Hz	1	1	

Set LCD Drive Waveform.

Setup	P2	Reset initialize condition
Line Inversion Mode	0	○
Frame Inversion Mode	1	

Power consumption is reduced in the following order:
Line inversion > Frame inversion
Typically, when driving large capacitance LCD, Line inversion is more susceptible to influence of crosstalk.
Regarding driving waveform, refer to LCD driving waveform.

Set Power Save Mode

Setup	P1	P0	Reset initialize condition
Power Save Mode 1	0	0	
Power Save Mode 2	0	1	
Normal Mode	1	0	○
High Power Mode	1	1	

Power consumption is increased in the following order:
Power Save Mode 1 < Power Save Mode 2 < Normal Mode < High Power Mode

Address Set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

The range of address in the Write Mode can be set from 000000 to 101011(bin).
The range of address in the Read Mode can be set from 000000 to 101110(bin).

	MSB					LSB
Internal Register	Address [5]	Address [4]	Address [3]	Address [2]	Address [1]	Address [0]
Command	ICSET P2	ADSET P4	ADSET P3	ADSET P2	ADSET P1	ADSET P0

Address [5:0]: MSB bit is specified in ICSET P2 and [4:0] are specified as ADSET P4 - P0.
Don't set out of range address, otherwise address will be set to 000000.

Mode Set (MODE SET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	0	P3	P2	P1	P0

Set display ON and OFF

Setup	P3	Reset initialize condition
Display OFF (DISPOFF)	0	○
Display ON (DISPON)	1	

Display OFF : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1frame of data write. Display OFF mode will be disabled after Display ON command.
Display ON : SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

Set Bias Level

Setup	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

Please refer to LCD drive waveform, for example of SEG and COM output waveform

Set Duty

Setup	P1	P0	Reset initialize condition
1/4 Duty	0	0	○
1/3 Duty	0	1	
1/2 Duty	1	0	
Static	1	1	

Blink Control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	P2	P1	P0

Set Blink condition.

Blink mode (Hz)	P2	P1	P0	Reset initialize condition
OFF	0	0	0	○
0.5	0	0	1	
1	0	1	0	
2	0	1	1	
0.3	1	0	0	
0.2	1	0	1	

The Blink frequency varies depending on fCLK characteristics at internal clock mode.
Refer to Oscillation Characteristics for fCLK.

All Pixels Control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	P2	P1	P0

All display Set ON, OFF

Setup	P1	Reset initialize condition
Normal	0	○
All Pixels ON	1	

Setup	P0	Reset initialize condition
Normal	0	○
All Pixels OFF	1	

All Pixels ON: All pixels are ON regardless of DDRAM data.
All Pixels OFF: All pixels are OFF regardless of DDRAM data.

This command is valid in Display on status. The data of DDRAM is not changed by this command.
If set both P1 and P0 =”1”, All Pixels OFF will be selected.

P2 is used for P3 of Contrast Setting.

Contrast Setting (EVRSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	0	P2	P1	P0

BU91R63CH-M3BW has 16-step Electrical Volume Register (EVR) that can set the best V0 voltage level (Maximum LCD driving voltage).
Electrical Volume Register (EVR) is set to “0000” in reset initialize condition.
In “0000” condition, V0 output voltage is equal to VLCD input voltage.
Keep Contrast Setting for V0 voltage more than 2.7V only.
Refer to the below table for V0 voltage.

Contrast Setting (V0 voltage)	P3(Note)	P2	P1	P0	Reset initialize condition
1.000 * VLCD	0	0	0	0	○
0.975 * VLCD	0	0	0	1	
0.950 * VLCD	0	0	1	0	
0.925 * VLCD	0	0	1	1	
0.900 * VLCD	0	1	0	0	
0.875 * VLCD	0	1	0	1	
0.850 * VLCD	0	1	1	0	
0.825 * VLCD	0	1	1	1	
0.800 * VLCD	1	0	0	0	
0.775 * VLCD	1	0	0	1	
0.750 * VLCD	1	0	1	0	
0.725 * VLCD	1	0	1	1	
0.700 * VLCD	1	1	0	0	
0.675 * VLCD	1	1	0	1	
0.650 * VLCD	1	1	1	0	
0.625 * VLCD	1	1	1	1	

(Note) P3 setting uses P2 of APCTL.

LCD Driving Waveform

(1/4duty, 1/3bias)

Line Inversion

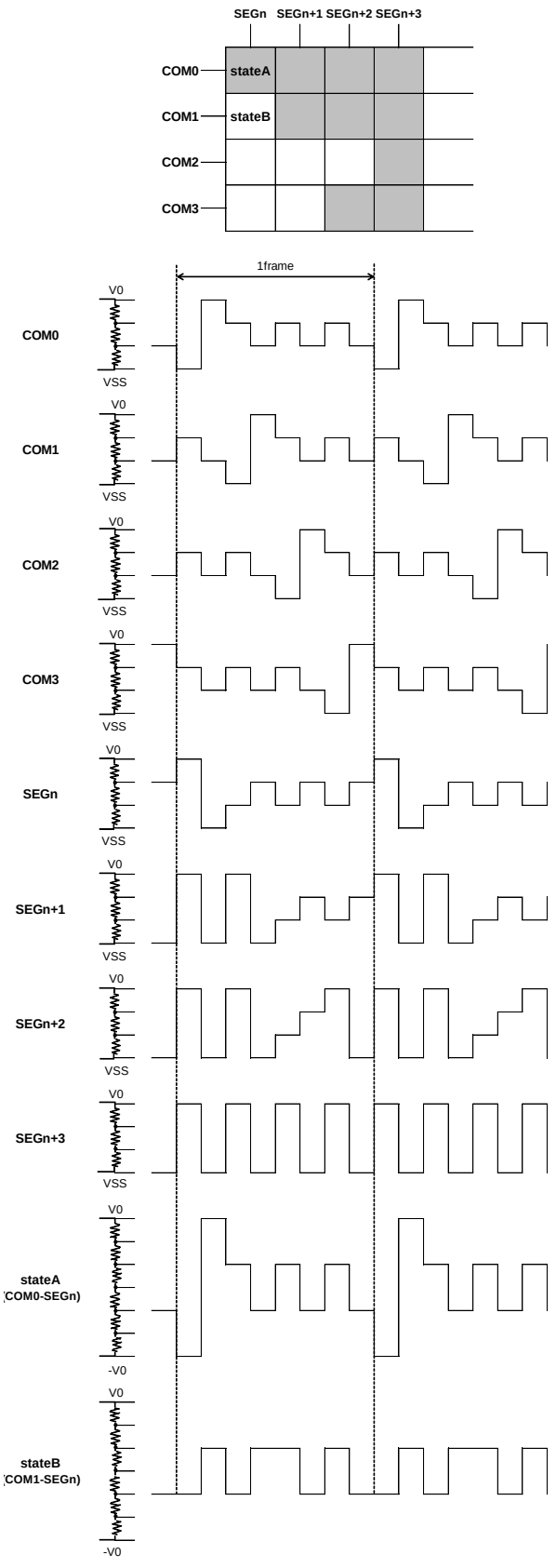


Figure 13. LCD Waveform at Line Inversion

Frame Inversion

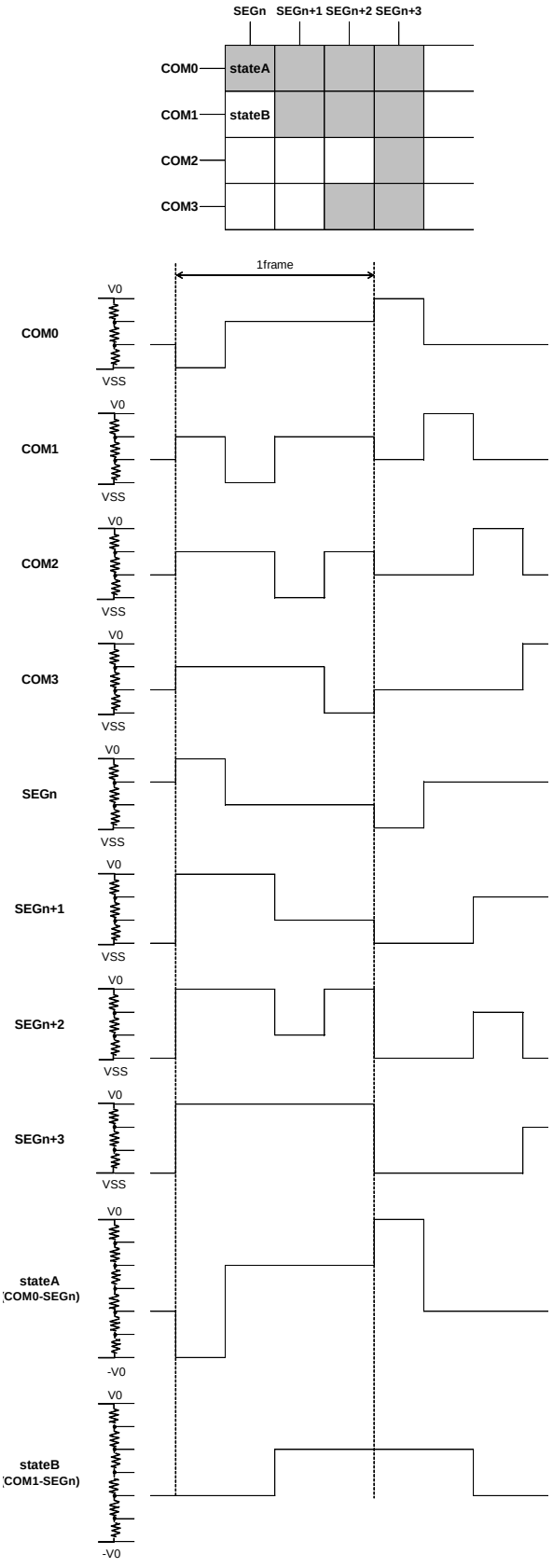


Figure 14. LCD Waveform at Frame Inversion

(1/4duty, 1/2bias)

Line Inversion

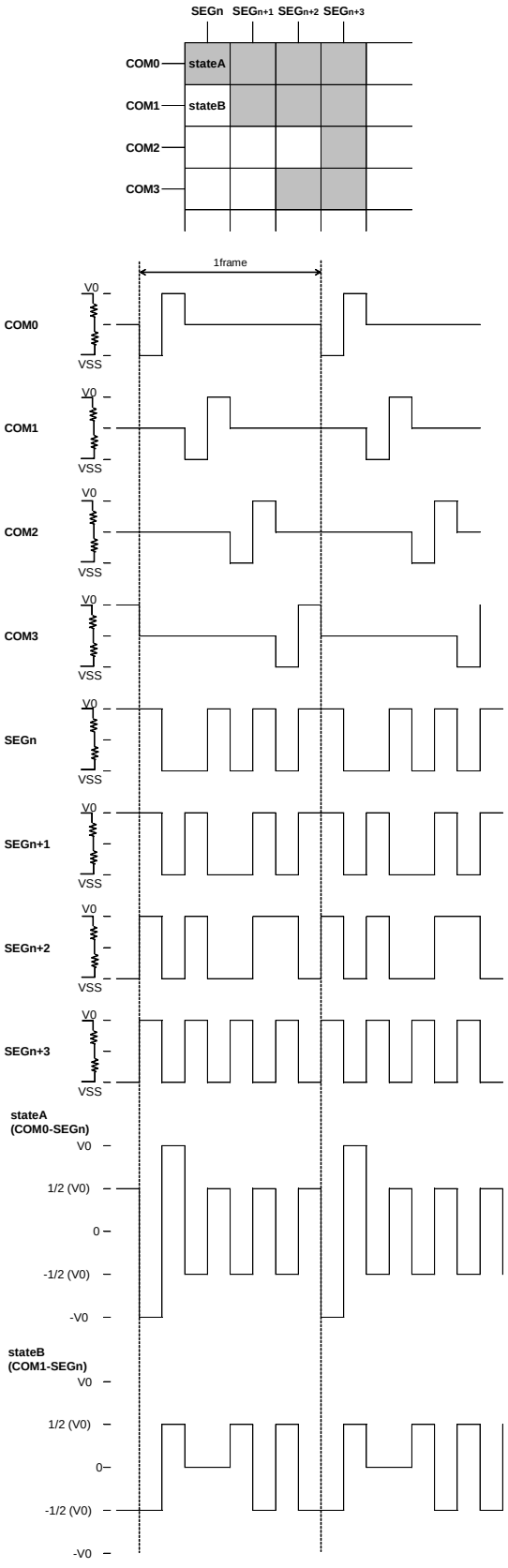


Figure 15. LCD Waveform in Line Inversion

Frame Inversion

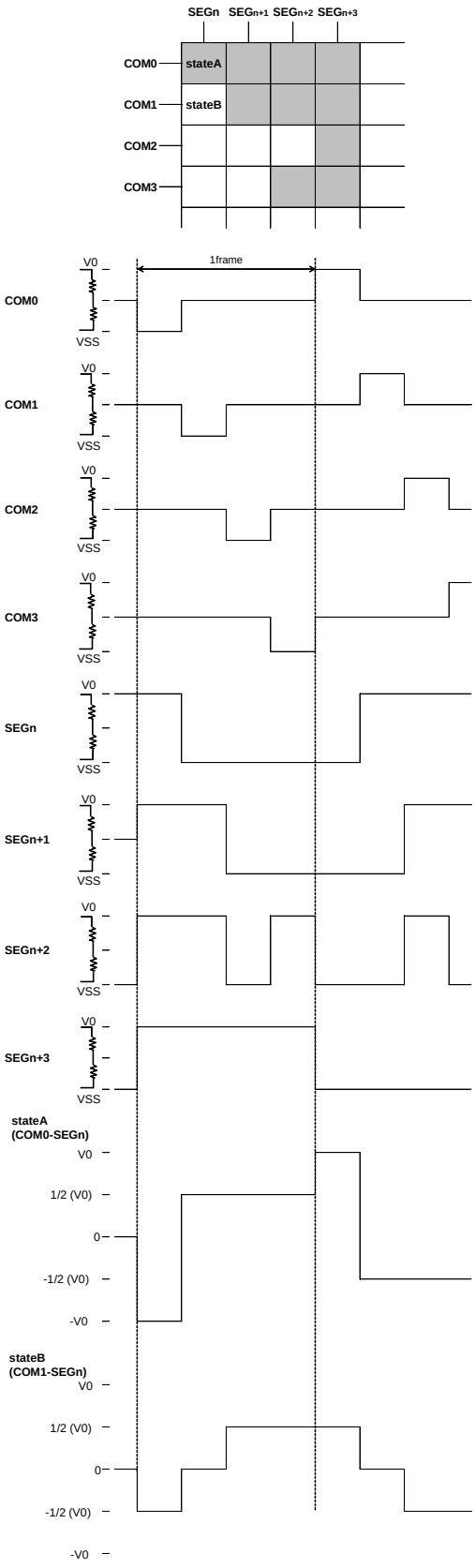


Figure 16. LCD Waveform in Frame Inversion

(1/3duty, 1/3bias)

Line Inversion

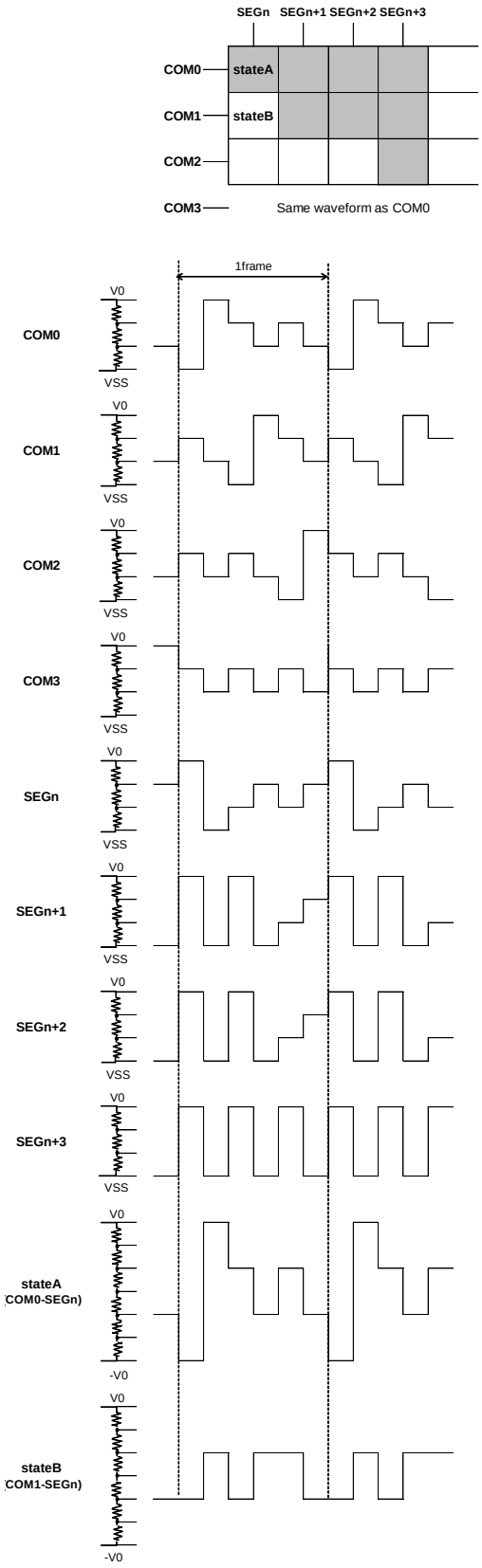


Figure 17. LCD Waveform in Line Inversion

Frame Inversion

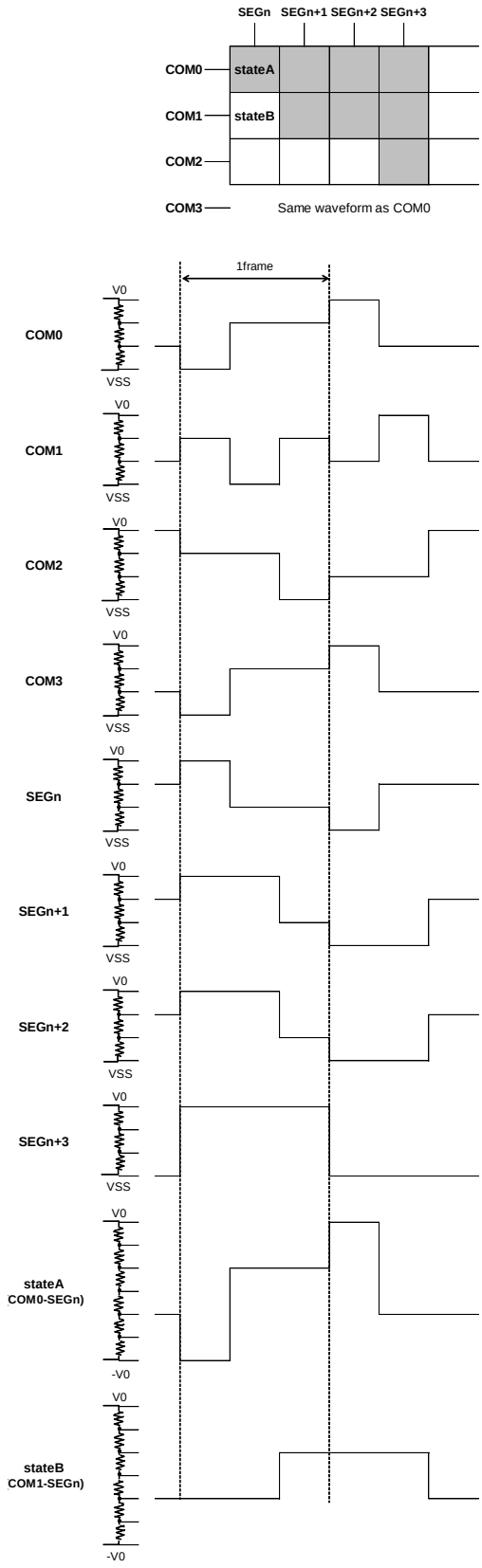


Figure 18. LCD Waveform in Frame Inversion

(1/3duty, 1/2bias)

Line Inversion

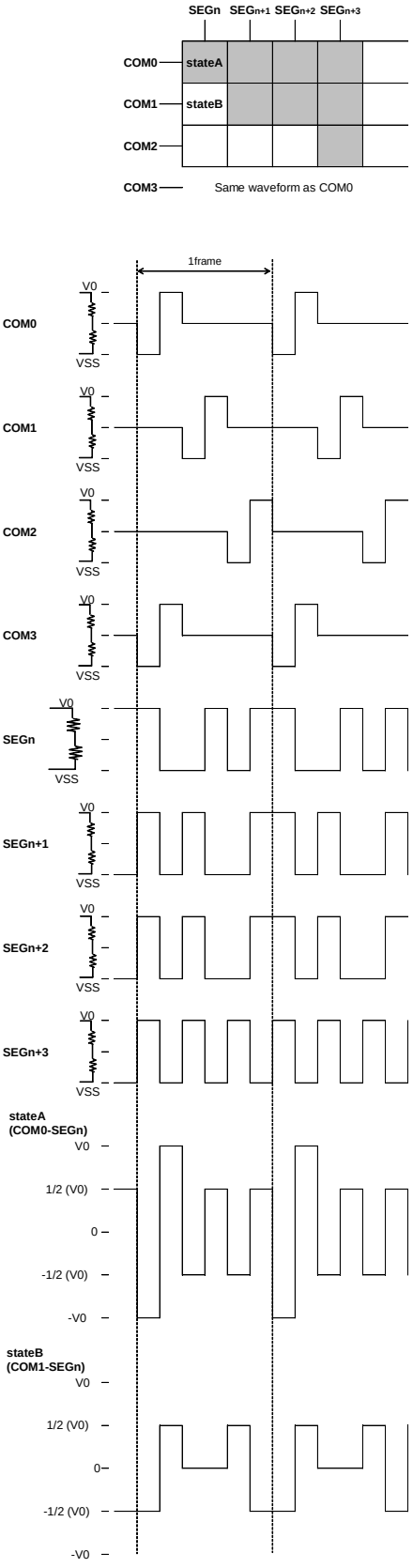


Figure 19. LCD Waveform in Line Inversion

Frame Inversion

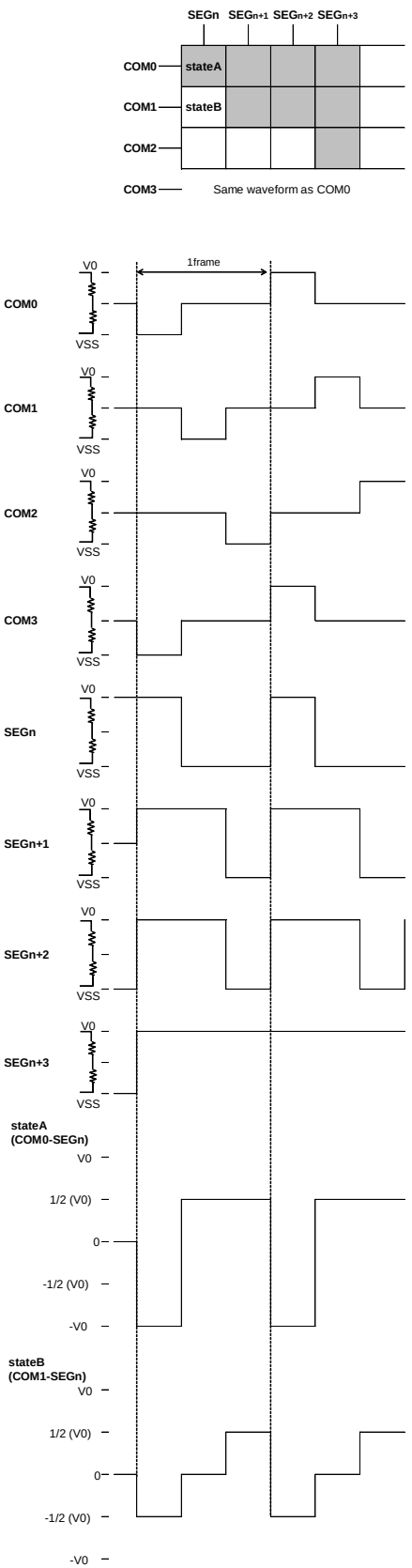
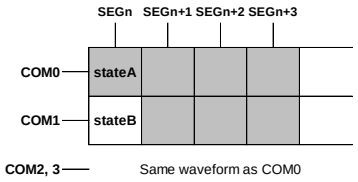


Figure 20. LCD Waveform in Frame Inversion

(1/2duty, 1/3bias)

Line Inversion



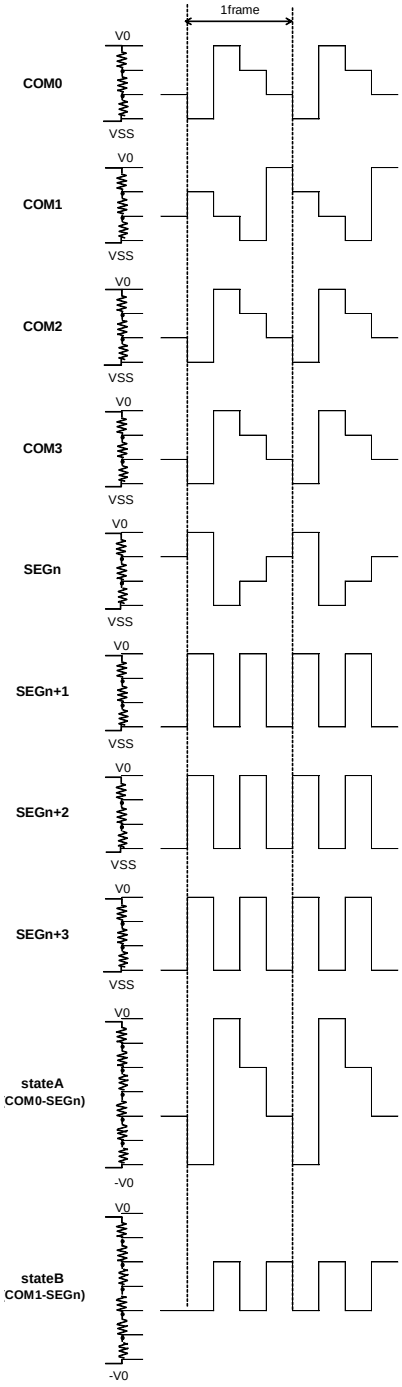
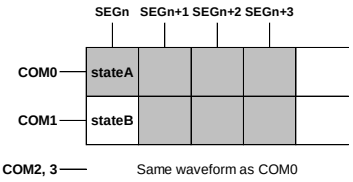


Figure 21. LCD Waveform in Line Inversion

Frame Inversion



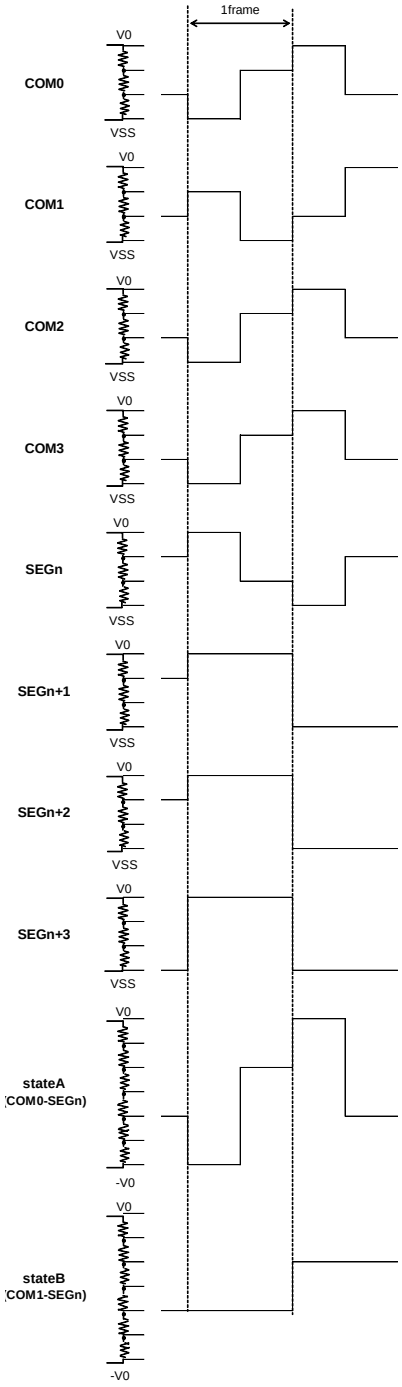
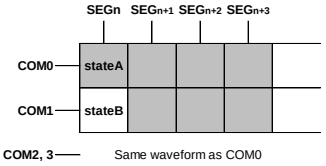


Figure 22. LCD Waveform in Frame Inversion

(1/2duty, 1/2bias)

Line Inversion



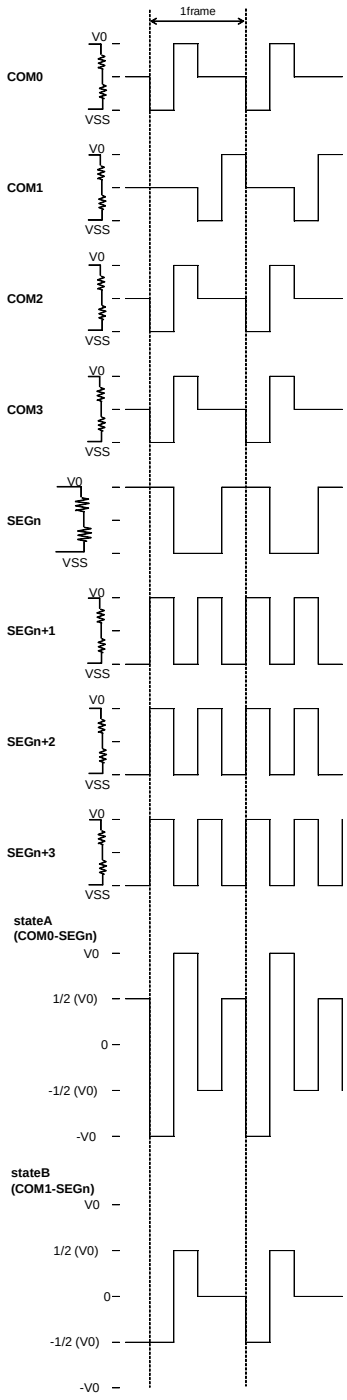
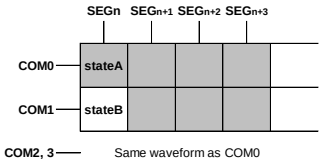


Figure 23. LCD Waveform in Line Inversion

Frame Inversion



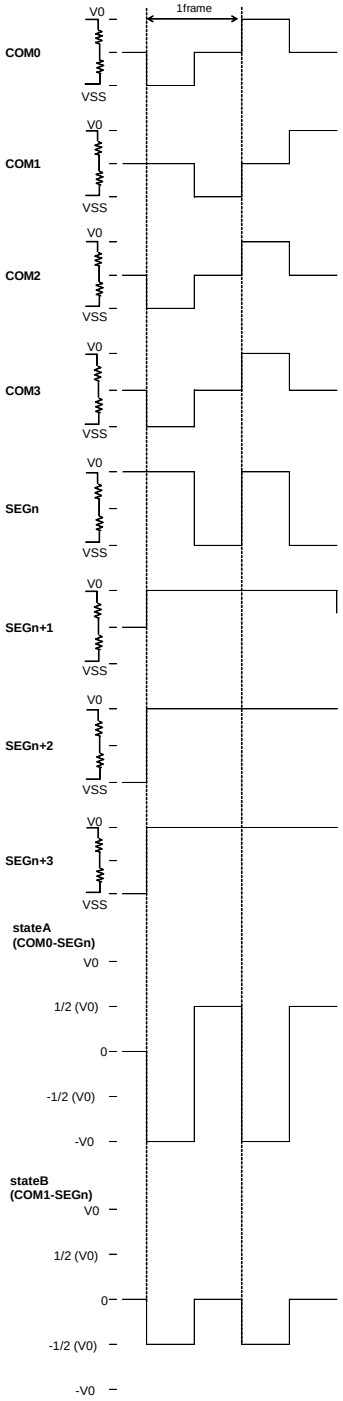
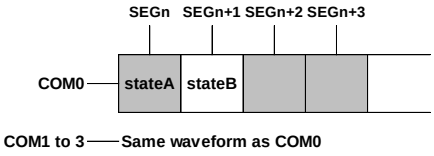


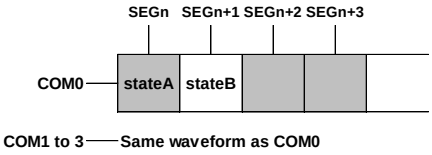
Figure 24. LCD Waveform in Frame Inversion

(Static)

Line Inversion



Frame Inversion



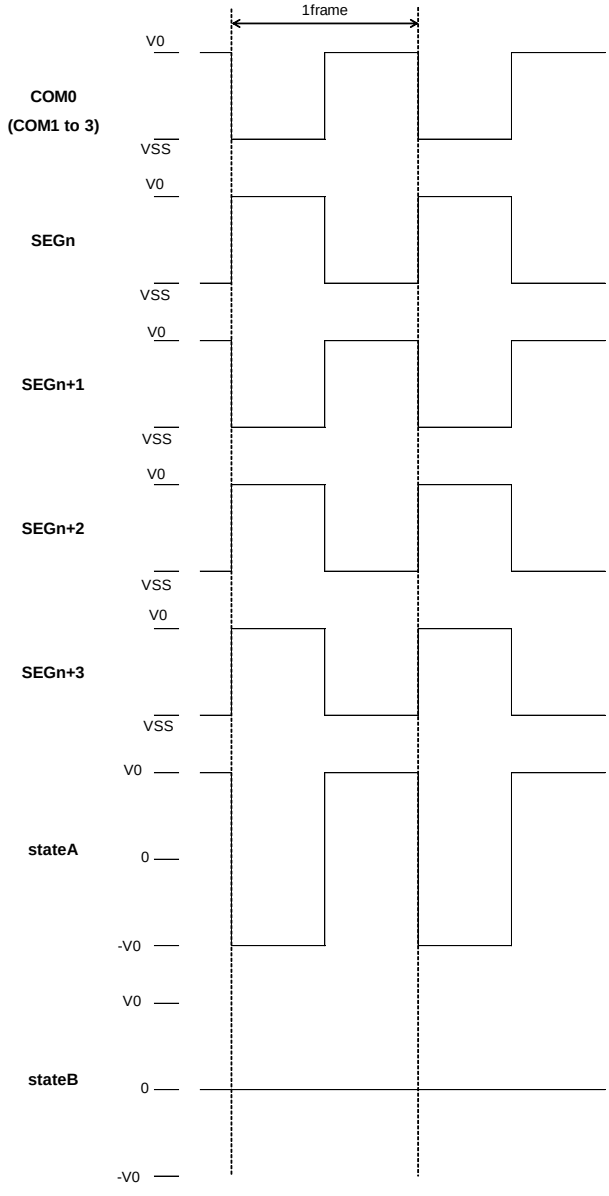


Figure 25. LCD Waveform in Line Inversion

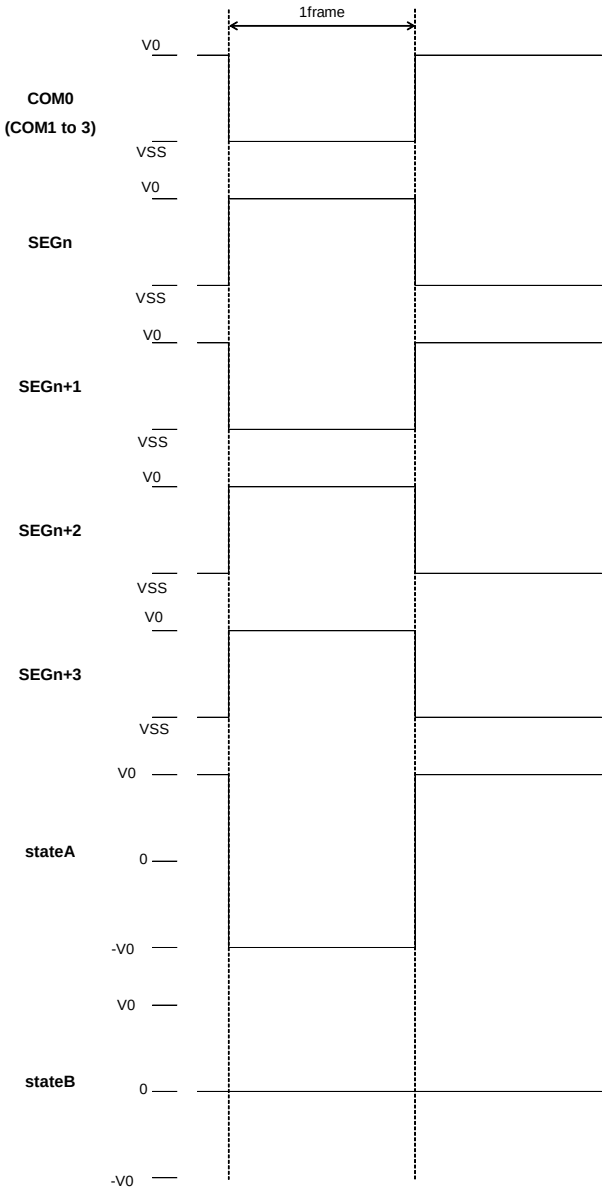


Figure 26. LCD Waveform in Frame Inversion

Example of Display Data

If LCD layout pattern is shown as in Figure 27 and 28 and DDRAM data is shown as in Table below, display pattern will be shown as in Figure 29.

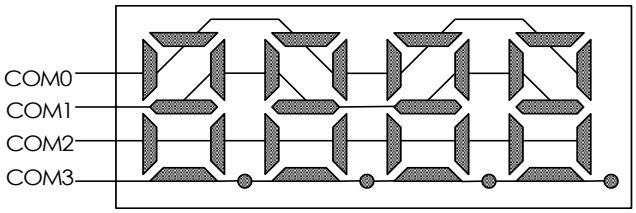


Figure 27. Example COM Line Pattern

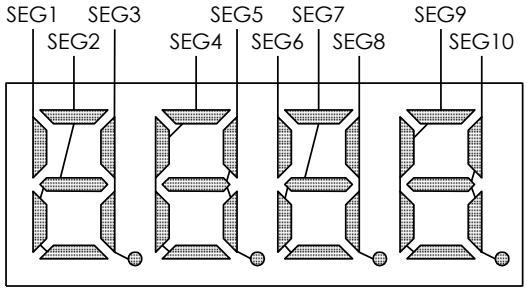


Figure 28. Example SEG Line Pattern

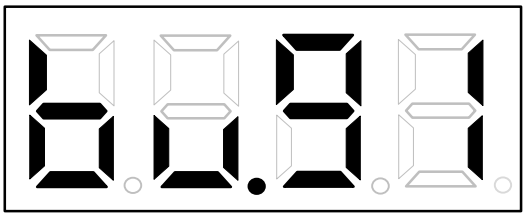


Figure 29. Example Display Pattern

<DDRAM data mapping in Figure 29 display pattern>

		SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	SEG 18	SEG 19
COM0	D0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
COM2	D2	0	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
COM3	D3	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Address		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

Initialize Sequence

Follow the Power-on sequence below to initialize condition.

Power on
↓
STOP condition
↓
START condition
↓
Issue slave address
↓
Execute Software Reset by sending ICSET command.

After Power-on and before sending initialize sequence, each register value, DDRAM address and DDRAM data are random.

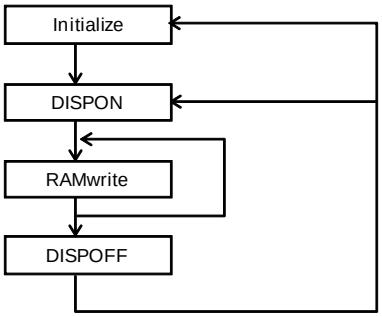
Start Sequence

Start Sequence Example1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power ON									VDD=0→3.3[V] (Tr=1[ms]) VLCD=0→5.0[V]
	↓									
2	wait 100us									Initialize
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
	↓									
5	Slave address	0	1	1	1	1	1	0	0	Issue Slave address
	↓									
6	ICSET	1	1	1	0	1	0	1	0	Software Reset
	↓									
7	BLKCTL	1	1	1	1	0	*	0	0	Blink OFF
	↓									
8	DISCTL	1	0	1	0	0	0	1	0	80Hz, Line Inversion, Normal mode
	↓									
9	APCTL	1	1	1	1	1	0	0	0	Set MSB of EVRSET
	↓									
10	EVRSET	1	1	1	0	0	0	0	0	EVRSET V0=1.00*VLCD
	↓									
11	ICSET	1	1	1	0	1	*	0	0	RAM MSB address set
	↓									
12	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
13	Display Data	*	*	*	*	*	*	*	*	address 00h - 01h
	Display Data	*	*	*	*	*	*	*	*	address 02h - 03h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	address 2Ah – 2Bh
	↓									
14	Stop									Stop condition
	↓									
15	Start									Start condition
	↓									
16	Slave address	0	1	1	1	1	1	0	0	Issue Slave address
	↓									
17	MODESET	1	1	0	0	1	0	0	0	Display ON, 1/4 Duty, 1/3Bias
	↓									
18	Stop									Stop condition

(*: don't care)

Start Sequence Example2



Initialize Sequence

DISPON Sequence

RAM write Sequence

DISPOFF Sequence

BU91R63CH-M3BW is initialized with “Initialize Sequence”, starts to display with “DISPON Sequence”, updates display data with “RAM Write Sequence” and stops the display with “DISPOFF Sequence”.
Execute “DISPON Sequence” in order to restart display.

Initialize Sequence (In case of VDD ≠ VLCD)

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
VDD ON									
wait 100us									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	7C
ICSET	1	1	1	0	1	0	1	0	Execute Software Reset
VLCD ON									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	7C
ICSET	1	1	1	0	1	0	1	0	Execute Software Reset
MODESET	1	1	0	0	0	0	0	0	Display OFF
ICSET	1	1	1	0	1	0	0	0	Set RAM Address
ADSET	0	0	0	0	0	0	0	0	Set RAM Address
Display data	*	*	*	*	*	*	*	*	Display data
⋮									
STOP									

Initialize Sequence (In case of VDD = VLCD)

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
VDD, VLCD ON									
wait 100us									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	7C
ICSET	1	1	1	0	1	0	1	0	Execute Software Reset
MODESET	1	1	0	0	0	0	0	0	Set Display OFF
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	Set RAM Address
Display data	*	*	*	*	*	*	*	*	Display data
⋮									
STOP									

DISPON Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	7C
ICSET	1	1	1	0	1	0	0	0	Set Internal OSC mode
DISCTL	1	0	1	0	0	0	1	0	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
EVRSET	1	1	1	0	0	0	0	0	Set Contrast Setting
MODESET	1	1	0	0	1	0	0	0	Display ON
STOP									

RAM Write Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	7C
DISCTL	1	0	1	0	0	0	1	0	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
EVRSET	1	1	1	0	0	0	0	0	Set Contrast Setting
MODESET	1	1	0	0	1	0	0	0	Display ON
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display Data	*	*	*	*	*	*	*	*	Display data
⋮									
STOP									

DISPOFF Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	7C
MODESET	1	1	0	0	0	0	0	0	Display OFF
STOP									

Abnormal operation may occur in BU91R63CH-M3BW due to the effect of noise or other external factor.
To avoid this phenomenon, it is highly recommended to input command according to sequence described above during initialization, display ON/OFF and refresh of RAM data.

Cautions in Power ON/OFF

Please keep Power ON/OFF sequence as below waveform.
To prevent incorrect display, malfunction and abnormal current,
VDD must be turned on before VLCD In power up sequence.
VDD must be turned off after VLCD In power down sequence.
Please satisfies t1>0ns, t2>0ns

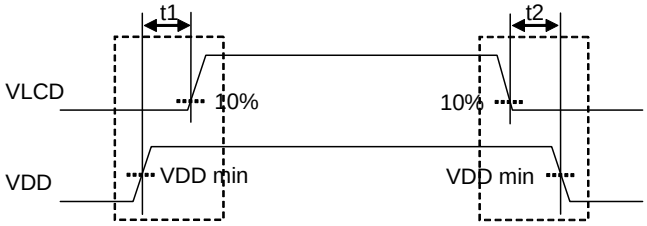


Figure 30. Recommended Power ON/OFF Sequence

BU91R63CH-M3BW has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Keep the following recommended Power-On conditions in order to power up properly.

Set power up conditions to meet the recommended tR, tF, tOFF, and Vbot specification below in order to ensure P.O.R operation.
Set pin T0=VSS to enable POR circuit.

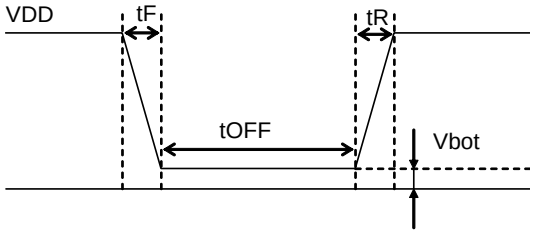


Figure 31. Power ON/OFF Waveform

Recommended condition of tR, tF, tOFF, Vbot (Ta=25°C)

tR(Note)	tF(Note)	tOFF(Note)	Vbot(Note)
1ms to 500ms	1ms to 500ms	Min 20ms	Less than 0.1V

(Note) This function is guaranteed by design, not tested in production process.

If it is difficult to keep above conditions, execute the following sequence as quickly as possible after Power-On.
Setting T0=VDD disables the POR circuit, in such case, execute the following sequence.
Note that however it cannot accept command while supply is unstable or below the minimum supply range.
Note also that software reset is not a complete alternative to POR function.

1. Generate STOP Condition

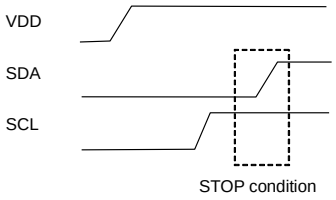


Figure 32. Stop Condition

2. Generate START Condition.

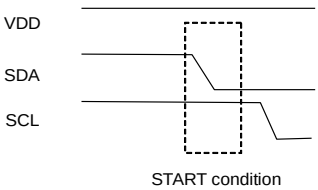


Figure 33. Start Condition

3. Issue Slave Address

4. Execute Software Reset (ICSET) Command

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Data transmission

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

Ordering Information

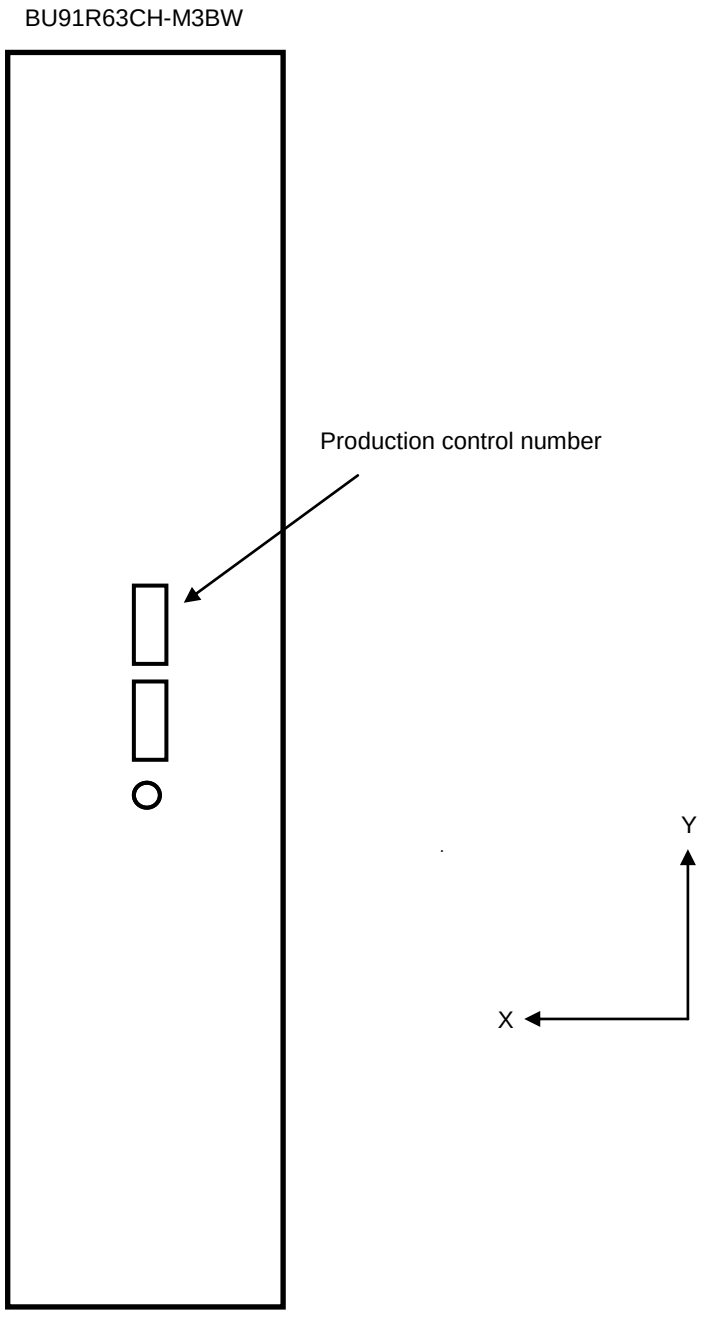
B	U	9	1	R	6	3	C	H	-	M3	B	W

Part Number

Lineup

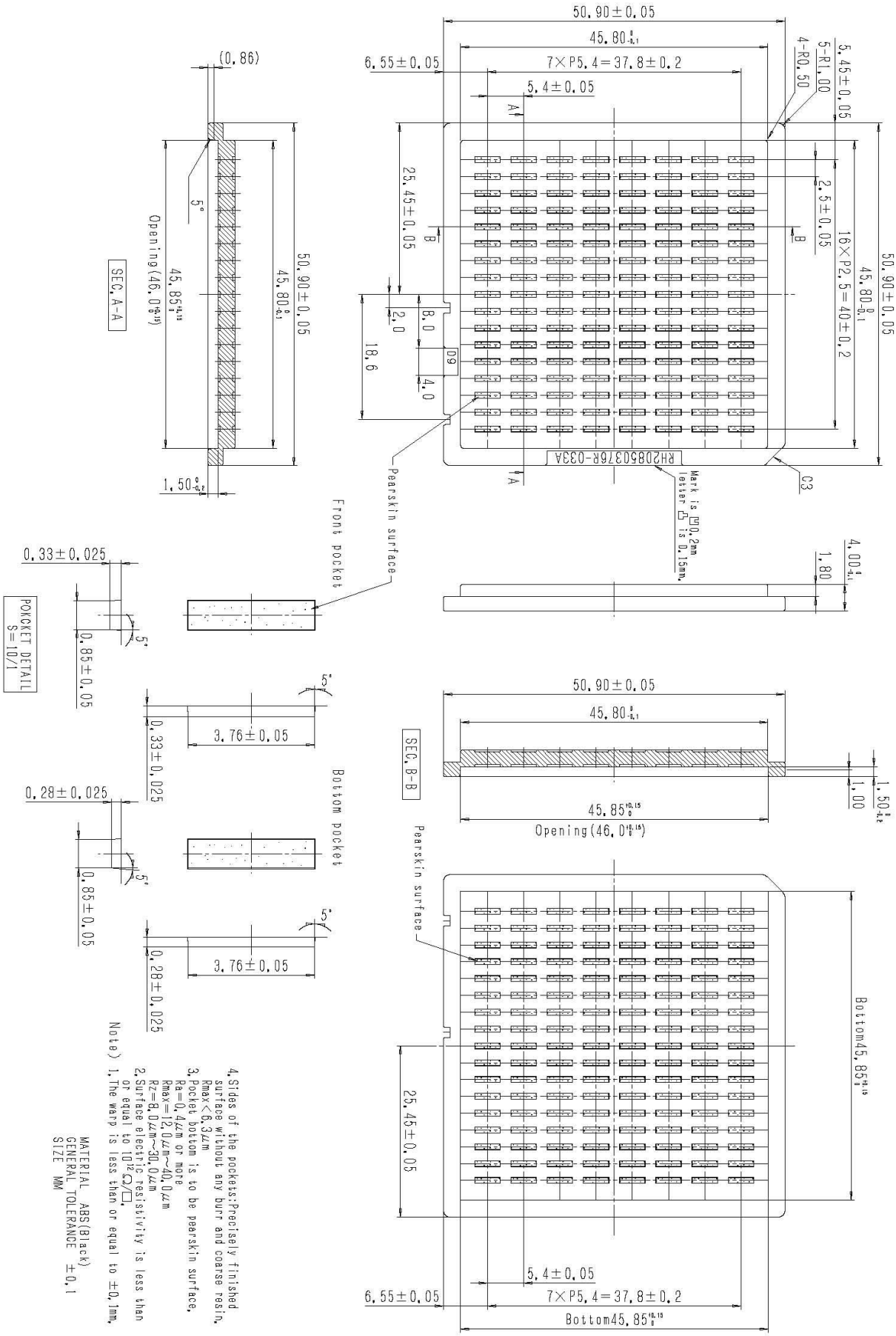
Package		Orderable Part Number
Au Bump with Tray	MOQ: 16,320pcs	BU91R63CH-M3BW

Marking Diagram



Physical Dimension Tray Information

Package Name	Au Bump with Tray



Revision History

Version	Release	Page	Change
001	10 Feb. 2016	-	First Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BU91R63CH-M3BW - Web Page

Part Number	BU91R63CH-M3BW
Package	Au BUMP chip
Unit Quantity	16320
Minimum Package Quantity	16320
Packing Type	Tray
Constitution Materials List	inquiry
RoHS	Yes