

**NPN Epitaxial Planar Transistor**

# BU941ZNF3

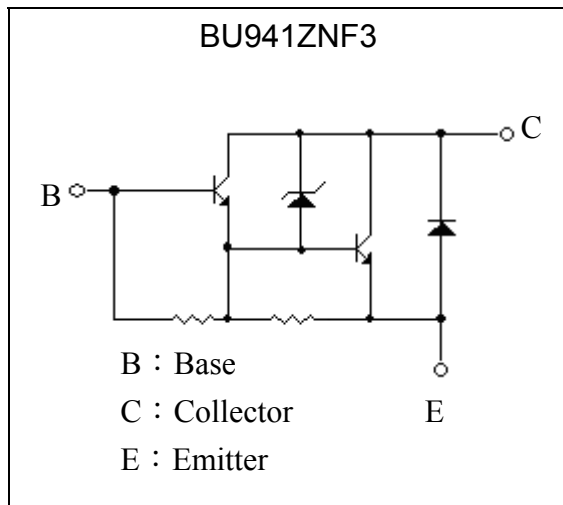
**Features**

- High  $BV_{CEO}$
- Low  $V_{CE(SAT)}$
- High current capability
- Built-in clamping zener
- Pb-free lead plating package

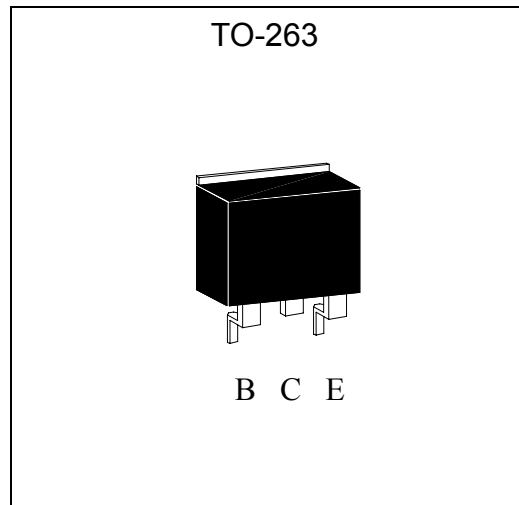
**Applications**

- High ruggedness electronic ignitions

**Equivalent Circuit**

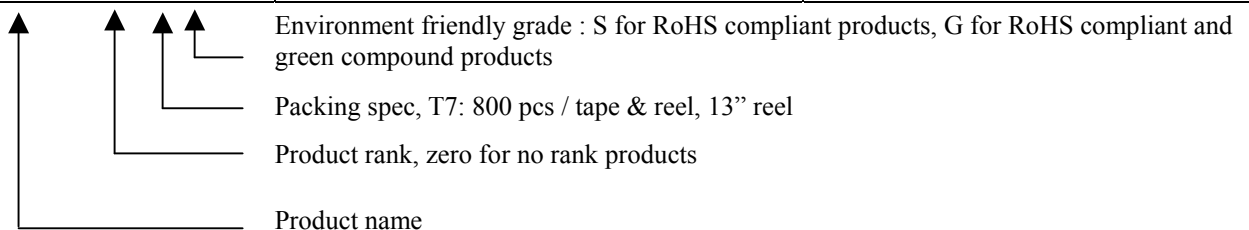


**Outline**



**Ordering Information**

Device	Package	Shipping
BU941ZNF3-0-T7-X	TO-263 (Pb-free lead plating package)	800pcs / tape & reel





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CBO</sub>	350	V
Collector-Emitter Voltage	V <sub>CEO</sub>	350	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C(DC)</sub>	15	A
	I <sub>C(Pulse)</sub>	30 *1	
Base Current	I <sub>B(DC)</sub>	1	A
	I <sub>B(Pulse)</sub>	5 *1	
Power Dissipation	Pd(T <sub>A</sub> =25°C)	2	W
	Pd(T <sub>C</sub> =25°C)	150	
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	75	°C/W
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	1	°C/W
Junction Temperature	T <sub>j</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-65~+175	°C

Note : \*1. Single Pulse Pw=10ms

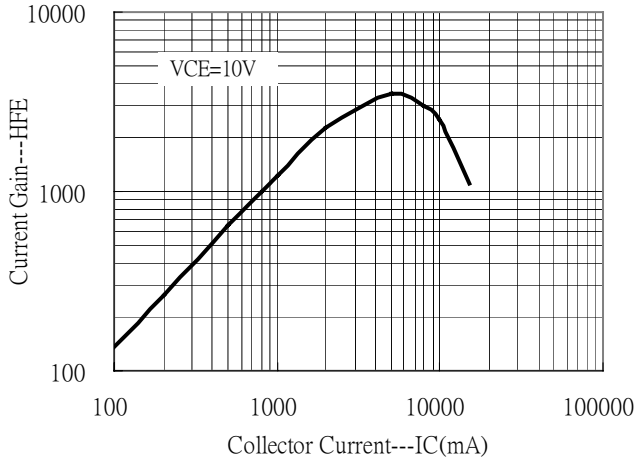
**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	350	-	450	V	I <sub>C</sub> =1mA, I <sub>E</sub> =0
BV <sub>CEO</sub>	350	-	450	V	I <sub>C</sub> =100mA, I <sub>B</sub> =0
I <sub>CEO</sub>	-	-	100	μA	V <sub>CE</sub> =350V, I <sub>E</sub> =0
I <sub>CBO</sub>	-	-	100	μA	V <sub>CB</sub> =350V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	10	mA	V <sub>EB</sub> =5V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub> 1	-	-	1.6	V	I <sub>C</sub> =6A, I <sub>B</sub> =10mA
*V <sub>CE(sat)</sub> 2	-	-	1.5	V	I <sub>C</sub> =8A, I <sub>B</sub> =100mA
*V <sub>CE(sat)</sub> 3	-	-	1.6	V	I <sub>C</sub> =10A, I <sub>B</sub> =250mA
*V <sub>BE(sat)</sub> 1	-	-	2.2	V	I <sub>C</sub> =8A, I <sub>B</sub> =100mA
*V <sub>BE(sat)</sub> 2	-	-	2.5	V	I <sub>C</sub> =10A, I <sub>B</sub> =250mA
*V <sub>FEC</sub>	-	-	1.6	V	I <sub>C</sub> =10A
*h <sub>FE</sub> 1	1000	-	3200	-	V <sub>CE</sub> =10V, I <sub>C</sub> =5A
*h <sub>FE</sub> 2	600	-	-	-	V <sub>CE</sub> =10V, I <sub>C</sub> =10A
*h <sub>FE</sub> 3	400	-	-	-	V <sub>CE</sub> =10V, I <sub>C</sub> =13A

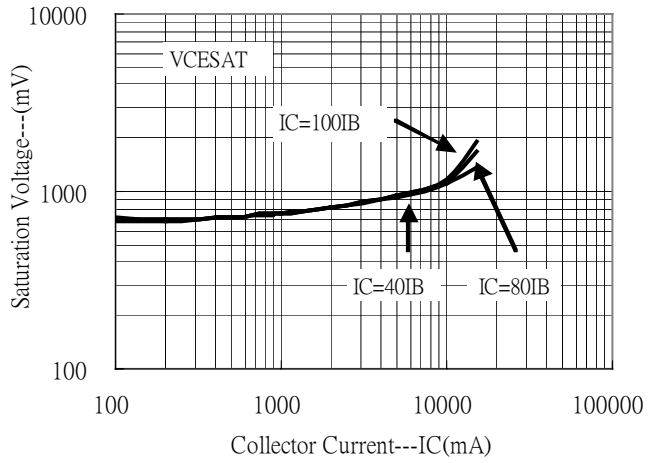
\*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

## Typical Characteristics

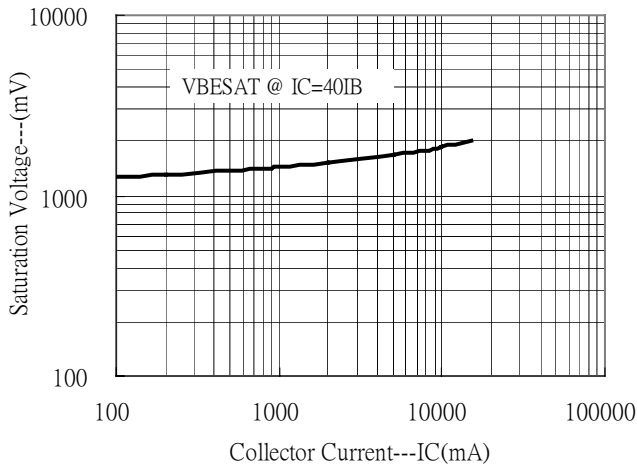
Current Gain vs Collector Current



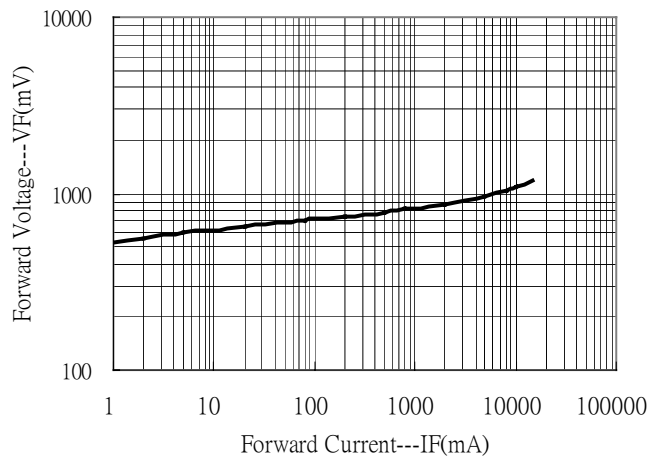
Saturation Voltage vs Collector Current



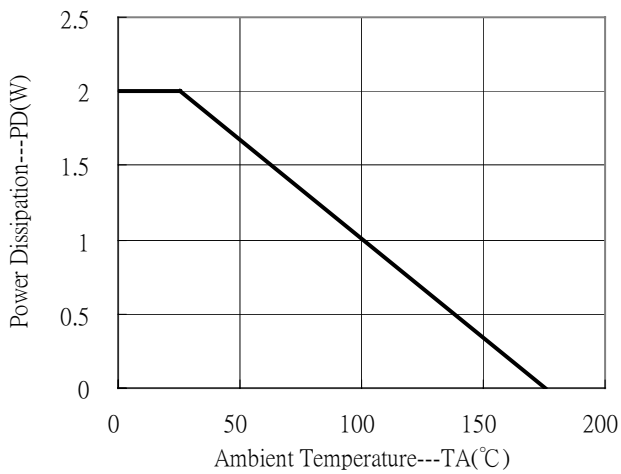
Saturation Voltage vs Collector Current



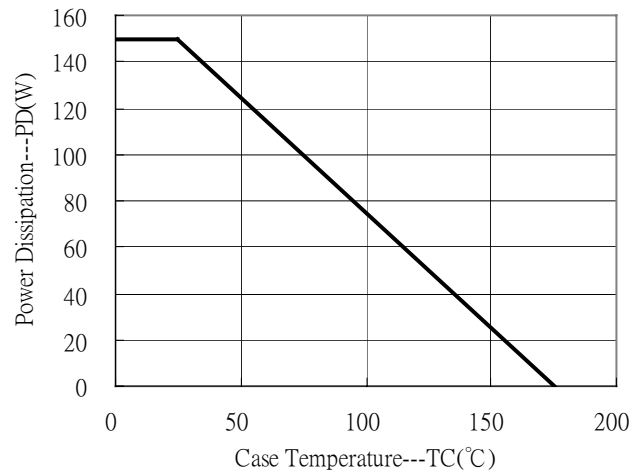
Built-in Diode Forward Characteristics



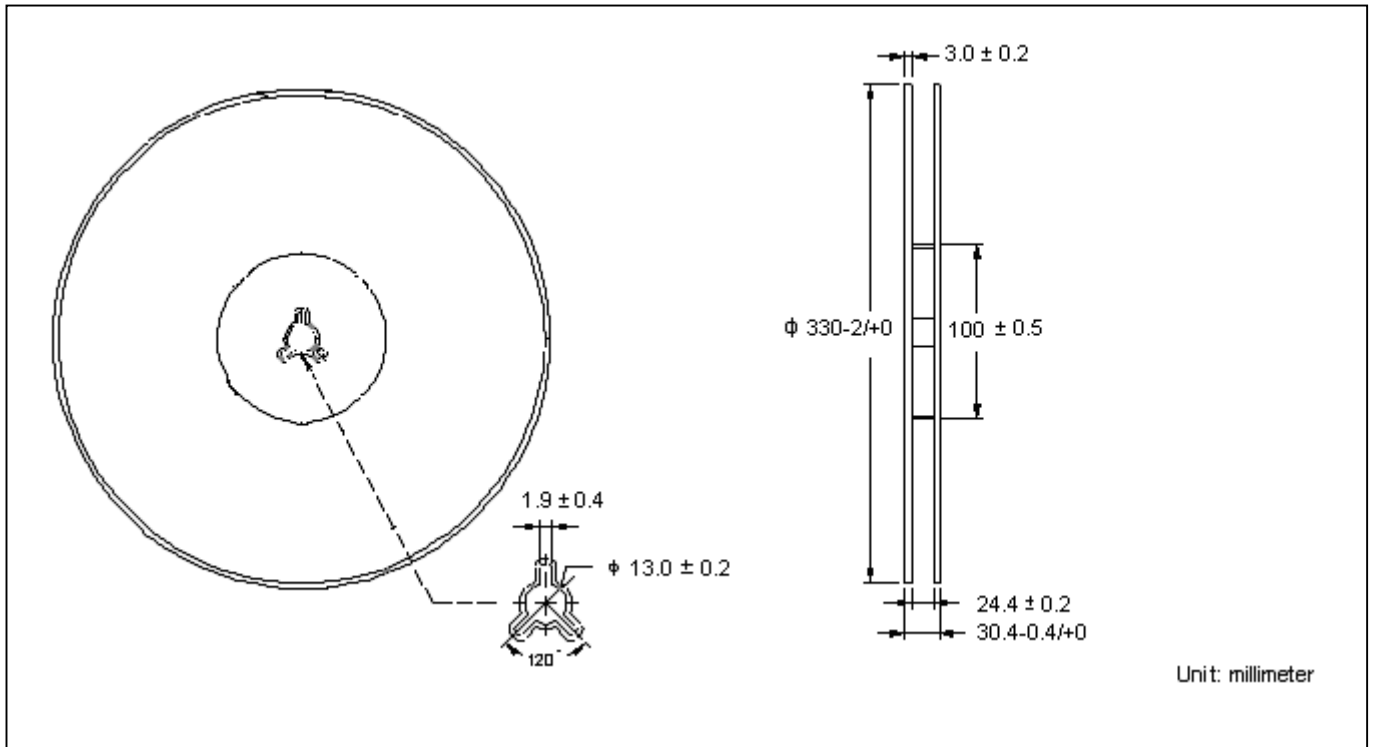
Power Derating Curve



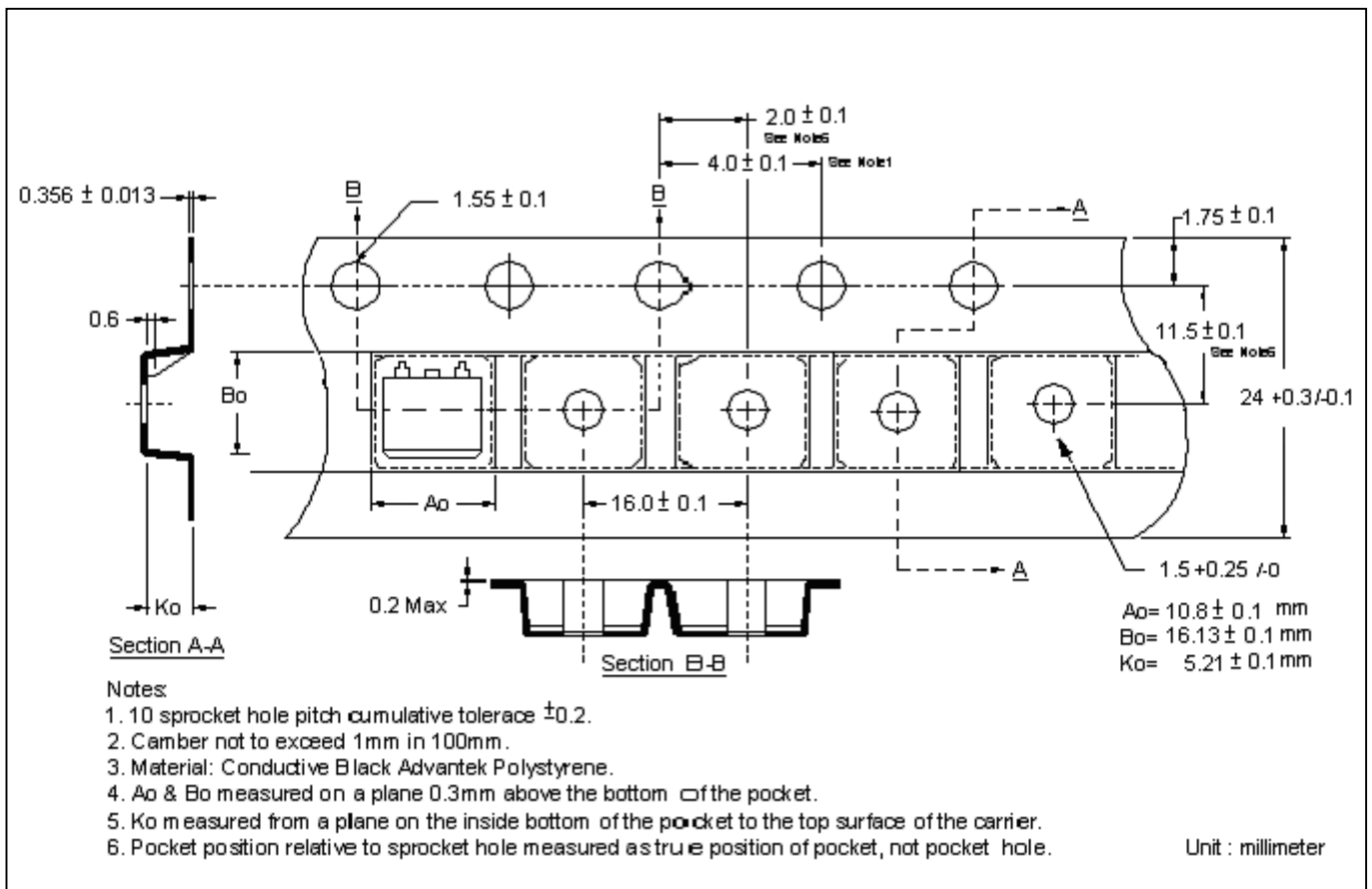
Power Derating Curve



**Reel Dimension**



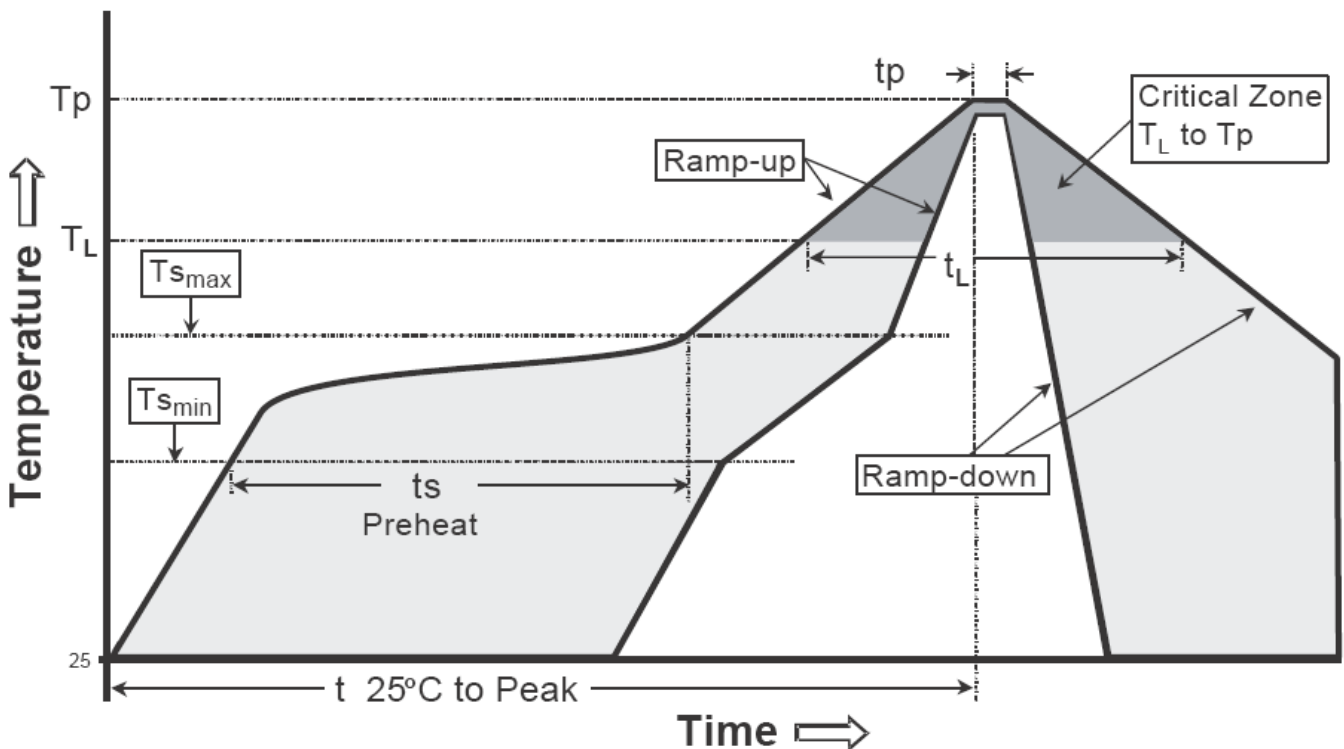
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

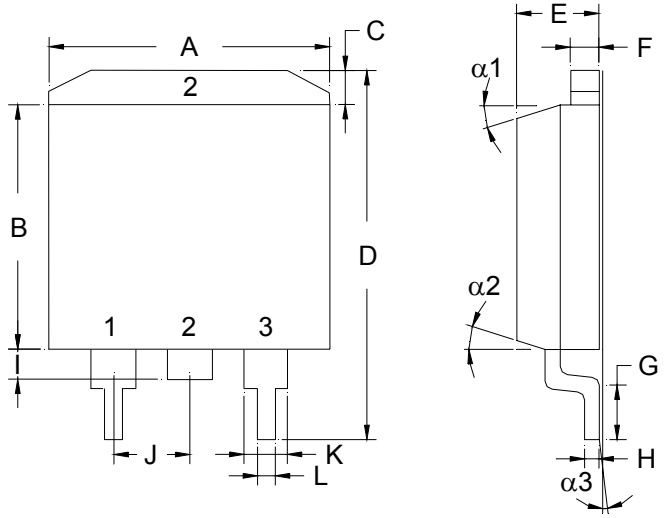
**Recommended temperature profile for IR reflow**



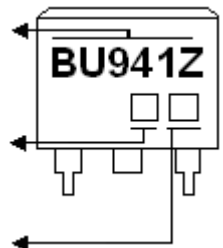
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-263 Dimension**



**Marking :**



Device Name ←

Year Code:  
 5→2015, 6→2016, ..., etc ←

Month Code:  
 1→Jan, 2→Feb, ..., 9→Sep, A→Oct, B→Nov, C→Dec ←

Style : Pin 1.Base 2.Collector 3.Emitter

3-Lead Plastic Surface Mounted Package  
 CYStek Package Code : F3

\*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.3800	0.4050	9.65	10.29	I	0.0500	0.0700	1.27	1.78
B	0.3300	0.3700	8.38	9.40	J	-	*0.1000	-	*2.54
C	-	0.0550	-	1.40	K	0.0450	0.0550	1.14	1.40
D	0.5750	0.6250	14.61	15.88	L	0.0200	0.0390	0.51	0.99
E	0.1600	0.1900	4.06	4.83	$\alpha 1$	-	-	6°	8°
F	0.0450	0.0550	1.14	1.40	$\alpha 2$	-	-	6°	8°
G	0.0900	0.1100	2.29	2.79	$\alpha 3$	-	-	0°	5°
H	0.0180	0.0290	0.46	0.74					

**Notes :** 1.Controlling dimension : millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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