STRUCTURE: Silicon Monolithic integrated circuit

PRODUCT NAME: Servo signal processor for compact disc player

TYPE NAME: **BU9543KV**

FEATURES: The BU9543KV is a servo signal processor complete with built-in pre-servo amplifier and sampling rate converter for application to compact disc player.

O Absolute maximum ratings (Ta=25°C)

Items	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	4.5	V
Internal power supply voltage	V_{CORE}	2.5	V
Power dissipation	P_d	0.85 *1	W
Operating temp. range	T_{opr}	-40 ~ +85	°C
Storage temp. range	T_{stg}	-55 ~ +125	°C

*1 Use of this processor at Ta = 25°C and over is subject to reduction of 8.5mW per 1°C.

* Operation is not guaranteed.

O Recommendation Operating range (Ta=-40 ~ +85°C)

Items	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	2.7 ~ 3.6	V
Internal power supply voltage	V_{CORE}	1.4 ~ 1.65	V

* This product is not designed for protection against radioactive rays.

O Electrical characteristics (Digital system)

V_{DD}=3.0V, V_{CORE}=1.5V (Unless otherwise specified Ta = 25°C)

Items		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Input voltage	H-level voltage	V_{IH}	2.1	-	-	V	
	L-level voltage	V_{IL}	-	-	0.9	V	
Hysteresis input voltage	H-level voltage	V_{IH}	2.3	-	-	V	
	L-level voltage	V_{IL}	-	-	1.1	V	
Input L current to Pull-up resistor		I_{IL}	-35	-75	-115	μA	V_{IN}=0V
Input H current to Pull-down resistor		I_{IH}	20	50	85	μA	V_{IN}=3V
Input current		I_I	-	-	±1	μA	V_{IN}=0~3V
Output voltage	H-level voltage	V_{OH}	2.5	-	-	V	I_O=-0.6mA
	L-level voltage	V_{OL}	-	-	0.5	V	I_O=0.6mA

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
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O Electrical Characteristics (Analog system 1/2)

V_{DD}=3.0V, V_{CORE}=1.5V (Unless otherwise specified Ta = 25°C, R_L=10kΩ, standard V_C)

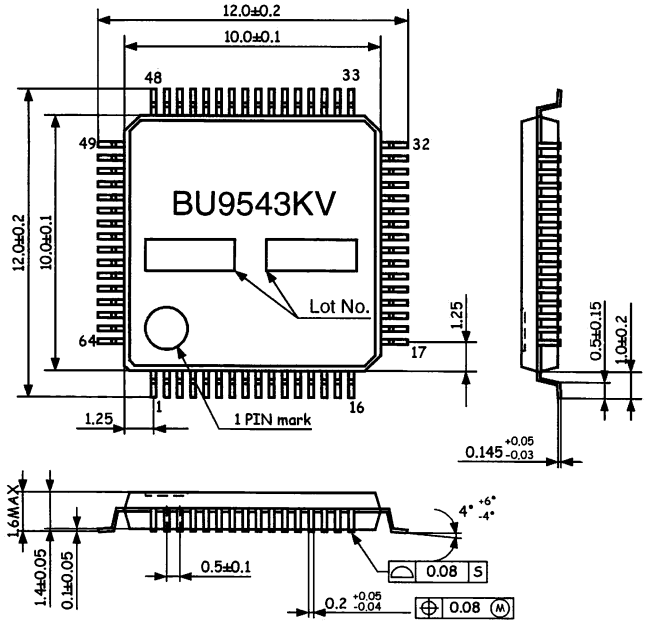
Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
Total						
Circuit current 1	I_{Q1}	-	10	27	mA	AVDD1,AVDD2,DVDD
Circuit current 2	I_{Q2}	-	5	10	mA	VDD_CORE
PLL (VCO)						
Max. oscillation Frequency	f_{VCOH}	4.6	6.5	-	MHz	1/4 of FLAG1 and VCO outputs
Min. oscillation Frequency	f_{VCOL}	-	1.1	1.7	MHz	1/4 of FLAG1 and VCO outputs
FC DAC						
Offset voltage	V_{FCOF}	-50	-	50	mV	FCO
Max. output voltage	V_{FCH}	0.2	0.5	-	V	FCO
Min. output voltage	V_{FCL}	-	-0.5	-0.2	V	FCO
PCO						
L-level output voltage	V_{PCH}	-	-1.0	-0.6	V	PCO
H-level output voltage	V_{PCL}	0.6	1.0	-	V	PCO
Audio DAC						
Distortion rate	THD	-	0.01	-	%	LDACO,RDACO,0dB 1kHz sine
Dynamic range	DR	-	90	-	dB	LDACO,RDACO,-60dB 1kHz sine
S/N ratio	S/N	-	96	-	dB	LDACO,RDACO
Max. output level	V_{SMAX}	0.75	0.85	0.95	V_{rms}	LDACO,RDACO,0dB 1kHz sine
EFM comparator						
Threshold level	V_{EFM}	-200	-	200	mV	RFI,ANA_MONI0,FLAG2
Servo ADC						
Offset voltage	V_{ADOF}	-140	-	140	mV	ANA_MONI0,ANA_MONI1
Max. conversion level	V_{ADH}	1.0	1.2	1.4	V	ANA_MONI0,ANA_MONI1
Min. conversion level	V_{ADL}	-1.4	-1.2	-1.0	V	ANA_MONI0,ANA_MONI1
Servo DAC						
Offset voltage	V_{DAOF}	-80	-	80	mV	FDOUT,TDOUT,SDOUT,CLVOUT
Max. output voltage	V_{DAH}	0.8	1.2	-	V	FDOUT,TDOUT,SDOUT,CLVOUT
Min. output voltage	V_{DAL}	-	-1.2	-0.8	V	FDOUT,TDOUT,SDOUT,CLVOUT
Bias amplifier						
Max. output current	I_{BO}	-	±1.5	-	mA	VBIAS and BIAS fluctuation to be 200mV MAX.

O Electrical Characteristics (Analog system 2/2)

V_{DD}=3.0V, V_{CORE}=1.5V (Unless otherwise specified Ta = 25°C, R_L=10kΩ, standard V_C)

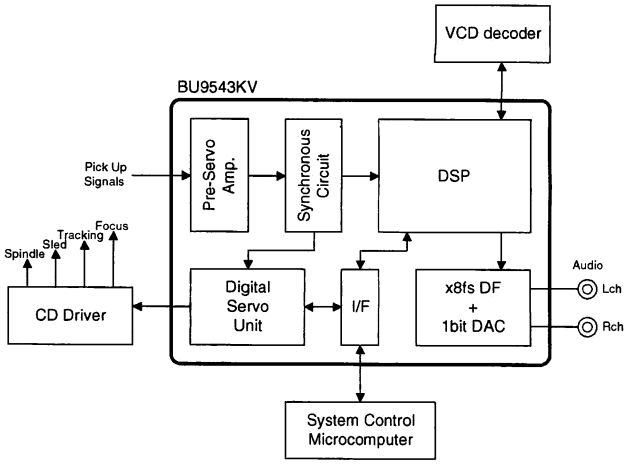
Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
RF amplifier						
Offset voltage	V_{RFOF}	-	0	-	mV	AC,BD,EQO
Max. output voltage	V_{RFH}	1.0	1.2	-	V	AC,BD,EQO
Min. output voltage	V_{RFL}	-	-1.3	-1.1	V	AC,BD,EQO
FE amplifier						
Offset voltage	V_{FEOF}	-	0	-	mV	AC,BD,ANA_MONI0,ANA_MONI1
Max. output voltage	V_{FEH}	1.0	1.4	-	V	AC,BD,ANA_MONI0,ANA_MONI1
Min. output voltage	V_{FEL}	-	-1.4	-1.0	V	AC,BD,ANA_MONI0,ANA_MONI1
TE amplifier						
Offset voltage	V_{TEOF}	-	70	-	mV	E,F,ANA_MONI0,ANA_MONI1
Max. output voltage	V_{TEH}	1.0	1.4	-	V	E,F,ANA_MONI0,ANA_MONI1
Min. output voltage	V_{TEL}	-	-1.4	-1.0	V	E,F,ANA_MONI0,ANA_MONI1
Asymmetric amplifier						
Offset voltage	V_{ASYOF}	-	0	-	mV	ASY=V_C,RFI,ANA_MONI0(ASY_TEST)
Max. output voltage	V_{ASYH}	1.1	1.4	-	V	ASY,RFI,ANA_MONI0(ASY_TEST)
Min. output voltage	V_{ASYL}	-	-1.4	-1.1	V	ASY,RFI,ANA_MONI0(ASY_TEST)
APC						
Output voltage1	V_{APC1}	2.4	2.8	-	V	PD="H",LD,ANA_MONI0(APCREF)
Output voltage2	V_{APC2}	-	0.1	0.5	V	PD="L",LD,ANA_MONI0(APCREF)
Max. reference voltage	V_{APCH}	-	220	-	mV	PD,LD,ANA_MONI0(APCREF)
Min. reference voltage	V_{APCL}	-	145	-	mV	PD,LD,ANA_MONI0(APCREF)

O Package Outline, Appearance marking diagram



VQFP64 (UNIT : mm)

O Block diagram



O Description of Terminal

No.	Name	Description of terminals
1	AVDD1	Analog power terminal
2	AC	A + C voltage input
3	BD	B + D voltage input
4	VBIAS	Bias level (VDD/2)
5	AGND1	Analog GND
6	E	E voltage input
7	F	F voltage input
8	PD	Photo detector input
9	LD	Laser drive output
10	ASY	For asymmetric correction
11	PCO	PCO output
12	FCO	FCO-DAC output
13	FDOUT	Focus drive output
14	TDOUT	Tracking drive output
15	SDOUT	Sled drive output
16	CLVOUT	CLV drive output
17	DVDD	Reference clock for SDRAM
18	MCK	Command transfer clock input
19	DIN/DOUT	Command data input/output
20	R/W	Command read/write signal
21	BUSY	Busy signal output
22	SUBSYQ	Sub code synchronous signal
23	SUBDATA	Sub code data signal output
24	SUBCK	Sub code bit clock input
25	WFCK	Disc frame synchronous signal
26	VDD_CORE	Internal digital power supply
27	DGND	Digital GND
28	CLK	Output for various clocks
29	CLK88	Clock output for driver IC
30	RESETB	"L" → reset condition
31	XBUFO	X'tal buffer output
32	DGND	Digital GND

No.	Name	Description of terminals
33	DVDD	I/O Digital power supply
34	DOUTA	Audio serial data output
35	LRCK	Audio LR signal output
36	DCK	Audio serial bit clock output
37	VDD_CORE	Internal digital power supply
38	DFDIN	Audio serial data input
39	DFLRCK	Audio LR signal input
40	DFDCK	Audio serial bit clock input
41	DFSCKI	Audio system clock input
42	DGND	Digital GND
43	FLAG0	Various flag output
44	FLAG1	Various flag output
45	FLAG2	Various flag output
46	FLAG3	Various flag output
47	DVDD	I/O Digital power supply
48	XI	X'tal connecting (input) terminal
49	XO	X'tal connecting terminal
50	DGND	Digital GND
51	TEST_IN	Test signal input
52	TEST_OUT	Test signal output
53	DVDD2	I/O Digital power supply
54	AGND2	Audio system analog GND
55	LDACO	Audio Lch output
56	VCDAC	Audio reference voltage
57	RDACO	Audio Rch output
58	AVDD2	Audio analog power supply
59	AD_MONI0	Monitor signal output
60	AD_MONI1	Monitor signal output
61	ANA_MONI0	Analog monitor signal output
62	ANA_MONI1	Analog monitor signal output
63	RFI	RF data re-input terminal
64	EQO	After-RF-equalizer output

O Cautions

(1) ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur and break mode (open or short) can not be specified if power supply, operating temperature, and those of ABSOLUTE MAXIMUM RATINGS are exceeded. If such a special condition is expected, components for safety such as fuse must be used.

(2) Power Supply

Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

(3) Functionality in the strong electro-magnetic field

Malfunction may occur if in the strong electro-magnetic field.

(4) Input terminals

All LSI contain parasitic components. Some are junctions which normally reverse bias. When these junctions forward bias, currents flows on unwanted path, malfunction or device damage may occur. To prevent this, all input terminal voltage must be between ground and power supply, or in the range of guaranteed value in the Electrical characteristics. And no voltage should be supplied to all input terminal when power is not supplied.

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