

Standard LCD Segment Driver



BU9799KV MAX 200 segments (SEG50xCOM4)

● **Features**

- Integrated RAM for display data (DDRAM): 50 x 4 bit (Max 200 Segment)
- LCD drive output : 4 Common output, 50 Segment output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator circuit
- No external components
- Low power consumption design
- Independent power supply for LCD driving
- Integrated Electrical volume register (EVR) function

● **Key Specifications**

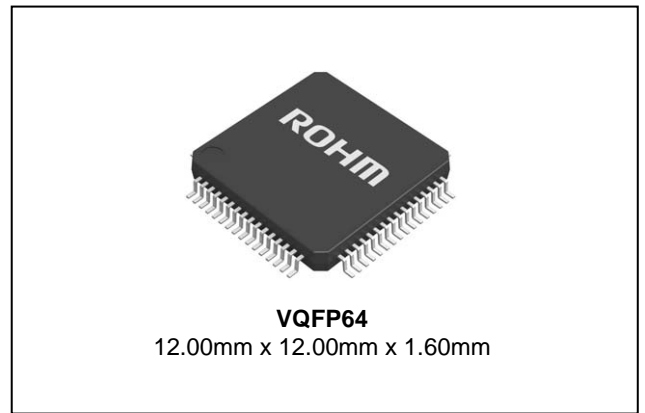
- Supply Voltage Range: +2.5V to +5.5V
- LCD drive power supply Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 200 Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 2wire serial interface

● **Applications**

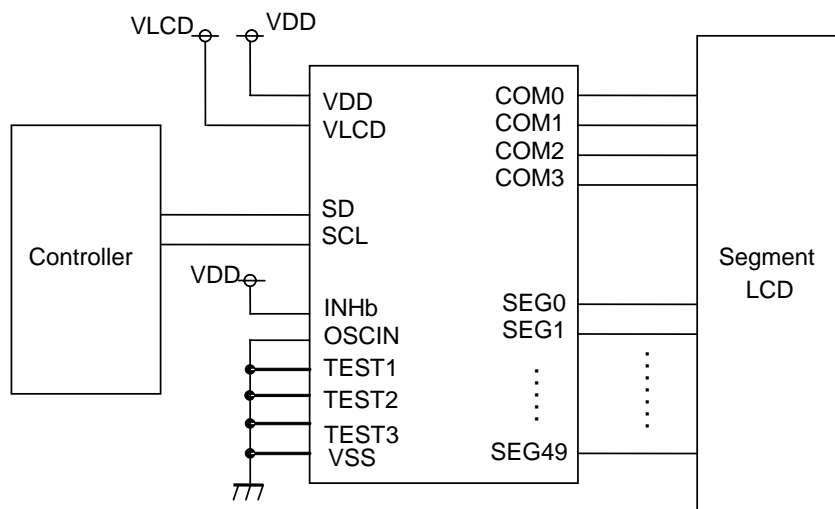
- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliances
- Meter equipment, etc.

● **Package**

W (Typ.) x D (Typ.) x H (Max.)



● **Typical Application Circuit**



Internal oscillator circuit mode

Figure 1. Typical application circuit

●Block Diagram / Pin Configuration / Pin Description

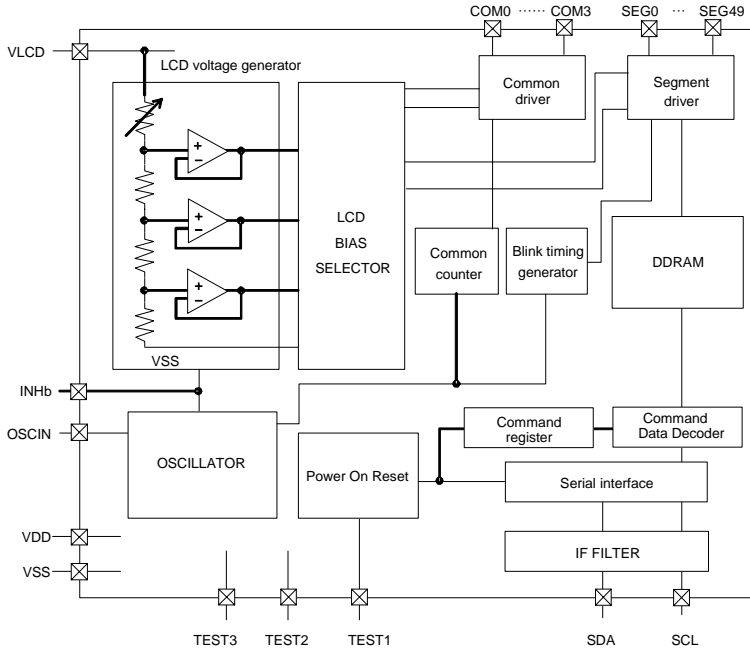


Figure 2. Block Diagram

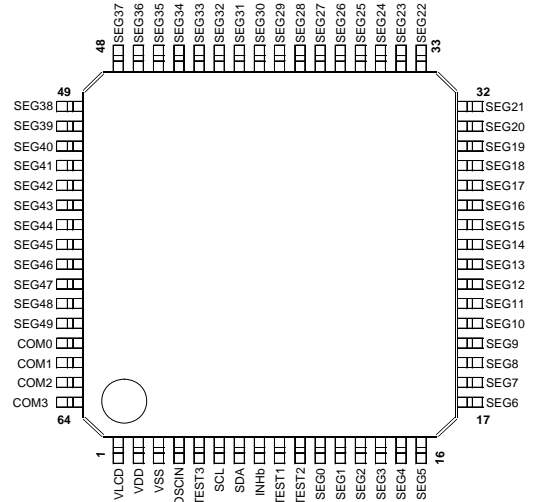


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

| Terminal | Terminal No. | I/O | Function |
|----------|--------------|-----|--|
| INHb | 8 | I | Input terminal for turning off display H: turn on display L: turn off display |
| TEST1 | 9 | I | Test input (ROHM use only) TEST1="L": POR circuit enable TEST1="H": POR circuit disable, refer to "Cautions in Power ON/OFF" |
| TEST2 | 10 | I | Test input (ROHM use only) Must be connected to VSS |
| TEST3 | 5 | I | Test input (ROHM use only) Must be connected to VSS |
| OSCIN | 4 | I | External clock input External clock and Internal clock modes can be selected by command. Must be connected to VSS when use internal oscillation circuit. |
| SDA | 7 | I | Serial data input |
| SCL | 6 | I | Serial data transfer clock |
| VSS | 3 | | GND |
| VDD | 2 | | Power supply |
| VLCD | 1 | | Power supply for LCD driving |
| SEG0-49 | 11-60 | O | SEGMENT output for LCD driving |
| COM0-3 | 61-64 | O | COMMON output for LCD driving |

● Absolute Maximum Ratings (VSS=0V)

| Parameter | Symbol | Ratings | Unit | Remarks |
|-------------------------------|--------|-----------------|------|---|
| Power Supply Voltage1 | VDD | -0.5 to +7.0 | V | Power supply |
| Power Supply Voltage2 | VLCD | -0.5 to +7.0 | V | LCD drive voltage |
| Power dissipation | Pd | 0.75 | W | When operated at more than 25°C, subtract 7.5mW/°C (Package only) |
| Input voltage range | VIN | -0.5 to VDD+0.5 | V | |
| Operational temperature range | Topr | -40 to +85 | °C | |
| Storage temperature range | Tstg | -55 to +125 | °C | |

● Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

| Parameter | Symbol | Ratings | | | Unit | Remarks |
|-----------------------|--------|---------|-----|-----|------|-------------------|
| | | MIN | TYP | MAX | | |
| Power Supply Voltage1 | VDD | 2.5 | - | 5.5 | V | Power supply |
| Power Supply Voltage2 | VLCD | 2.5 | - | 5.5 | V | LCD drive voltage |

● Electrical Characteristics

DC Characteristics (VDD=2.5V to 5.5V, VLCD=2.5V to 5.5V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|--------------------------|--------|--------|-----|--------|------|--|
| | | MIN | TYP | MAX | | |
| "H" level input voltage | VIH | 0.8VDD | - | VDD | V | SDA,SCL |
| "L" level input voltage | VIL | VSS | - | 0.2VDD | V | SDA,SCL |
| "H" level input current | IIH | - | - | 1 | μA | SDA,SCL |
| "L" level input current | IIL | -1 | - | - | μA | SDA,SCL |
| LCD Driver on resistance | SEG | RON | - | 3.5 | - | kΩ Iload=±10μA |
| | COM | RON | - | 3.5 | - | |
| Standby current | Ist | - | - | 5 | μA | Display off, Oscillation off |
| Power consumption 1 | IDD | - | 2.5 | 15 | μA | VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse |
| Power consumption 2 | ILCD | - | 10 | 20 | μA | VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse |

Oscillation Characteristics (VDD=2.5V to 5.5V, VLCD=2.5V to 5.5V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|-----------------|--------|--------|-----|-----|------|-----------------------------|
| | | MIN | TYP | MAX | | |
| Frame frequency | fCLK | 56 | 80 | 104 | Hz | FR = 80Hz setting, VDD=3.3V |

MPU interface Characteristics

(VDD=2.5V to 5.5V, VLCD=2.5V to 5.5V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|----------------------------|---------|--------|-----|-----|------|------------|
| | | MIN | TYP | MAX | | |
| Input rise time | tr | - | - | 0.3 | μs | |
| Input fall time | tf | - | - | 0.3 | μs | |
| SCL cycle time | tSCYC | 2.5 | - | - | μs | |
| "H" SCL pulse width | tSHW | 0.6 | - | - | μs | |
| "L" SCL pulse width | tSLW | 1.3 | - | - | μs | |
| SDA setup time | tSDS | 100 | - | - | μs | |
| SDA hold time | tSDH | 100 | - | - | us | |
| Buss free time | tBUF | 1.3 | - | - | μs | |
| START condition hold time | tHD;STA | 0.6 | - | - | μs | |
| START condition setup time | tSU;STA | 0.6 | - | - | μs | |
| STOP condition setup time | tSU;STO | 0.6 | - | - | μs | |

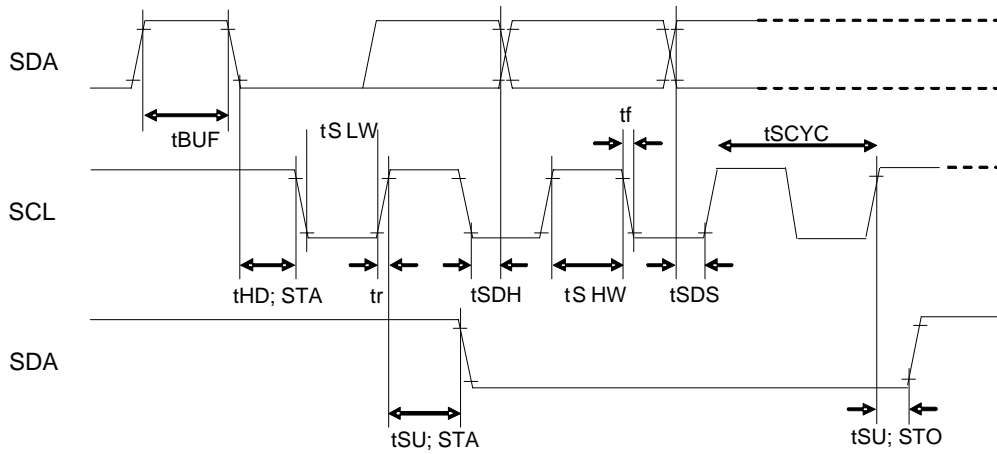


Figure 4. Interface Timing

● I/O equivalent circuit

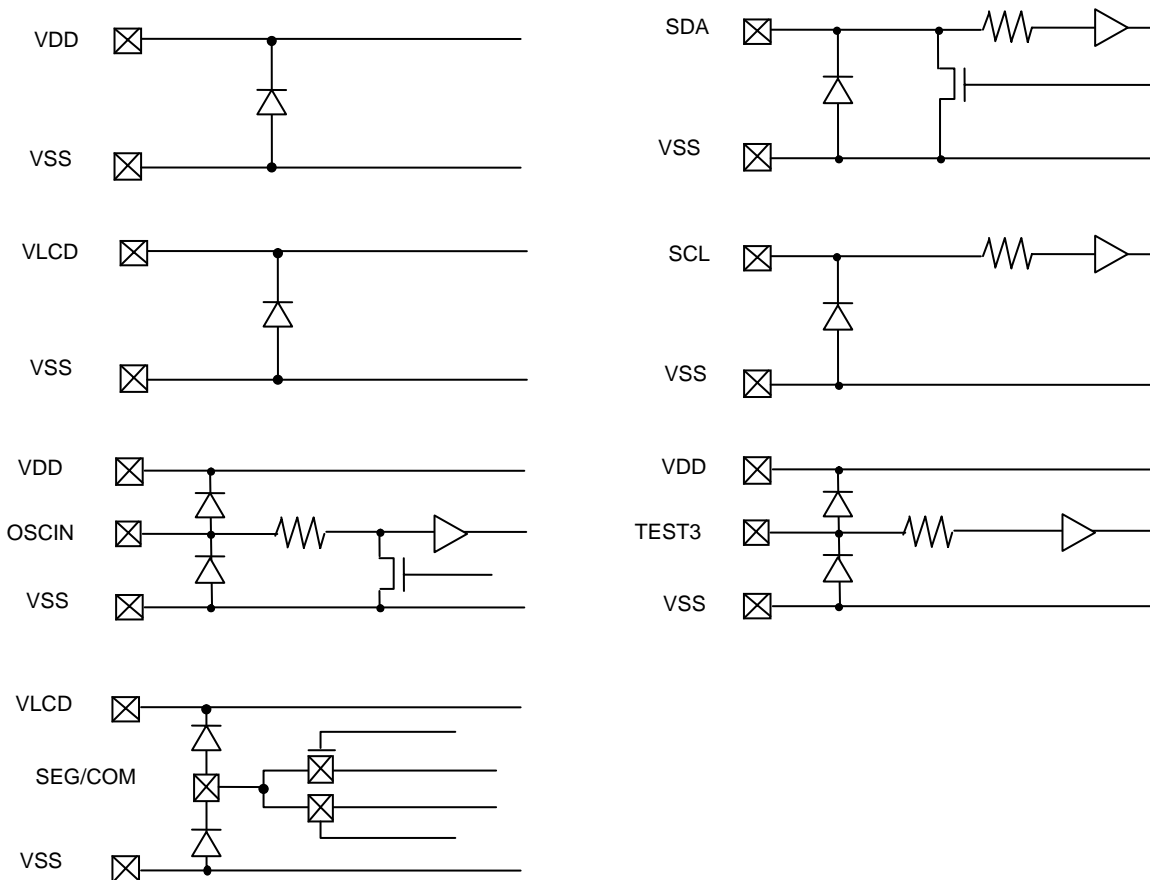
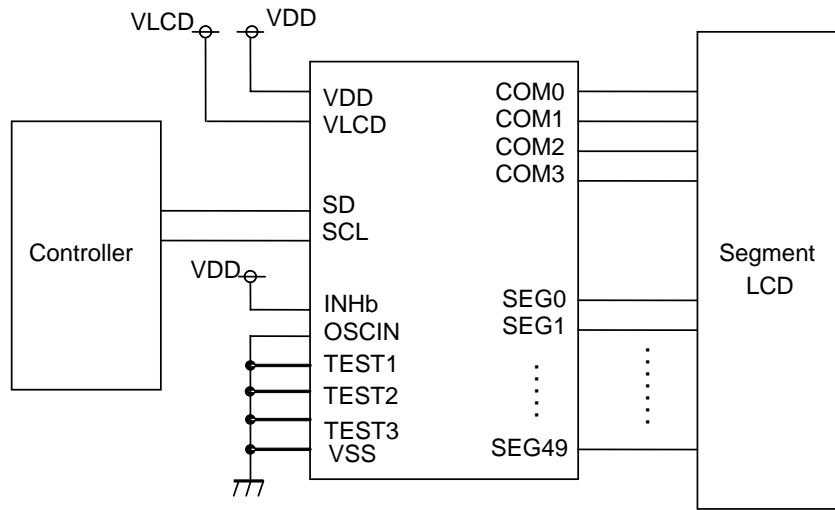
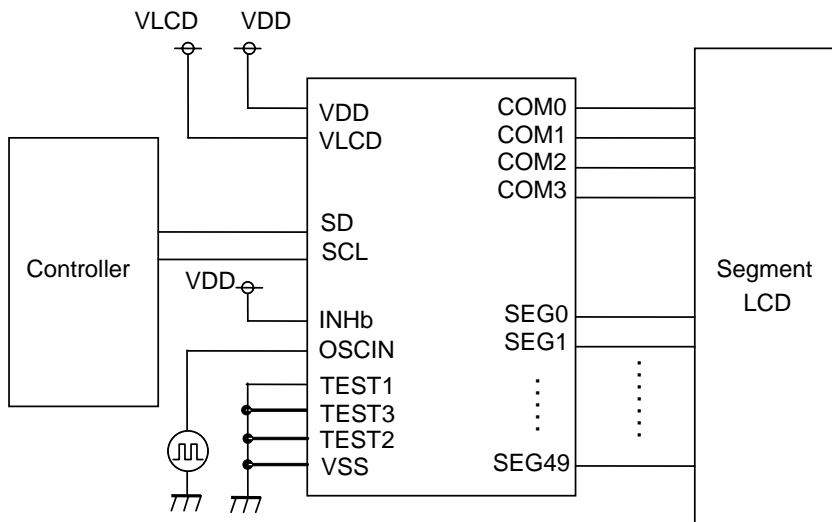


Figure 5. I/O equivalent circuit

● Example of recommended circuit



Internal oscillator circuit mode



External clock input mode

Figure 6. Example of recommended circuit

●Functional descriptions

○Command /Data transfer method

This device is controlled by 2-wire signal (SDA, SCL).

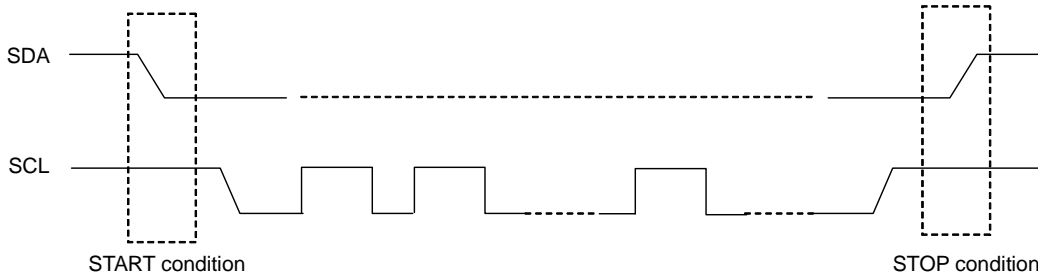


Figure 7. 2-SPI Command/Data transfer Format

It is necessary to generate START condition and STOP condition in 2wire serial interface transfer method.

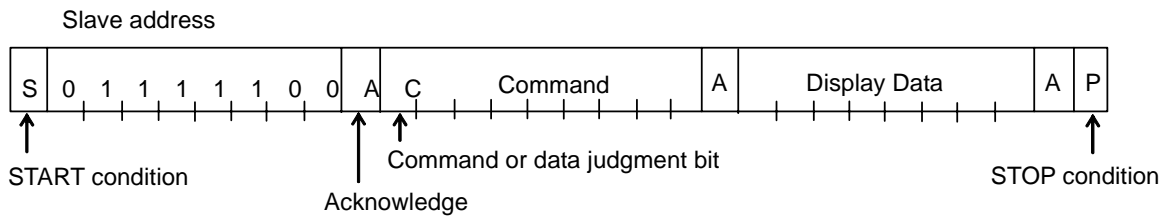


Figure 8. Interface protocol

Method of how to transfer command and data is shown as follows.

- 1) Generate "START condition".
- 2) Issue Slave address.
- 3) Transfer command and display data.

○Acknowledge

Data format is 8bits. After transfer of 8-bits data, Acknowledge bit is returned.

When SCL 8th = 'L' after transfer 8bit data (Slave Address, Command, Display Data), SDA outputs 'L'

When SCL 9th = 'L', SDA stops output function.

(Since SDA Output format is NMOS-Open-Drain, it can't output 'H' level.)

If there is no need Acknowledge function, please input 'L' level from SCL 8th='L' to SCL 9th='L'.

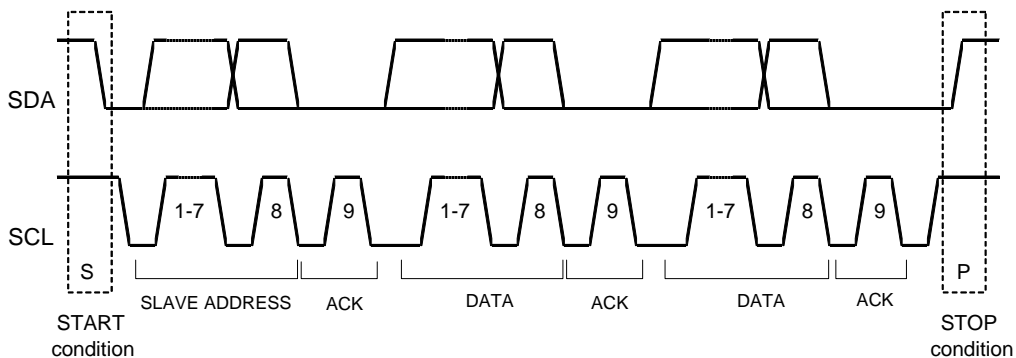
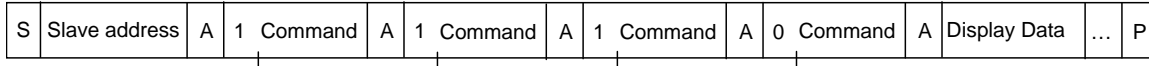


Figure 9. Acknowledge timing

○Command transfer method

Issue Slave Address (“01111100”) after generation of “START condition”.
 1byte after Slave Address becomes command input.
 MSB (“command or data judge bit”) of command decide if next data is command or display data.
 When set “command or data judge bit”=‘1’, next byte data is command.
 When set “command or data judge bit”=‘0’, next byte data is display data.

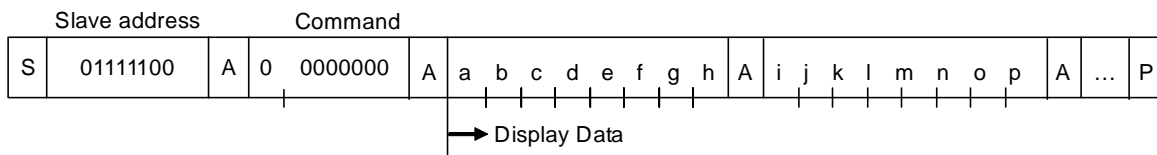


When display data is transferred, inputting of command is not allowed
 When one wants to input command again, please generate “START condition” once.
 If “START condition” or “STOP condition” are inputted in the middle of command transmission, command will be canceled.
 If Slave address is inputted after “START condition”, execution of command is allowed.
 Please input “Slave Address” in the first data transmission after “START condition”.
 When Slave Address cannot be recognized in the first data transmission, Acknowledge does not return and next transmission will be invalid. When data transmission is invalid status, if “START conditions” are transmitted again, it will return to valid status.

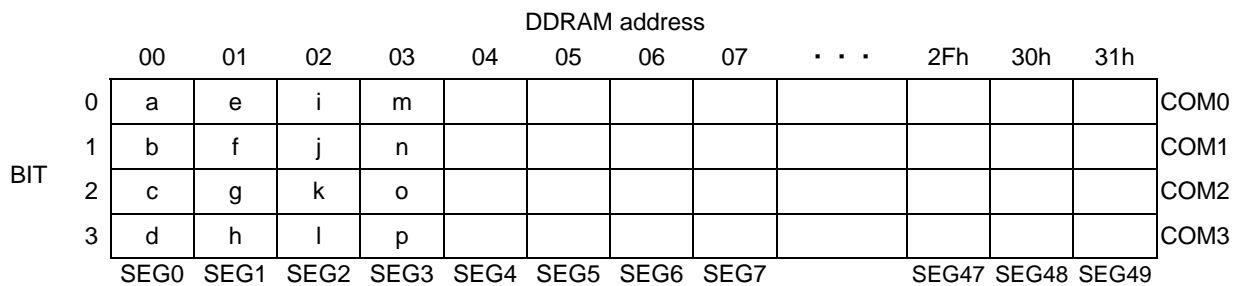
Take care to observe MPU Interface characteristic such as Input rise time and Setup/Hold time when transferring command and data (Refer to MPU Interface).

○Write display and transfer method

This device has Display Data RAM (DDRAM) of 50×4=200bits.
 The relationship between data input and display data, DDRAM data and address are as follows;



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.
 Data can be continuously written in DDRAM by transmitting Data continuously.
 (When RAM data is written successively after writing RAM data to 31h (SEG49), the address is returned to 00h (SEG0) by the auto-increment function.



Data transfer to DDRAM happens every 4bit data.
 So it will be finished to transfer with no need to wait ACK.

OOSCILLATOR

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock input. If internal oscillator circuit will be used, OSCIN must be connected to VSS.

*When using external clock mode, it has to input external clock from OSCIN terminal after ICSET command setting.

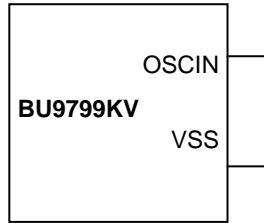


Figure 10. Internal oscillator circuit mode

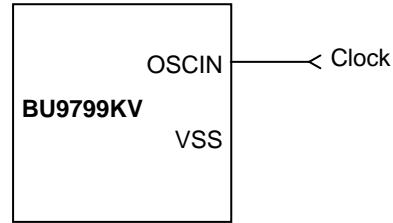


Figure 11. External clock input mode

○ LCD Driver Bias Circuit

This device generates LCD driving voltage with on-chip Buffer AMP.

And it can drive LCD at low power consumption.

*1/3 and 1/2Bias can set in MODESET command.

*Line and frame inversion can set in DISCTL command.

Refer to the "LCD driving waveform" about each LCD driving waveform.

○ Blink timing generator

This device has Blink function.

* This device will be at Blink mode with BLKCTL command.

Blink frequency varies widely by characteristic of fCLK, when internal oscillator circuit is used.

Refer to Oscillation Characteristics for more details on fCLK.

○ Reset initialize condition

Initial conditions after execution of Software Reset are as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Command Description about initialize value of register.

●Command / Function List

Description List of Command / Function

| No. | Command | Function |
|-----|---------------------------|------------------------|
| 1 | Mode Set (MODE SET) | Set LCD drive mode |
| 2 | Address set (ADSET) | Set LCD display mode 1 |
| 3 | Display control (DISCTL) | Set LCD display mode 2 |
| 4 | Set IC Operation (ICSET) | Set IC operation |
| 5 | Blink control (BLKCTL) | Set Blink mode |
| 6 | All Pixel control (APCTL) | Set pixel condition |
| 7 | EVR Set 1 (EVRSET1) | Set EVR 1 |
| 8 | EVR Set 2 (EVRSET2) | Set EVR 2 |

●Detailed command description

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

OMode Set (MODE SET)

| | | | | | | | | |
|-----|----|----|----|----|----|----|-----|--|
| MSB | | | | | | | LSB | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| C | 1 | 0 | 0 | P3 | P2 | * | * | |

(* : Don't care)

Set display ON and OFF

| | | |
|-------------|----|----------------------------|
| Setting | P3 | Reset initialize condition |
| Display OFF | 0 | ○ |
| Display ON | 1 | |

Display OFF : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1frame off data write. Display OFF mode will be finished by Display ON.

Display ON : SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

Set bias level

| | | |
|----------|----|----------------------------|
| setup | P2 | Reset initialize condition |
| 1/3 Bias | 0 | ○ |
| 1/2 Bias | 1 | |

Refer to LCD driving waveform

OAddress set (ADSET)

| | | | | | | | | |
|-----|----|----|----|----|----|----|-----|--|
| MSB | | | | | | | LSB | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| C | 0 | 0 | P4 | P3 | P2 | P1 | P0 | |

It is set address as follows;

| | | | | | |
|-------------------|-------------|-------------|-------|-------------|--|
| | MSB | | | LSB | |
| Internal register | Address [5] | Address [4] | · · · | Address [0] | |
| command | ICSET [P2] | ADSET [P4] | · · · | ADSET [P0] | |

The range of address can be set as 00000 to 10001(2).

Don't set out of range address, otherwise address will be set 00000.

ICSET command is only define MSB bit of address, not set the address of DDRAM.

If want to set the address of DDRAM, it has to be input ADSET command.

ODisplay control (DISCTL)

| | | | | | | | |
|-----|----|----|----|-----|----|----|----|
| MSB | | | | LSB | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 0 | 1 | P4 | P3 | P2 | P1 | P0 |

Set Power save mode FR

| Power save mode FR | P4 | P3 | Reset initialize condition |
|-------------------------|----|----|----------------------------|
| Normal mode (80Hz) | 0 | 0 | ○ |
| Power save mode1 (71Hz) | 0 | 1 | |
| Power save mode2 (64Hz) | 1 | 0 | |
| Power save mode3 (50Hz) | 1 | 1 | |

* Power consumption is reduced in the follow order:
Normal mode > Power save mode1 > Power save mode2 > Power save mode3

Set LCD drive waveform

| Setup | P2 | Reset initialize condition |
|-----------------|----|----------------------------|
| Line inversion | 0 | ○ |
| Frame inversion | 1 | |

* Power consumption is reduced in the follow order: Line inversion > Frame inversion
Refer to LCD drive waveform

Set Power save mode SR

| Setup | P1 | P0 | Reset initialize condition |
|------------------|----|----|----------------------------|
| Power save mode1 | 0 | 0 | |
| Power save mode2 | 0 | 1 | |
| Normal mode | 1 | 0 | ○ |
| High power mode | 1 | 1 | |

* Power consumption is increased in the follow order:
Power save mode 1 < Power save mode 2 < Normal mode < High power mode

(Reference current consumption data)

| Setup | Current consumption |
|-------------------|---------------------|
| Power save mode 1 | ×0.6 |
| Power save mode 2 | ×0.8 |
| Normal mode | ×1.0 |
| High power mode | ×1.2 |

*Above data is reference. It depends on Panel load.

(Note) The setting of Power save mode FR, LCD waveform, Power save mode will influence the following display image qualities.
Please select most suitable value from current consumption and display image quality with LCD panel.

| Mode | Flicker | Image quality, contrast |
|--------------------|---------|-------------------------|
| Power save mode FR | ○ | - |
| LCD waveform | ○ | ○ |
| Power save mode SR | - | ○ |

○Set IC Operation (ICSET)

| | | | | | | | |
|-----|----|----|----|----|----|----|-----|
| MSB | | | | | | | LSB |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 0 | 1 | P2 | P1 | P0 |

P2: Define the MSB bit of address of DDRAM. Refer to ADSET command.

Set software reset execution

| | |
|------------------------|----|
| Setup | P1 |
| No operation | 0 |
| Software Reset execute | 1 |

This command will be set initialize condition.

When executed Software reset, P1 and P0 will be ignored.

Set oscillator mode

| | | |
|----------------------|----|----------------------------|
| setup | P0 | Reset initialize condition |
| Internal oscillation | 0 | ○ |
| External clock input | 1 | |

Internal oscillation: Must be connected to VSS.

External clock input: Input external clock from OSCIN terminal

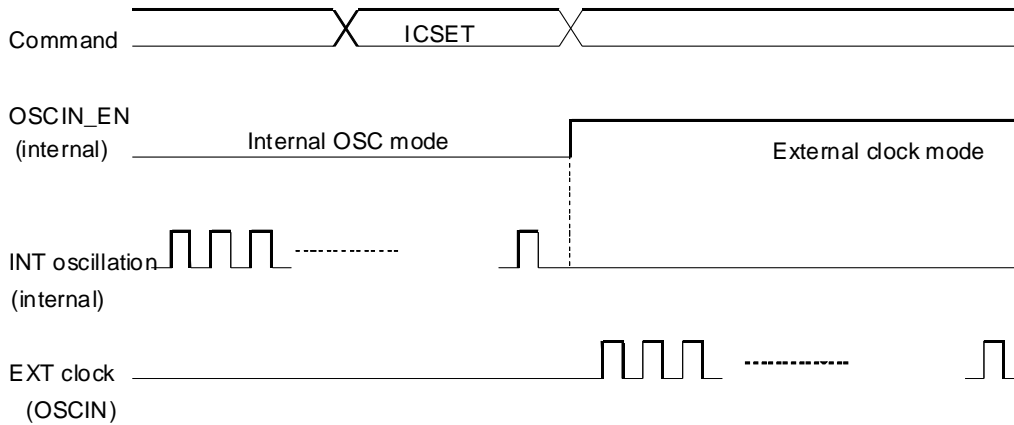


Figure 12. Oscillator mode change timing

○Blink control (BLKCTL)

| | | | | | | | |
|-----|----|----|----|----|----|----|-----|
| MSB | | | | | | | LSB |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 1 | 0 | * | P1 | P0 |

Set blink mode

| | | | |
|-----------------|----|----|----------------------------|
| Blink mode (Hz) | P1 | P0 | Reset initialize condition |
| OFF | 0 | 0 | ○ |
| 0.5 | 0 | 1 | |
| 1 | 1 | 0 | |
| 2 | 1 | 1 | |

○All Pixel control (APCTL)

| | | | | | | | |
|-----|----|----|----|----|----|----|-----|
| MSB | | | | | | | LSB |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 1 | 1 | 1 | P1 | P0 |

All display set ON, OFF

| | | |
|--------------|----|----------------------------|
| APON | P1 | Reset initialize condition |
| Normal | 0 | ○ |
| All pixel ON | 1 | |

| | | |
|---------------|----|----------------------------|
| APOFF | P0 | Reset initialize condition |
| Normal | 0 | ○ |
| All pixel OFF | 1 | |

All pixels ON : All pixels are ON regardless of DDRAM data
 All pixels OFF : All pixels are OFF regardless of DDRAM data

(Note) This command is valid in Display on status.
 The data of DDRAM don't change by this command. If set both P1 and P0 ="1", APOFF will be select.

○EVR Set 1(EVRSET1)

| | | | | | | | |
|-----|----|----|----|----|----|----|-----|
| MSB | | | | | | | LSB |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 0 | 0 | P2 | P1 | P0 |

It is able to control 32-step Electrical Volume Register (EVR).
 It is able to set V0 voltage level (the max level voltage of LCD driving voltage).
 It is set electrical volume register as follows;

| | | | | | |
|---------|---------|---------|---------|---------|----------------------------|
| MSB | | | LSB | | |
| EVR4 | EVR3 | EVR2 | EVR1 | EVR0 | |
| EVRSET1 | EVRSET1 | EVRSET1 | EVRSET2 | EVRSET2 | |
| P2 | P1 | P0 | P1 | P0 | |
| 0 | 0 | 0 | 0 | 0 | Reset initialize condition |

Electrical Volume Register (EVR) is set "00000" in reset initialize condition
 In "00000" condition, V0 voltage output VLCD voltage.
 Please refer to next page about V0 output voltage.
 It is prohibited the EVR setting that V0 voltage will be under 2.5V.

EVRSET1 is defined the upper 3bit of electrical volume register.
 It will be set the electrical volume register by this command (EVRSET1) input.

○EVR Set 2(EVRSET2)

| | | | | | | | |
|-----|----|----|----|----|----|----|-----|
| MSB | | | | | | | LSB |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| C | 1 | 1 | 1 | 1 | 0 | P1 | P0 |

EVRSET2 is defined the lower 2bit of electrical volume register.
 It will be set the electrical volume register by this command (EVRSET2) input.

○The relationship of Electrical Volume Register (EVR) setting and V0 voltage

| EVR | Calculation formula | VLCD= 5.500 | VLCD= 5.000 | VLCD= 4.000 | VLCD= 3.500 | VLCD= 3.000 | VLCD= 2.500 | [V] |
|-----|---------------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| 0 | VLCD | V0= 5.500 | V0= 5.000 | V0= 4.000 | V0= 3.500 | V0= 3.000 | V0= 2.500 | [V] |
| 1 | 0.967*VLCD | V0= 5.323 | V0= 4.839 | V0= 3.871 | V0= 3.387 | V0= 2.903 | V0= 2.419 | [V] |
| 2 | 0.937*VLCD | V0= 5.156 | V0= 4.688 | V0= 3.750 | V0= 3.281 | V0= 2.813 | V0= 2.344 | [V] |
| 3 | 0.909*VLCD | V0= 5.000 | V0= 4.545 | V0= 3.636 | V0= 3.182 | V0= 2.727 | V0= 2.273 | [V] |
| 4 | 0.882*VLCD | V0= 4.853 | V0= 4.412 | V0= 3.529 | V0= 3.088 | V0= 2.647 | V0= 2.206 | [V] |
| 5 | 0.857*VLCD | V0= 4.714 | V0= 4.286 | V0= 3.429 | V0= 3.000 | V0= 2.571 | V0= 2.143 | [V] |
| 6 | 0.833*VLCD | V0= 4.583 | V0= 4.167 | V0= 3.333 | V0= 2.917 | V0= 2.500 | V0= 2.083 | [V] |
| 7 | 0.810*VLCD | V0= 4.459 | V0= 4.054 | V0= 3.243 | V0= 2.838 | V0= 2.432 | V0= 2.027 | [V] |
| 8 | 0.789*VLCD | V0= 4.342 | V0= 3.947 | V0= 3.158 | V0= 2.763 | V0= 2.368 | V0= 1.974 | [V] |
| 9 | 0.769*VLCD | V0= 4.231 | V0= 3.846 | V0= 3.077 | V0= 2.692 | V0= 2.308 | V0= 1.923 | [V] |
| 10 | 0.750*VLCD | V0= 4.125 | V0= 3.750 | V0= 3.000 | V0= 2.625 | V0= 2.250 | V0= 1.875 | [V] |
| 11 | 0.731*VLCD | V0= 4.024 | V0= 3.659 | V0= 2.927 | V0= 2.561 | V0= 2.195 | V0= 1.829 | [V] |
| 12 | 0.714*VLCD | V0= 3.929 | V0= 3.571 | V0= 2.857 | V0= 2.500 | V0= 2.143 | V0= 1.786 | [V] |
| 13 | 0.697*VLCD | V0= 3.837 | V0= 3.488 | V0= 2.791 | V0= 2.442 | V0= 2.093 | V0= 1.744 | [V] |
| 14 | 0.681*VLCD | V0= 3.750 | V0= 3.409 | V0= 2.727 | V0= 2.386 | V0= 2.045 | V0= 1.705 | [V] |
| 15 | 0.666*VLCD | V0= 3.667 | V0= 3.333 | V0= 2.667 | V0= 2.333 | V0= 2.000 | V0= 1.667 | [V] |
| 16 | 0.652*VLCD | V0= 3.587 | V0= 3.261 | V0= 2.609 | V0= 2.283 | V0= 1.957 | V0= 1.630 | [V] |
| 17 | 0.638*VLCD | V0= 3.511 | V0= 3.191 | V0= 2.553 | V0= 2.234 | V0= 1.915 | V0= 1.596 | [V] |
| 18 | 0.625*VLCD | V0= 3.438 | V0= 3.125 | V0= 2.500 | V0= 2.188 | V0= 1.875 | V0= 1.563 | [V] |
| 19 | 0.612*VLCD | V0= 3.367 | V0= 3.061 | V0= 2.449 | V0= 2.143 | V0= 1.837 | V0= 1.531 | [V] |
| 20 | 0.600*VLCD | V0= 3.300 | V0= 3.000 | V0= 2.400 | V0= 2.100 | V0= 1.800 | V0= 1.500 | [V] |
| 21 | 0.588*VLCD | V0= 3.235 | V0= 2.941 | V0= 2.353 | V0= 2.059 | V0= 1.765 | V0= 1.471 | [V] |
| 22 | 0.576*VLCD | V0= 3.173 | V0= 2.885 | V0= 2.308 | V0= 2.019 | V0= 1.731 | V0= 1.442 | [V] |
| 23 | 0.566*VLCD | V0= 3.113 | V0= 2.830 | V0= 2.264 | V0= 1.981 | V0= 1.698 | V0= 1.415 | [V] |
| 24 | 0.555*VLCD | V0= 3.056 | V0= 2.778 | V0= 2.222 | V0= 1.944 | V0= 1.667 | V0= 1.389 | [V] |
| 25 | 0.545*VLCD | V0= 3.000 | V0= 2.727 | V0= 2.182 | V0= 1.909 | V0= 1.636 | V0= 1.364 | [V] |
| 26 | 0.535*VLCD | V0= 2.946 | V0= 2.679 | V0= 2.143 | V0= 1.875 | V0= 1.607 | V0= 1.339 | [V] |
| 27 | 0.526*VLCD | V0= 2.895 | V0= 2.632 | V0= 2.105 | V0= 1.842 | V0= 1.579 | V0= 1.316 | [V] |
| 28 | 0.517*VLCD | V0= 2.845 | V0= 2.586 | V0= 2.069 | V0= 1.810 | V0= 1.552 | V0= 1.293 | [V] |
| 29 | 0.508*VLCD | V0= 2.797 | V0= 2.542 | V0= 2.034 | V0= 1.780 | V0= 1.525 | V0= 1.271 | [V] |
| 30 | 0.500*VLCD | V0= 2.750 | V0= 2.500 | V0= 2.000 | V0= 1.750 | V0= 1.500 | V0= 1.250 | [V] |
| 31 | 0.491*VLCD | V0= 2.705 | V0= 2.459 | V0= 1.967 | V0= 1.721 | V0= 1.475 | V0= 1.230 | [V] |

 Prohibit setting

●LCD driving waveform

(1/3bias)

Line inversion

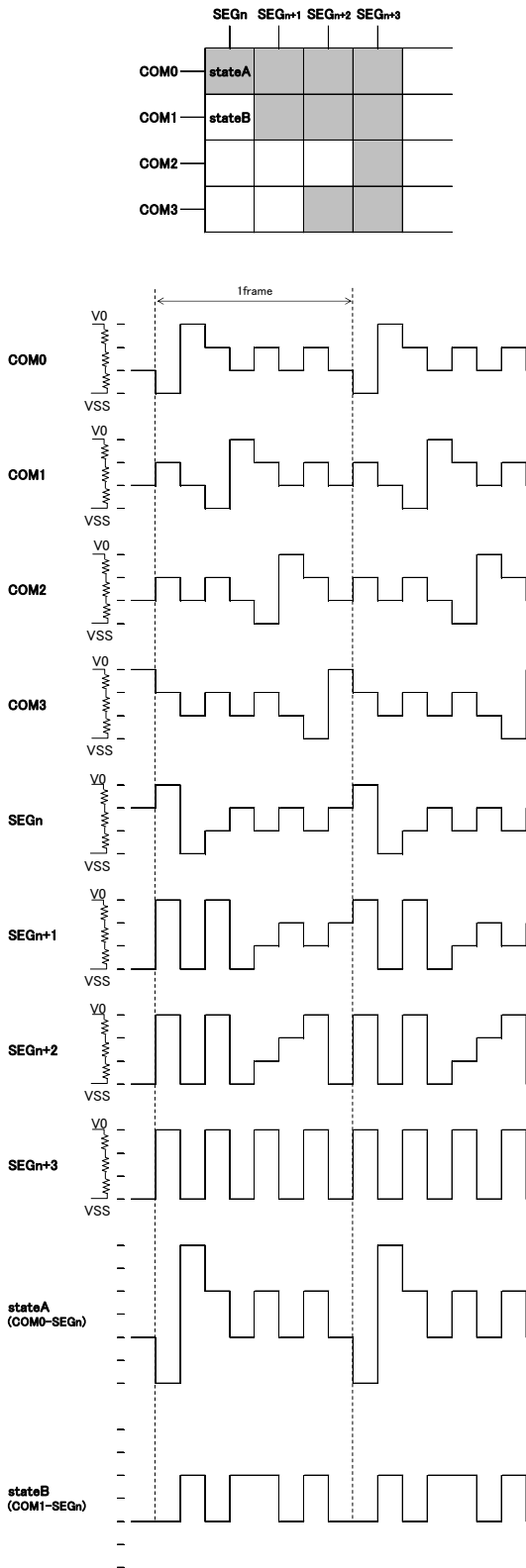


Figure 13. LCD waveform at line inversion (1/3bias)

Frame inversion

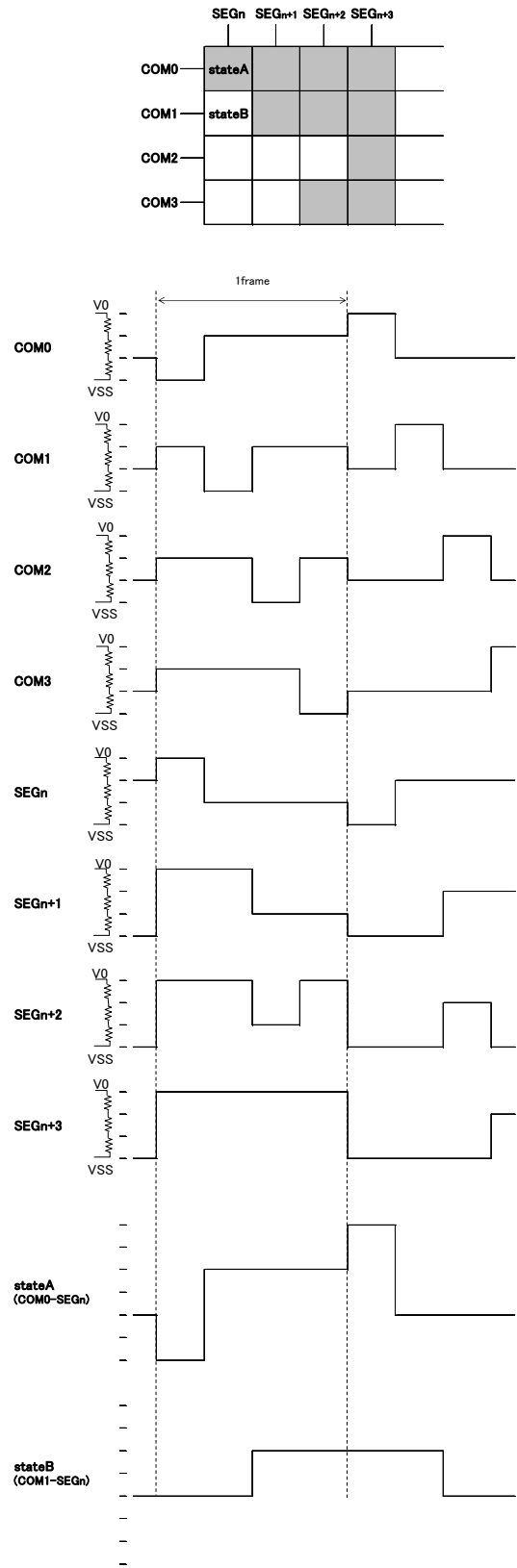


Figure 14. LCD waveform at frame inversion (1/3bias)

(1/2bias)

Line inversion

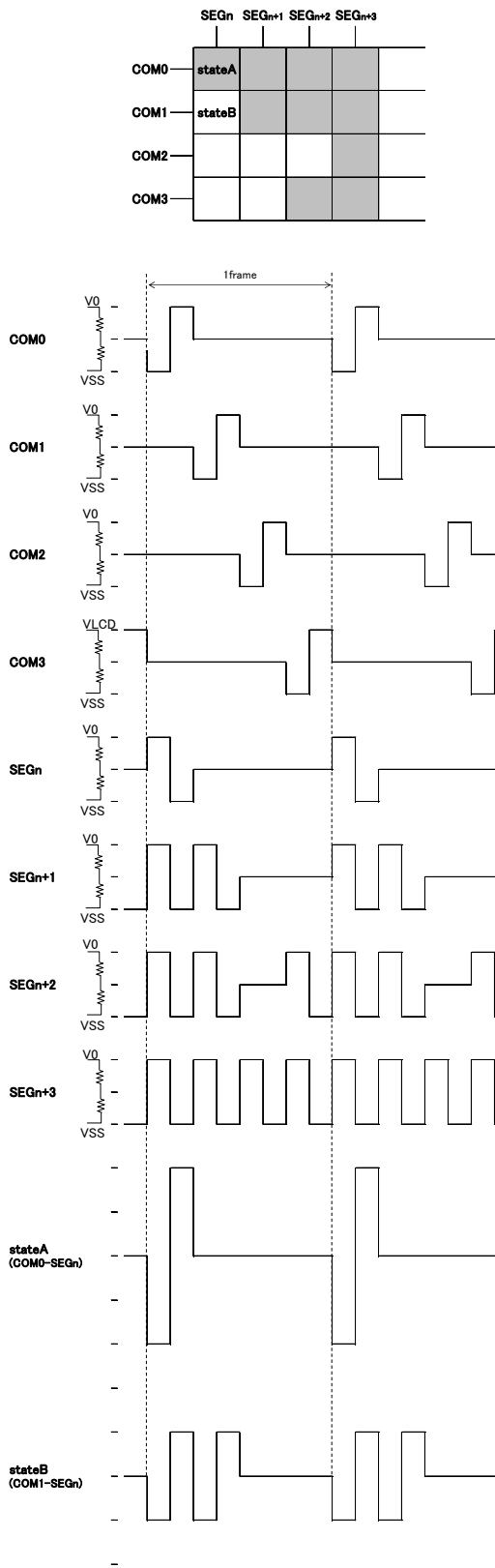


Figure 15. LCD waveform in line inversion (1/2bias)

Frame inversion

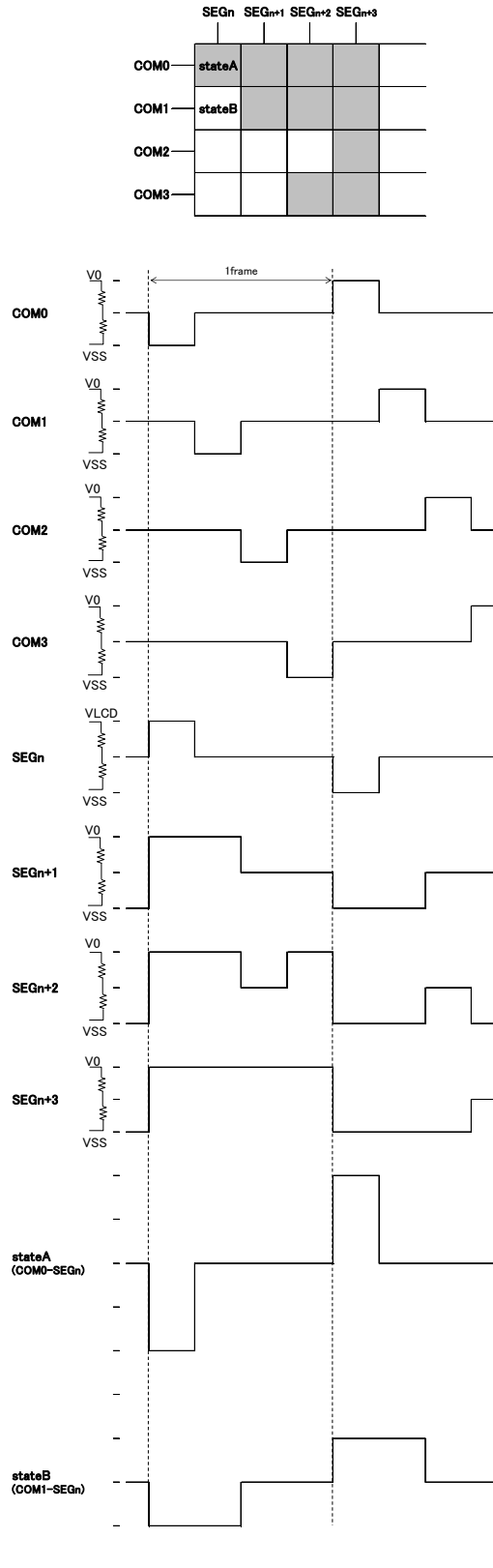


Figure 16. LCD waveform in frame inversion (1/2bias)

●Example of display data

If LCD layout pattern is like as Figure 17, Figure 18, and display pattern is like as Figure 19. Display data will be shown as follows;

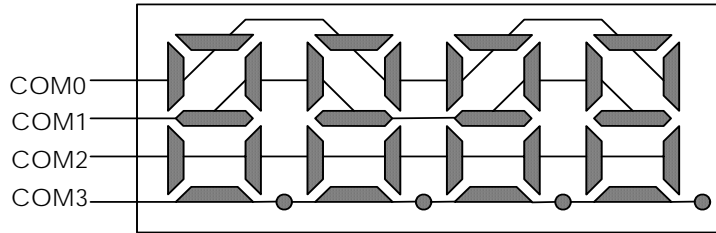


Figure 17. Example COM line pattern

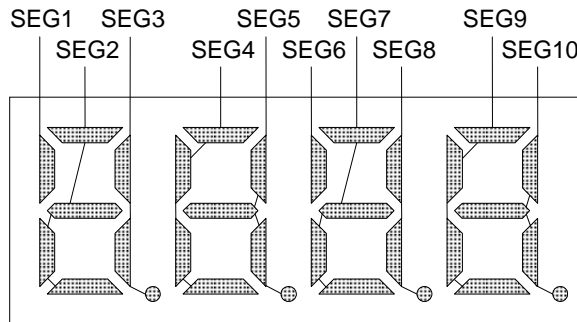


Figure 18. Example SEG line pattern

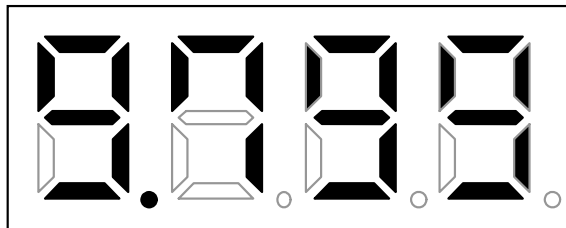


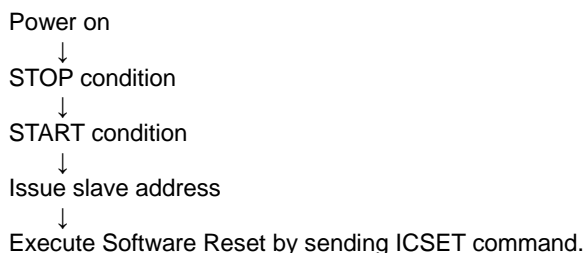
Figure 19. Example Display pattern

<DDRAM data mapping in Figure 19 display pattern>

| | | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | |
|---------|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | E | |
| | | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | G | |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| COM0 | D0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COM1 | D1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COM2 | D2 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COM3 | D3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Address | | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h |

●Initialize sequence

Please follow below sequence after Power-on to set this LSI to initial condition.



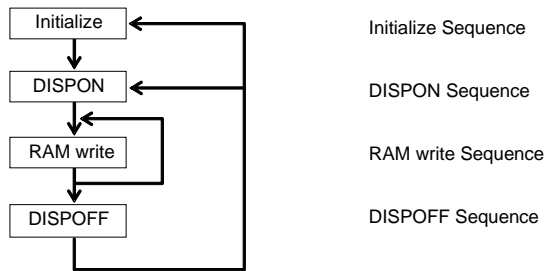
*Each register value and DDRAM address, DDRAM data are random condition after power on till initialize sequence is executed.

●Start sequence

○Start sequence example1

| No. | Input | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Descriptions |
|-----|---------------|----|----|----|----|----|----|----|----|---------------------|
| 1 | Power on | | | | | | | | | VDD=0→5V (Tr=0.1ms) |
| | ↓ | | | | | | | | | |
| 2 | wait 100μs | | | | | | | | | Initialize IC |
| | ↓ | | | | | | | | | |
| 3 | Stop | | | | | | | | | Stop condition |
| | ↓ | | | | | | | | | |
| 4 | Start | | | | | | | | | Start condition |
| | ↓ | | | | | | | | | |
| 5 | Slave address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Issue slave address |
| | ↓ | | | | | | | | | |
| 6 | ICSET | 1 | 1 | 1 | 0 | 1 | * | 1 | 0 | Software Reset |
| | ↓ | | | | | | | | | |
| 7 | BLKCTL | 1 | 1 | 1 | 1 | 0 | * | 0 | 1 | |
| | ↓ | | | | | | | | | |
| 8 | DISCTL | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| | ↓ | | | | | | | | | |
| 9 | EVRSET1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | |
| 10 | EVRSET2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| | ↓ | | | | | | | | | |
| 11 | ICSET | 1 | 1 | 1 | 0 | 1 | * | 0 | 1 | |
| | ↓ | | | | | | | | | |
| 12 | ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAM address set |
| | ↓ | | | | | | | | | |
| 13 | Display Data | * | * | * | * | * | * | * | * | address 00h - 01h |
| | Display Data | * | * | * | * | * | * | * | * | address 02h - 03h |
| | ⋮ | | | | | | | | | ⋮ |
| | Display Data | * | * | * | * | * | * | * | * | address 12h - 13h |
| | ↓ | | | | | | | | | |
| 14 | Stop | | | | | | | | | Stop condition |
| | ↓ | | | | | | | | | |
| 15 | Start | | | | | | | | | Start condition |
| | ↓ | | | | | | | | | |
| 16 | Slave address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Issue slave address |
| | ↓ | | | | | | | | | |
| 17 | MODESET | 1 | 1 | 0 | 0 | 1 | 0 | * | * | Display ON |
| | ↓ | | | | | | | | | |
| 18 | Stop | | | | | | | | | Stop condition |

○Start sequence example2



This LSI is initialized with Initialize Sequence. And start to display with DISPON Sequence.
 This LSI will update display data with RAM write Sequence.
 And stop the display with DISPOFF sequence.
 If you want to restart to display, This LSI will restart to display with DISPON Sequence.

Initialize sequence

| Input | DATA | | | | | | | | Description |
|---|------|----|----|----|----|----|----|----|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Power on wait 100us STOP START | | | | | | | | | |
| Slave address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Execute Software Reset Display OFF RAM address set Display data |
| ICSET | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | |
| MODESET | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Display data ... | * | * | * | * | * | * | * | * | |
| STOP | | | | | | | | | |

DISPON sequence

| Input | DATA | | | | | | | | Description |
|---------------|------|----|----|----|----|----|----|----|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| START | | | | | | | | | |
| Slave address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Execute internal OSC mode Set Display Control Set BLKCTL Set APCTL Set EVR1 Set EVR2 Display ON |
| ICSET | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| DISCTL | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| BLKCTL | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| APCTL | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| EVRSET1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| EVRSET2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |
| MODESET | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | |
| STOP | | | | | | | | | |

RAM write sequence

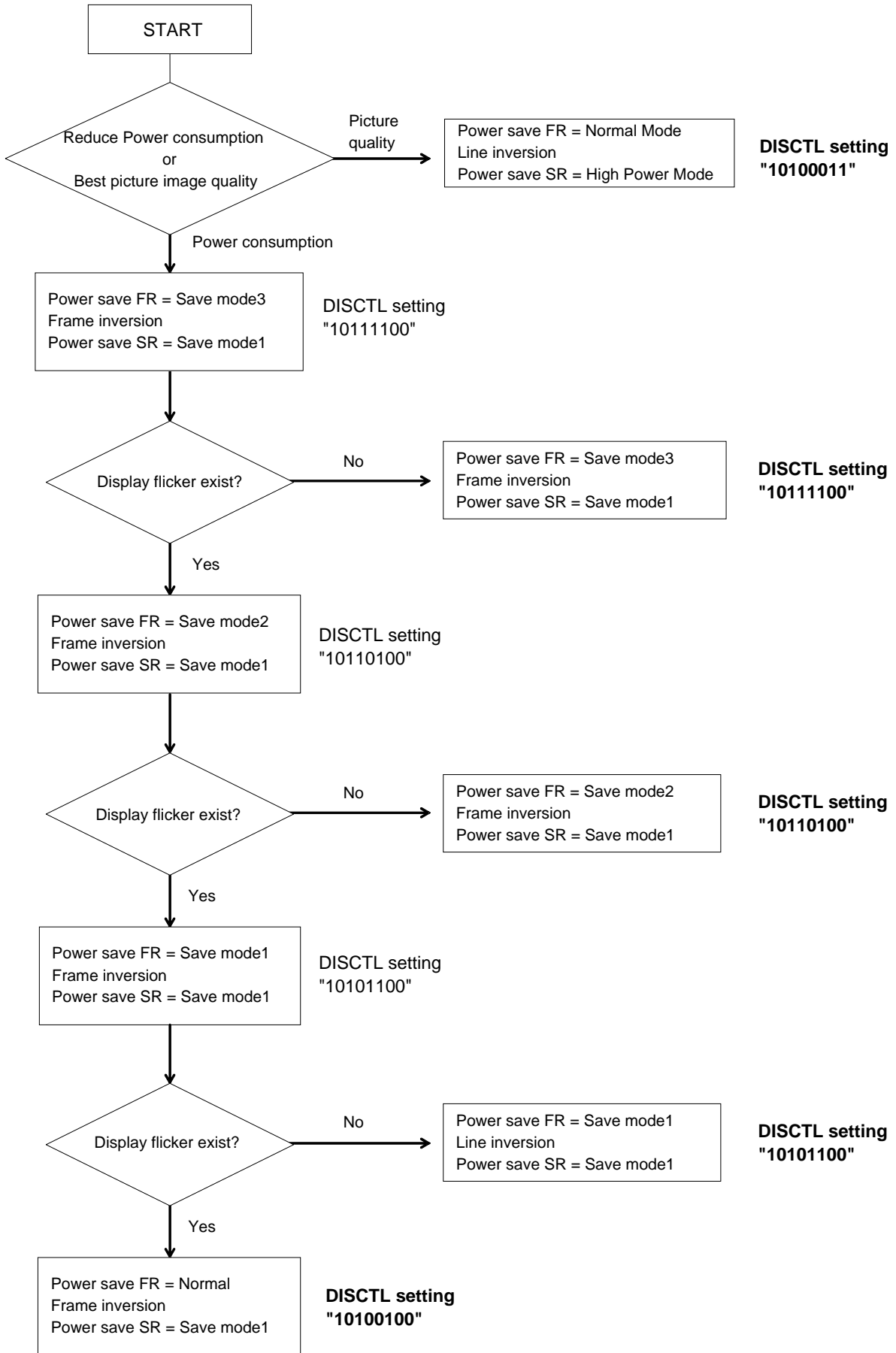
| Input | DATA | | | | | | | | Description |
|---------------------|------|----|----|----|----|----|----|----|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| START | | | | | | | | | |
| Slave address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Execute internal OSC mode Set Display Control Set BLKCTL Set APCTL Set EVR1 Set EVR2 Display ON RAM address set Display data |
| ICSET | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| DISCTL | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| BLKCTL | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| APCTL | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| EVRSET1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| EVRSET2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |
| MODESET | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | |
| ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Display Data ... | * | * | * | * | * | * | * | * | |
| STOP | | | | | | | | | |

DISPOFF sequence

| Input | DATA | | | | | | | | Description |
|---------------|------|----|----|----|----|----|----|----|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| START | | | | | | | | | |
| Slave address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Execute internal OSC mode Display OFF |
| ICSET | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| MODESET | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| STOP | | | | | | | | | |

According to the effect of noise or other external factor, BU9799KV occur abnormal operation.
 To avoid this phenomenon, please input command according to upper sequence certainly,
 when initializing IC, displaying ON/OFF, and refreshing RAM data.

●DISCTL setup flow chart



●Cautions in Power ON/OFF

○Power supply sequence
Please keep Power ON/OFF sequence as below waveform.

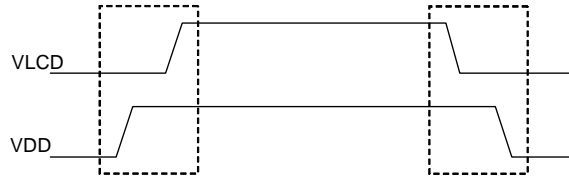


Figure 20. Power supply sequence

○Caution in P.O.R circuit use
This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended t_R , t_F , t_{OFF} , and V_{bot} spec below in order to ensure P.O.R operation

*It has to set TEST1="L" to be valid in POR circuit.

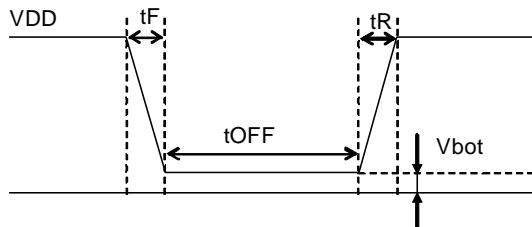


Figure 21. Power ON/OFF waveform

Recommended condition of t_R , t_F , t_{OFF} , V_{bot} ($T_a=25^\circ\text{C}$)

| t_R | t_F | t_{OFF} | V_{bot} |
|---------------|---------------|----------------|----------------|
| Less than 5ms | Less than 5ms | More than 20ms | Less than 0.3V |

If it is difficult to meet above conditions, execute the following sequence after Power-On.

*It has to keep the following sequence in the case of TEST1="H". As POR circuit is invalid status.

(1) TEST1 ="H"

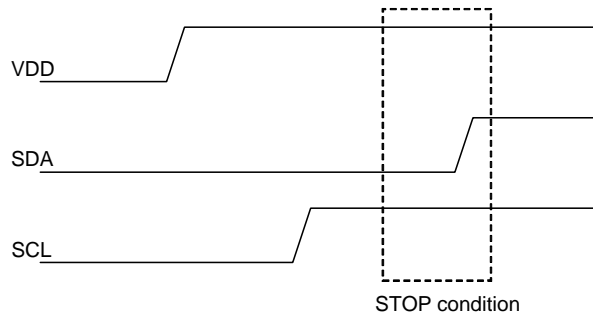


Figure 22. Stop condition

- (2) Generate STOP condition
- (3) Generate START condition
- (4) Issue slave address
- (5) Execute ICSET command (Software reset).
Refer to the item of the ICSET command for the details.

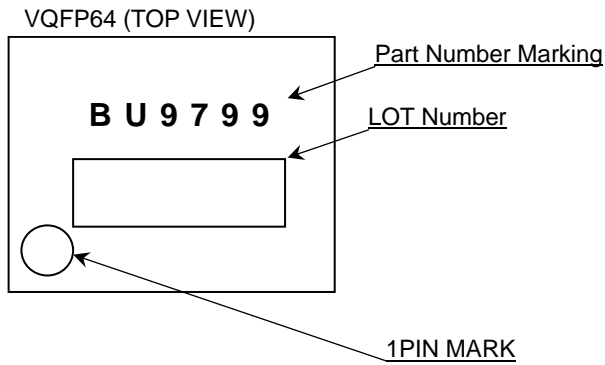
●Operational Notes

- (1) Absolute Maximum Ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.
- (2) Recommended Operating conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
- (3) Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
- (4) Power Supply Lines
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- (5) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
- (6) Short between Pins and Mounting Errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
- (7) Operation under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- (8) Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
- (9) Regarding Input Pins of the IC
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the GND voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC..
- (10) GND Wiring Pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.
- (11) External Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.
- (12) Unused Input Terminals
Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or ground line.
- (13) Rush current
When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parasitic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

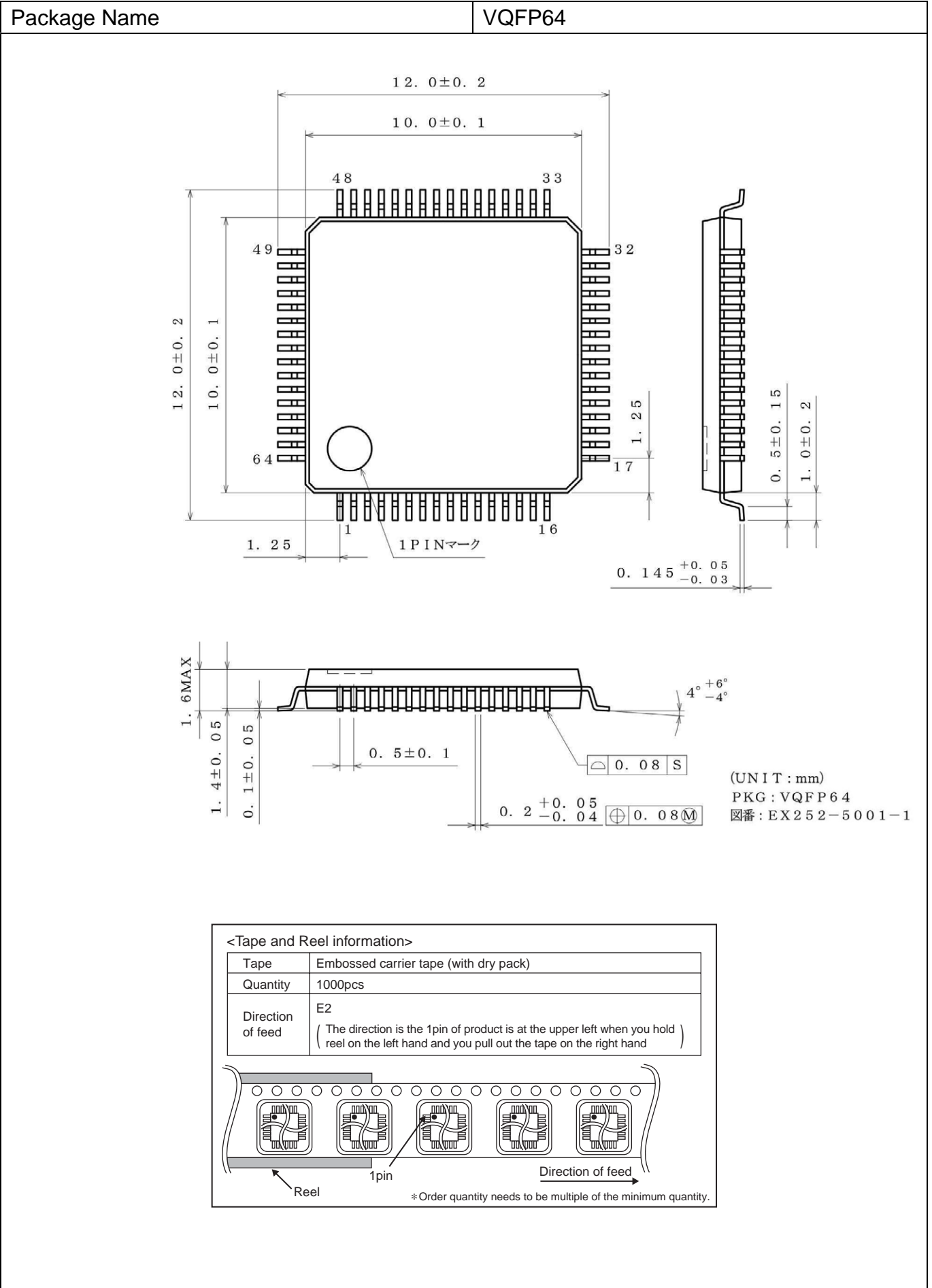
●Ordering Information

| | | | |
|-----------------|------------------------|---|-----|
| B U 9 7 9 9 K V | | - | E 2 |
| Part Number | Package KV : VQFP64 | Packaging and forming specification E2: Embossed tape and reel (VQFP64) | |

●Marking Diagram



●Physical Dimension, Tape and Reel Information



●Revision History

| Date | Revision | Changes |
|-------------|----------|--|
| 14.Mar.2012 | 001 | New Release |
| 8.Jan.2013 | 002 | Improved the statement in all pages. Deleted "Status of this document" in page 23. Changed format of Physical Dimension, Tape and Reel Information |

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| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

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Other Precaution

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General Precaution

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