

Structure	Silicon monolithic integrated circuit
Product	Digital video encoder
Type	BU9969KN
Features	Video format : NTSC-M, PAL-B/D/G/H/I Input pixel data format : YcbCr 4:2:2 656mode /601mode,RGB 16 bits(R:5bits/G:6bits/B:5bits) 656 input mode YCbCr 8 bits (corresponding to EAV,SAV input) 601 input mode YcbCr or RGB 16 bits (corresponding to Hsync,Vsync input) 10-bit Video DAC built-in, PLL built-in

○ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Digital core supply voltage	DVDD	-0.2 ~ 2.5	V
PLL supply voltage	PVDD		
Digital I/O supply voltage	IOVDD	-0.2 ~ 4.5	V
DAC supply voltage	AVDD		
Power dissipation 1	Pd1	450	^{*1} mW
Power dissipation 2	Pd2	700	^{*2} mW
Storage temperature range	Tstg	-25 ~ +125	°C

^{*1} IC simple substance. In the case of exceeding Ta=25°C, 4.5mW should be reduced per 1°C.

^{*2} A measured value at mounting on 50×50×1.6mm glass epoxy substrate.
 In the case of exceeding Ta=25°C, 7.0mW should be reduced per 1°C.

* The radiation-resistance design is not carried out.

* Operation is not guaranteed.

○ Operating Conditions (Ta=-20~+70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital core supply voltage	DVDD	1.7	1.8	1.9	V
PLL supply voltage	PVDD				
Digital I/O supply voltage	IOVDD	2.7	3.0	3.3	V
DAC supply voltage	AVDD				
Input "H" voltage	V _{IH}	IOVDD *0.8	-	IOVDD +0.2	V
Input "L" voltage	V _{IL}	-0.2	-	IOVDD *0.2	V

* Please connect the pull-up resistor of serial interface to digital I/O supply voltage.

* Please provide supply voltage to all power supply pins within 100 μsec. This method is the same also at the time of a power supply down.

Application example

- ROHM cannot provide adequate confirmation of patents.
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○ Electrical Characteristics (Ta=25°C, DVDD=PVDD=1.8V, IOVDD=AVDD=3.0V, GND=0V unless otherwise noted.)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
SYSCLK frequency 1	fsysclk1	-	27	-	MHz	656 input mode
SYSCLK frequency 2	fsysclk2	-	13.5	-	MHz	601 input mode
SYSCLK frequency deviation 1	dfsysclk1	-100	-	100	ppm	27MHz at 656 input mode
SYSCLK frequency deviation 2	dfsysclk2	-100	-	100	ppm	13.5MHz at 601 input mode
Digital core dynamic current	IDDCO	-	20	50	mA	^{*3}
Digital I/O dynamic current	IDDIO	-	0.5	10.0	mA	
Digital core static current	ISTDCO	-	1.5	8	μA	^{*4}
Digital I/O static current	ISTDIO	-	0.5	2	μA	^{*5}
Video DAC resolution	RES	-	-	10	bit	
Video DAC dynamic current	IDDV	-	40	55	mA	R _L =37.5Ω, R _{IREF} =1.2kΩ ^{*6}
Video DAC static current	ISTV	-	1	5	μA	RESETB=L ^{*2}
Integral linearity error	INL	-	±8.0	±15.0	LSB	R _L =37.5Ω, R _{IREF} =1.2kΩ ^{*6}
Differential linearity error	DNL	-	±1.0	±4.0	LSB	R _L =37.5Ω, R _{IREF} =1.2kΩ ^{*6}
Full scale voltage	V _{FS}	1.1	1.25	1.4	V	R _L =37.5Ω, R _{IREF} =1.2kΩ ^{*6}
PLL dynamic current	IDDP	-	1	2.5	mA	SYSCLK=27MHz input
PLL static current	ISTP	-	1	5	μA	^{*7}

^{*3} Built-in color bar output mode at 27MHz.

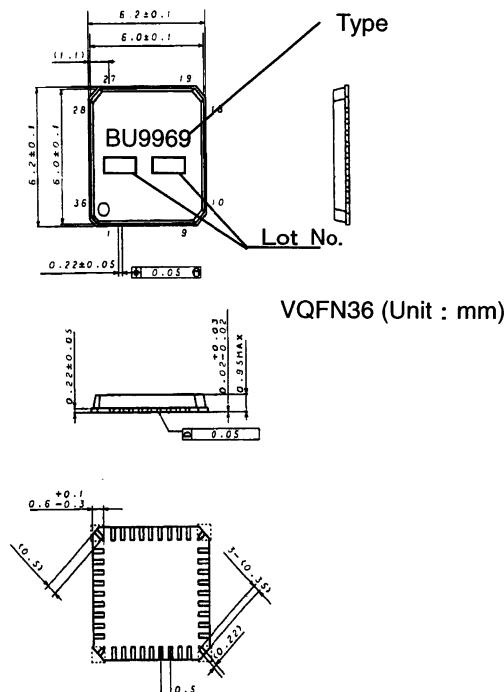
^{*4} RESETB = Low

^{*5} RESETB = Low and all input pins = Low

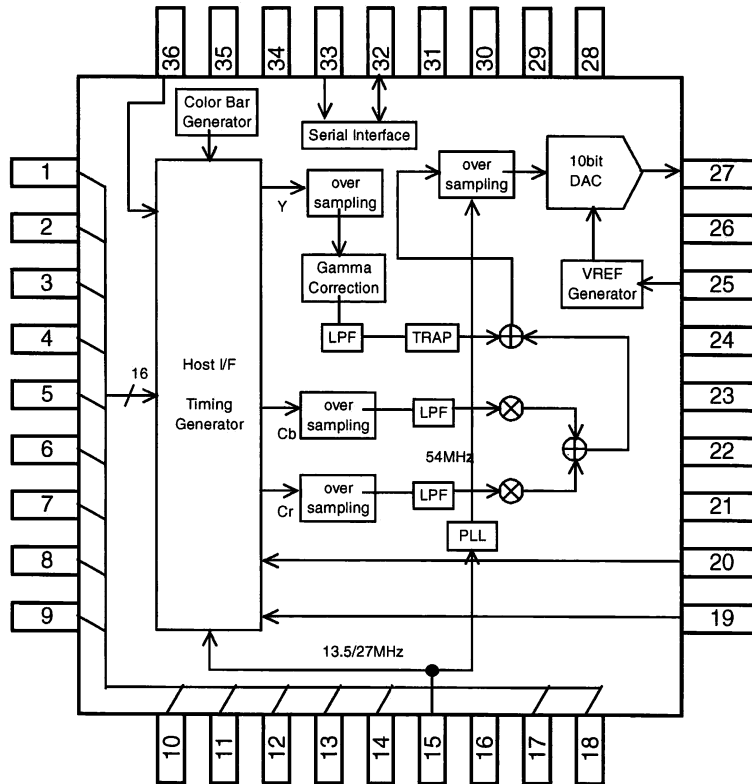
^{*6} R_L=37.5Ω shows the value at measurement.

^{*7} Set the RESETB or 1st bit of register PWD_M to "0".

○ Package outline



○ Block diagram



○ Terminal functions

Terminal No.	Terminal name	Description of terminals			Terminal No.	Terminal name	Description of terminals
		601 RGB	601 YCrCb	656 YCrCb			
1	DATA [0]	R[0]	Y[0]	YCbCr[0]	19	HS	Horizontal synchronous signal input
2	DATA [1]	R[1]	Y[1]	YCbCr[1]	20	VS	Vertical synchronous signal input
3	DATA [2]	R[2]	Y[2]	YCbCr[2]	21	GND	GND for digital core power supply
4	DATA [3]	R[3]	Y[3]	YCbCr[3]	22	IOVDD	I/O power supply
5	DATA [4]	R[4]	Y[4]	YCbCr[4]	23	N.C.	No Connection
6	DATA [5]	G[0]	Y[5]	YCbCr[5]	24	GND	GND for analog power supply
7	DATA [6]	G[1]	Y[6]	YCbCr[6]	25	IREF	DAC reference current setting terminal
8	DATA [7]	G[2]	Y[7]	YCbCr[7]	26	AVDD	Analog power supply
9	DATA [8]	G[3]	CbCr[0]	(Low)	27	VOUT	Composite video output
10	DATA [9]	G[4]	CbCr[1]	(Low)	28	TEST0	Test terminal
11	DATA [10]	G[5]	CbCr[2]	(Low)	29	TEST1	Test terminal
12	DATA [11]	B[0]	CbCr[3]	(Low)	30	TEST2	Test terminal
13	DATA [12]	B[1]	CbCr[4]	(Low)	31	TEST3	Test terminal
14	DATA [13]	B[2]	CbCr[5]	(Low)	32	SDI	Serial data input
15	SYCLK	System clock input			33	SCLK	Serial clock input
16	DVDD	Digital core power supply			34	GND	GND for PLL power supply
17	DATA [14]	B[3]	CbCr[6]	(Low)	35	PVDD	PLL power supply
18	DATA [15]	B[4]	CbCr[7]	(Low)	36	RESETB	Reset input (L : reset)

○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as power-supply voltage, operating temperature range, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(1 0) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(1 1) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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