SBOS380A − FEBRUARY 2007 − REVISED MAY 2007

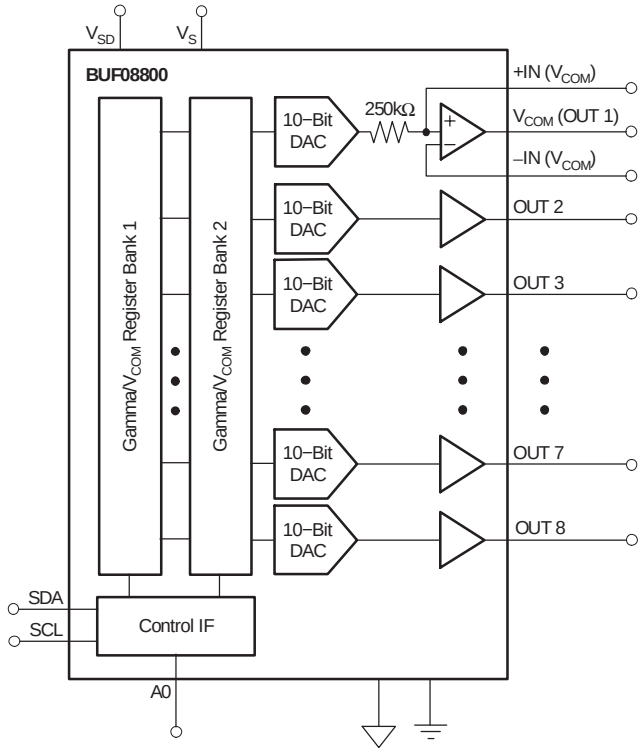
Programmable Reference Generator and 400mA V_{COM} Driver

FEATURES

- 10-BIT RESOLUTION
- 7- OR 8-CHANNEL GAMMA CORRECTION
- INTEGRATED V_{COM} DRIVER: 400mA PEAK CURRENT
- DIGITAL GATE VOLTAGE ADJUSTMENT CIRCUITS
- RAIL-TO-RAIL OUTPUT
- LOW SUPPLY CURRENT: 1mA/ch
- SUPPLY VOLTAGE: 7V to 22V
- DIGITAL SUPPLY: 2.0V to 5.5V
- INDUSTRY-STANDARD, TWO-WIRE INTERFACE
- HIGH ESD RATING: 4kV HBM

APPLICATIONS

- TFT-LCD REFERENCE DRIVERS
- REFERENCE VOLTAGE GENERATORS



DESCRIPTION

The BUF08800 reference generator offers eight programmable reference channels that can be used depending on the application needs. For example, all eight channels can be used for gamma correction, or some as gamma references and some to digitally adjust the gate voltages or V_{COM}.

All gamma/V_{COM} channels swing to within 100mV of the positive or negative supply rail with a 10mA load. All channels are programmed using a standard two-wire interface that supports standard operation up to 400kHz and also high-speed data transfer up to 3.4MHz.

The integrated V_{COM} driver features up to 400mA peak current drive. V_{COM} voltage compensation at different locations on the LCD panel can be accomplished using the negative input of the integrated V_{COM} op amp.

The Gate High and Low voltages can differ because of changes in panel size or technology. The BUF08800 supports digital adjustment circuits for the gate voltages. This feature enables the adjustment of gate voltages through software without changing hardware, thus reducing development time and risk.

The BUF08800 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process allows very dense logic as well as high supply voltage operation of up to 22V.

The BUF08800 is available in a small TSSOP-20 PowerPad™ package, and is specified from −40°C to +85°C.

RELATED PRODUCTS

FEATURES	PRODUCT
12-Channel Gamma Correction Buffer	BUF12800
20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800
16-, 20-Channel Prog. Buffer with Memory	BUF20820
Programmable V_{COM} Driver	BUF01900
18V Supply, Traditional Gamma Buffers	BUF11704
22V Supply, Traditional Gamma Buffers	BUF11705

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_S	+24V
Supply Voltage, V_{SD}	+6V
Supply Input Terminals, SCL, SDA, AO, LD:	
Voltage	−0.5V to +6V
Current	±10mA
Output Short-Circuit(2)	Continuous
Operating Temperature	−40°C to +95°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+125°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Short-circuit to ground.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

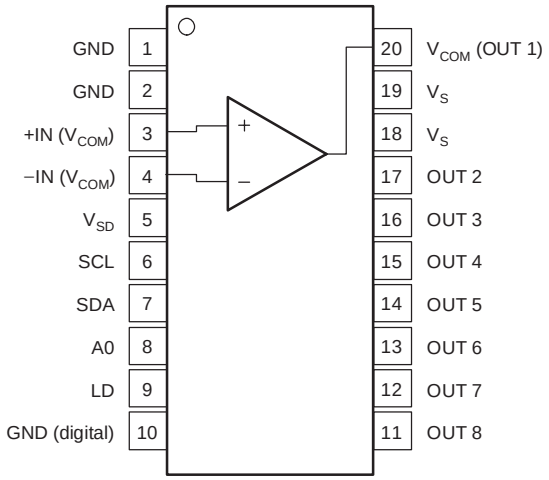
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
BUF08800	HTSSOP-20	PWP	BUF08800	BUF08800AIPWPR

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS

Top View **HTSSOP**

BUF08800



ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range: **T_A = −40°C to +85°C.**

At T_A = +25°C, V_S = +18V, V_{SD} = 2.5V, R_L = 1.5kΩ to GND, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF08800 MIN	BUF08800 TYP	BUF08800 MAX	UNITS
ANALOG						
Gamma Buffer Channels						
Reset Value		Code = 512		9		V
Buffer 2−4 Output Swing: High		**Code = 1023, Sourcing 10mA**	**17.8**	**17.85**		**V**
Buffer 2−4 Output Swing: Low		**Code = 0, Sinking 10mA**		**0.7**	**1**	**V**
Buffer 5−8 Output Swing: High		**Code = 1023, Sourcing 10mA**	**17.0**	**17.2**		**V**
Buffer 5−8 Output Swing: Low		**Code = 0, Sinking 10mA**		**0.2**	**0.25**	**V**
Continuous Output Current				30		mA
Output Accuracy				±10	±50	mV
vs Temperature		Code 512		±20		µV/°C
Integral Nonlinearity	INL			0.3	1	Bits
Differential Nonlinearity	DNL			0.3	2.5	Bits
Load Regulation, 10mA	REG	Code = 512, I_{OUT} = +5mA to −5mA Step		0.5	1.5	mV/mA
V_{COM} Driver/OUT 1						
Reset Value		Code = 00, No Load on Pin 2, I_{OUT} = 0		9		V
Driver Input Range		I_{OUT} = 0mA	0.7		17.9	V
Driver Offset		Referred to Pin 2, Code = 512		1	±5	mV
V_{COM}/OUT 1 Output Swing: High		**Pin 9, Code = 1023, Sourcing 10mA**	**17.8**	**17.9**		**V**
V_{COM}/OUT 1 Output Swing: Low		**Pin 9, Code = 0, Sinking 10mA**		**0.7**	**1**	**V**
V_{COM}/OUT 1 Output Swing: High		**Pin 9, Code = 1023, Sourcing 400mA**	**14**	**14.6**		**V**
V_{COM}/OUT 1 Output Swing: Low		**Pin 9, Code = 0, Sinking 400mA**		**3.5**	**4**	**V**
V_{BIAS} Output Impedance		Pin 2		250		kΩ
Overall Output Accuracy		Pin 20		±20	±50	mV
vs Temperature		Code = 512		±25		µV/°C
Integral Nonlinearity	INL	Pin 20		0.3	1	Bits
Differential Nonlinearity	DNL	Pin 20		0.3	2.5	Bits
Load Regulation, 100mA	REG	Pin 20, Code = 512, I_{OUT} = +200mA to −200mA Step		0.5	1.5	mV/mA
Program to Out Delay	t_D	All Channels		5		µs
ANALOG POWER SUPPLY						
Operating Range			7		22	V
Total Analog Supply Current	I_S	Outputs at Reset Values, No Load		7	15	mA
Over Temperature					**15**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		$0.7 \times V_{SD}$			V
Logic 0 Input Voltage	V_{IL}				$0.3 \times V_{SD}$	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency		**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Range	V_{SD}		2.0		5.5	V
Digital Supply Current(1)	I_{SD}	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		25	50	µA
Over Temperature				**100**		**µA**
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range		Junction Temperature < +125°C	−40		+95	°C
Storage Range			−65		+150	°C
Thermal Resistance(2)						
HTSSOP-20	θ_{JA}			35		°C/W
HTSSOP-20	θ_{JC}			20		°C/W

(1) See typical characteristic curve *Digital Supply Current vs Two-Wire Bus Activity.*

(2) Thermal pad attached to printed circuit board (PCB), 0lfm airflow, and 76mm × 76mm copper area.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +18V, V_{SD} = 2.5V, R_L = 1.5kΩ to GND, and C_L = 200pF, unless otherwise noted.

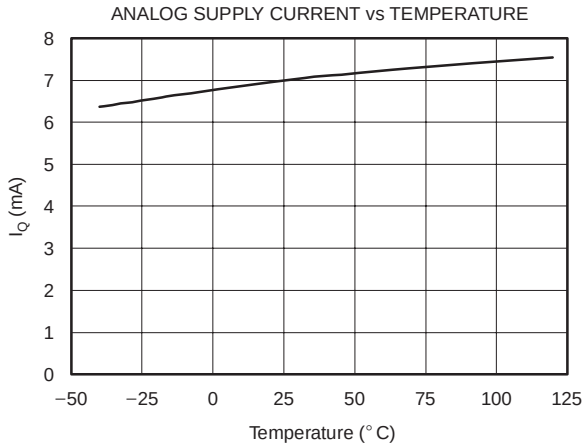


Figure 1

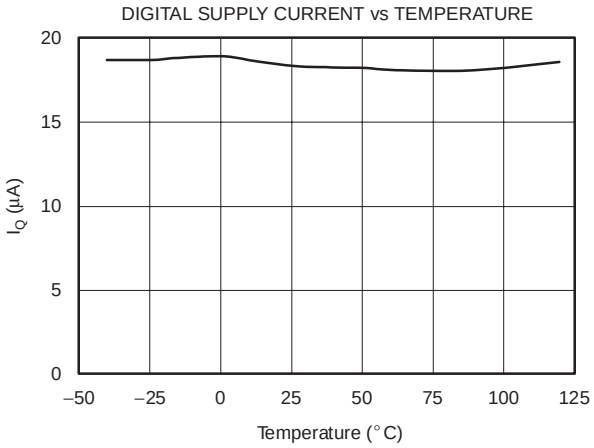


Figure 2

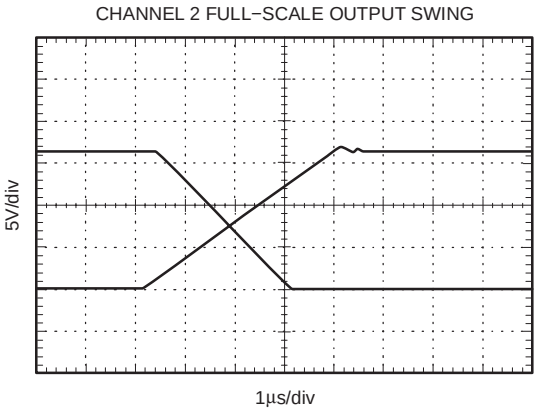


Figure 3

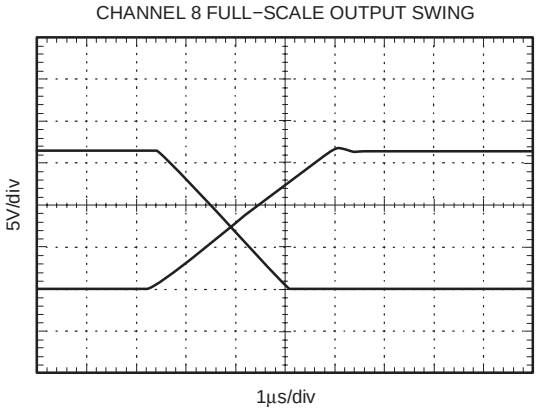


Figure 4

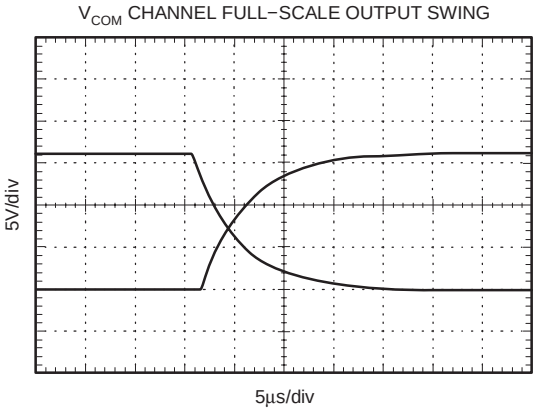


Figure 5

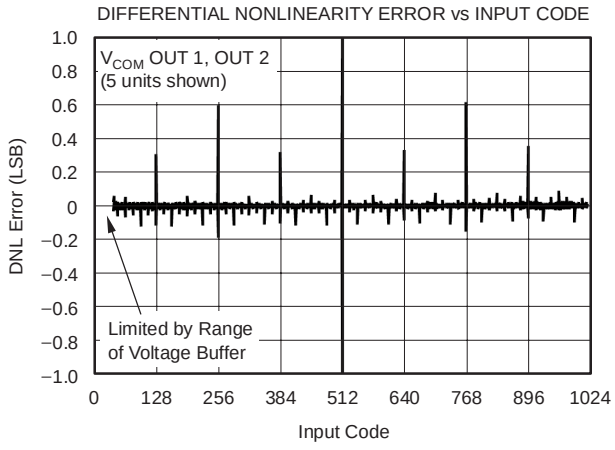


Figure 6

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +18V, V_{SD} = 2.5V, R_L = 1.5kΩ to GND, and C_L = 200pF, unless otherwise noted.

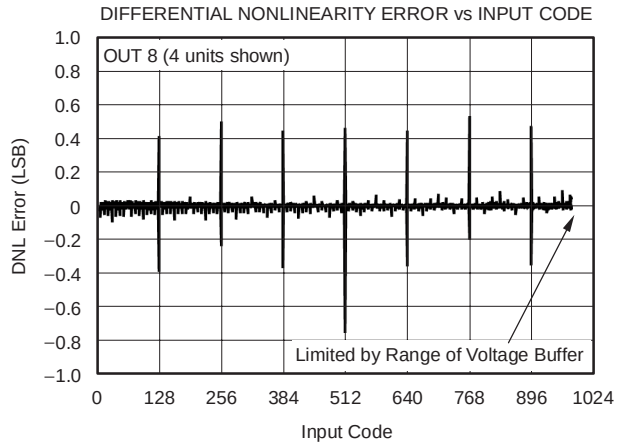


Figure 7

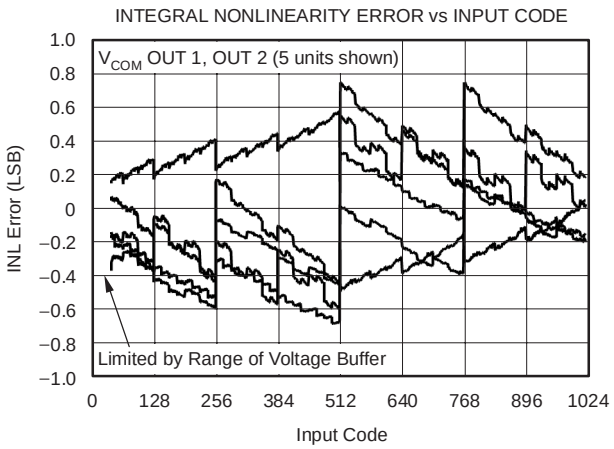


Figure 8

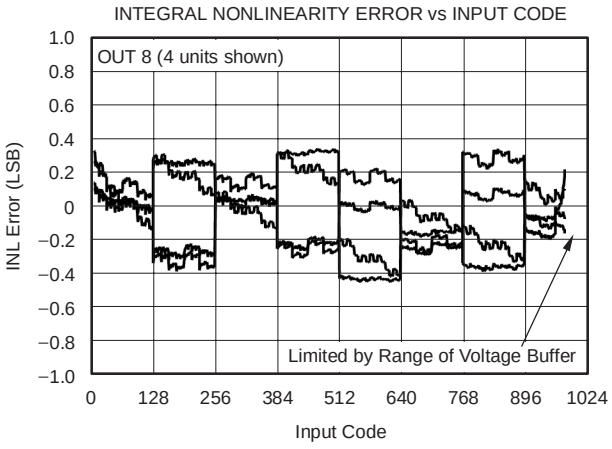


Figure 9

APPLICATIONS INFORMATION

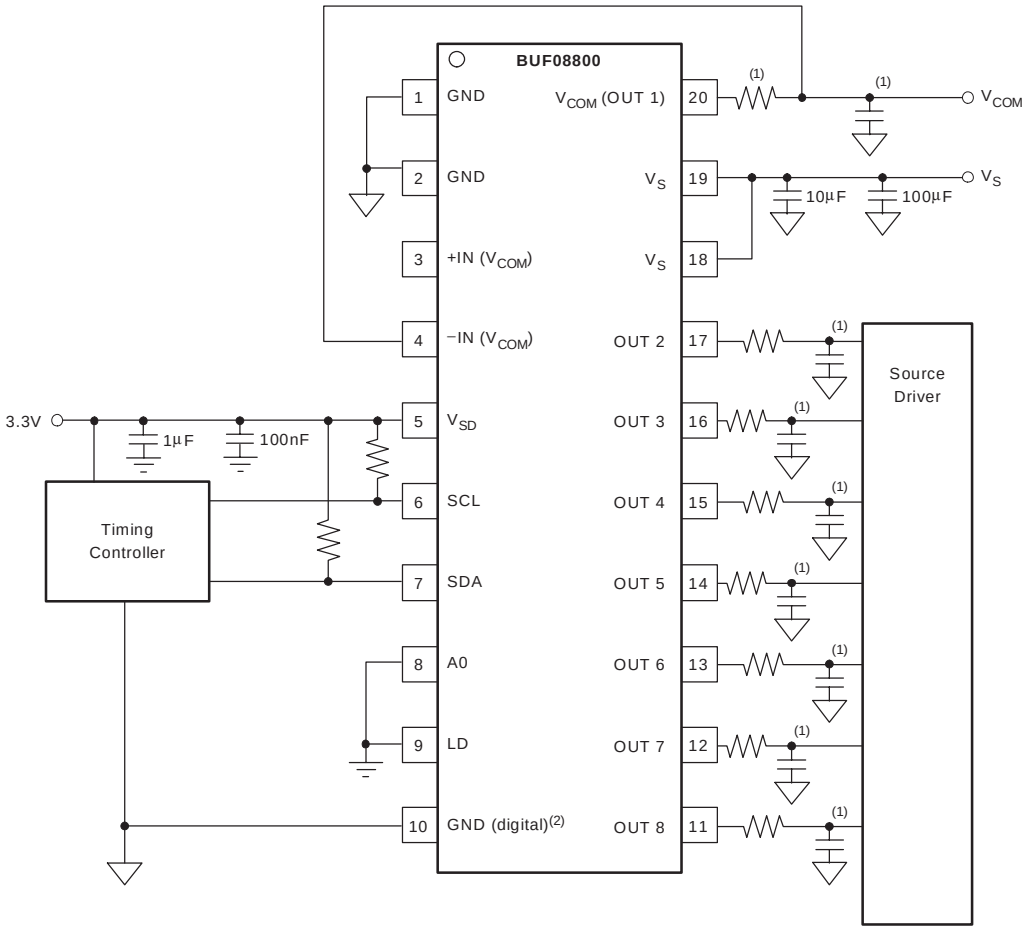
The BUF08800 programmable voltage reference allows fast and easy adjustment of eight programmable reference outputs, each with 10-bit resolution. It allows very simple, time-efficient adjustment of the V_{COM} and gamma reference voltages. The BUF08800 is programmed through a high-speed, standard two-wire interface. The BUF08800 features a double-register structure for each digital-to-analog converter (DAC) channel to simplify the implementation of dynamic gamma control (see the *Dynamic Control* section). This architecture allows pre-loading of register data and rapid updating of all channels simultaneously.

V_{COM} (OUT 1) and buffers 2−4 are able to swing to within 200mV of the positive supply rail, and to within 1V of the negative supply rail. Buffers 5−8 are able to swing to within 1V of the positive supply rail, and to within 250mV of the negative supply rail. (See the *Electrical Characteristics* table for further information.)

Buffers 2−8 are capable of full-scale change in output voltage in less than 4µs; see Figure 4.

The BUF08800 uses an analog supply of 7V to 22V and a digital supply of 2V to 5.5V. The digital supply must be applied prior to or simultaneously with the analog supply to avoid excessive current and power consumption; damage to the device may occur if it is left connected only to the analog supply for an extended time.

Figure 10 shows the BUF08800 in a typical configuration. In this configuration, the BUF08800 device address is 74h. The output of each DAC is immediately updated as soon as data is received in the corresponding register (LD = 0).



(1) RC combination optional
(2) GND and GND (digital) are internally connected and must be at the same voltage potential.

Figure 10. Typical Application Configuration

TWO-WIRE BUS OVERVIEW

The BUF08800 communicates through an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and 8 bits of data are sent followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF08800 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF08800.

ADDRESSING THE BUF08800

The address of the BUF08800 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 74h (1110100). If the A0 pin is HIGH, the device acknowledges on address 75h (1110101), as shown in Table 1.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

Table 1. BUF08800 Bus Address Options

BUF08800 ADDRESS	ADDRESS
A0 pin is LOW (device will not acknowledge on address 74h)	111 0100
A0 pin is HIGH (device will acknowledge on address 74h)	111 0101

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF08800 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with SCL = 400kHz, following the START condition; *xxx* are bits unique to the Hs-capable master, and can be any value. The BUF08800 responds to the High-speed mode command regardless of the value of these last three bits. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF08800 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. On receiving a master code, the BUF08800 switches on its Hs mode filters, and communicates at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF08800 switches out of Hs mode at the first occurrence of a STOP condition.

GENERAL CALL RESET AND POWER-UP

The BUF08800 responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF08800 acknowledges both bytes. Upon receiving a General Call Reset, the BUF08800 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

The BUF08800 automatically performs a reset upon power-up. As part of the reset, the BUF08800 is configured for all outputs to change to mid-value, $V_S/2$.

The BUF08800 resets all outputs to mid-value ($V_S/2$) when the device address is sent, followed by a valid DAC address with bits D7 to D5 set to ‘100’. If these bits are set to ‘010’, only the DAC being addressed in this most significant byte and the following least significant byte will be reset.

Table 2. Quick-Reference Table of Commands

COMMAND	CODE
General Call Reset	Address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110).
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where xxx are bits unique to the Hs-capable master. This byte is called the Hs master code.

OUTPUT VOLTAGE

Buffer output values are determined by the supply voltage and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1:

$$V_{OUT} = \left(\frac{V_S}{1024} \times \text{Decimal Value of Code} \right) \quad (1)$$

The BUF08800 outputs 2−8 are capable of a full-scale voltage output change in typically 4µs—no intermediate steps are required. Output swing is limited to the voltages specified in the Electrical Characteristics table. V_{COM} (OUT 1) through OUT 4 can swing from 1V to V_S − 0.2V; OUT 5 through OUT 8 can swing between 0.25V and V_S − 1V.

READ/WRITE OPERATIONS

The BUF08800 is able to read from a single DAC or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. See the timing diagrams; Figure 11 through Figure 14. DAC addresses begin with 0000, which correspond to V_{COM} (OUT 1), through 0111, which correspond to DAC_8; this address archetecture is shown in Table 3. Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

Table 3. Quick-Reference Table of DAC Addresses

DAC	ADDRESS
V_{COM} OUT 1	0000 0000
DAC 2	0000 0001
DAC 3	0000 0010
DAC 4	0000 0011
DAC 5	0000 0100
DAC 6	0000 0101
DAC 7	0000 0110
DAC 8	0000 0111

Writing

To write to a single DAC register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08800 acknowledges this byte.
3. Send a DAC address byte. Bits D7−D3 are unused and must be set to 0. Bits D2−D0 are the DAC address. Only DAC addresses 0000 to 0111 are valid and will be acknowledged.
4. Send two bytes of data for the specified DAC. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are used), followed by the least significant byte (bits D7−D0). The DAC register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF08800 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register will not be updated. Updating the DAC register is not the same as updating the DAC output voltage. See the *Output Latch* section.

The process of updating multiple registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF08800 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP condition is sent.

To write to multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08800 acknowledges this byte.
3. Send either the V_{COM} (OUT 1) address byte to start at the first DAC (V_{COM} OUT 1) or send the address of whichever DAC is the first to be updated. The BUF08800 begins with this DAC and steps through subsequent DACs in sequential order.
4. Send the bytes of data. The first two bytes are for the DAC addressed in step 3. Its register is automatically updated after receiving the second byte. The next two bytes are for the following DAC. The DAC register is updated after receiving the fourth byte. The last two bytes are for DAC_8. The DAC register is updated after receiving the 24th byte. For each DAC, begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning), followed by the least significant byte (bits D7−D0).
5. Send a STOP condition on the bus.

The BUF08800 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DACs that have received both bytes will be updated.

Reading

To read the register of one DAC:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08800 acknowledges this byte.
3. Send a DAC address byte. Bits D7−D3 have no meaning and must be ‘0’; bits D2−D0 are the DAC address. Only DAC addresses 0000 to 0111 are valid and will be acknowledged.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF08800 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning); the next is the least significant byte (bits D7−D0).
7. Acknowledge after receiving each byte.
8. Send a STOP condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

To read multiple DAC registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF08800 acknowledges this byte.
3. Send either the V_{COM} DAC (V_{COM} OUT 1) address byte to start at the first DAC or send the address byte for whichever DAC is the first in the sequence of DACs to be read. The BUF08800 begins with this DAC and steps through subsequent DACs in sequential order.
4. Send the device address and read/write bit = HIGH.
5. Receive bytes of data. The first two bytes are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning). The next byte is the least significant byte (bits D7−D0).
6. Acknowledge after receiving each byte.
7. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

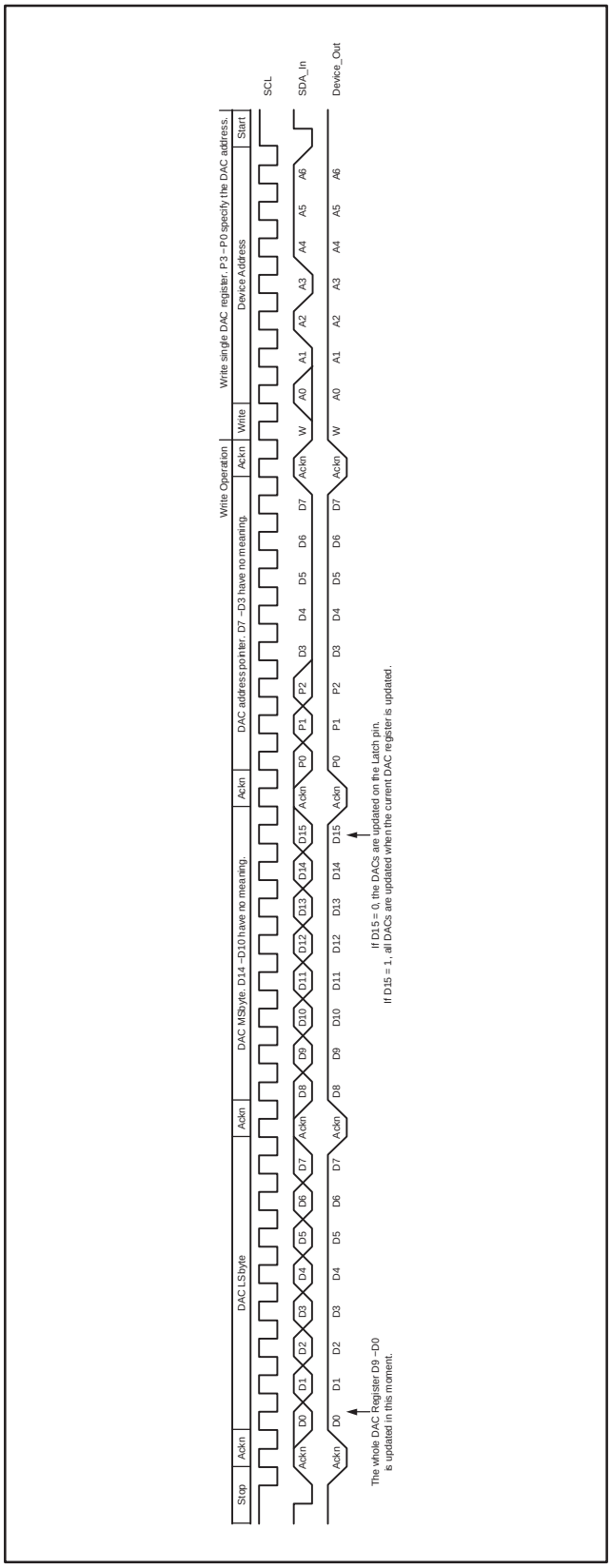


Figure 11. Write Single DAC Register

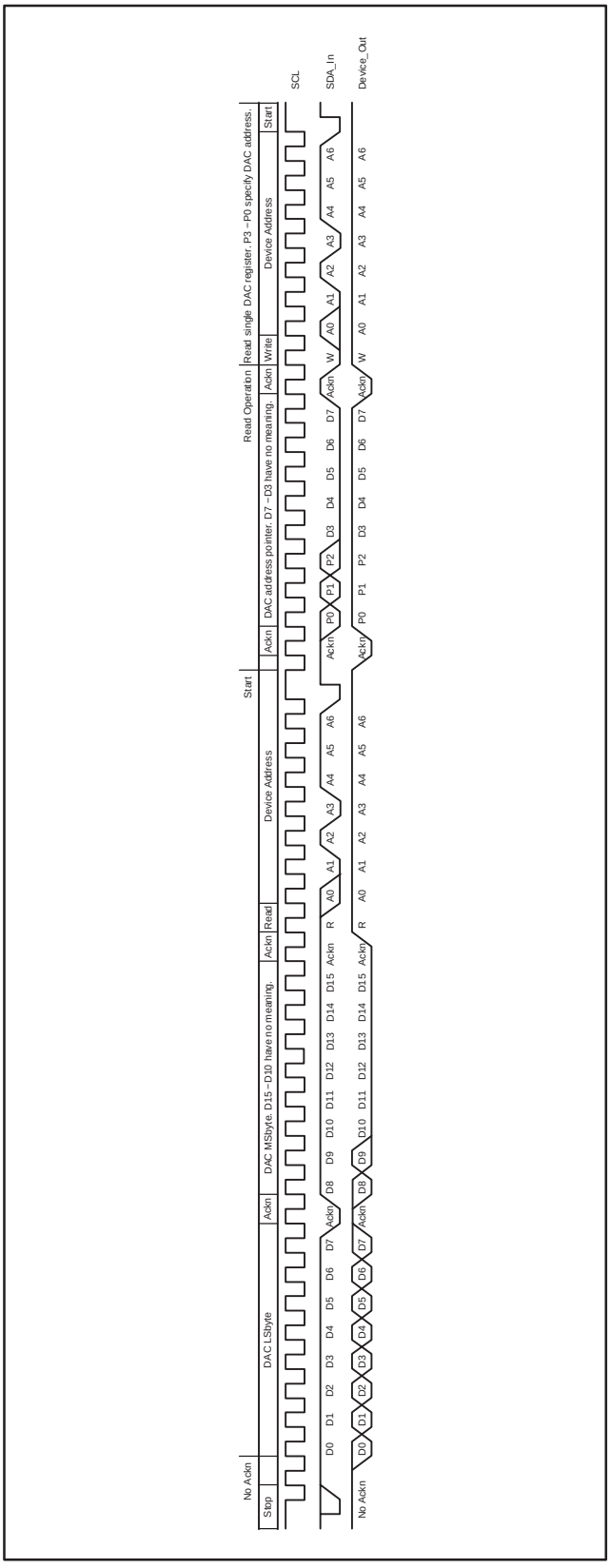


Figure 12. Read Single DAC Register

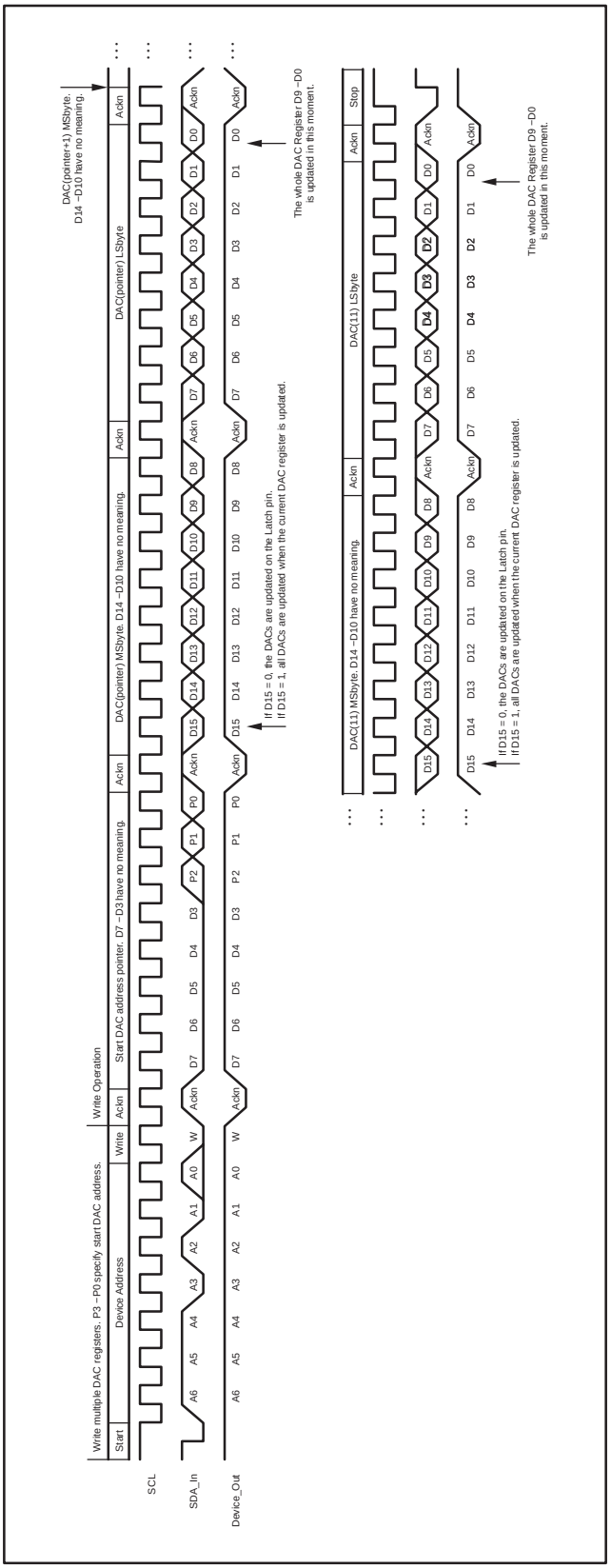


Figure 13. Write Multiple DAC Registers

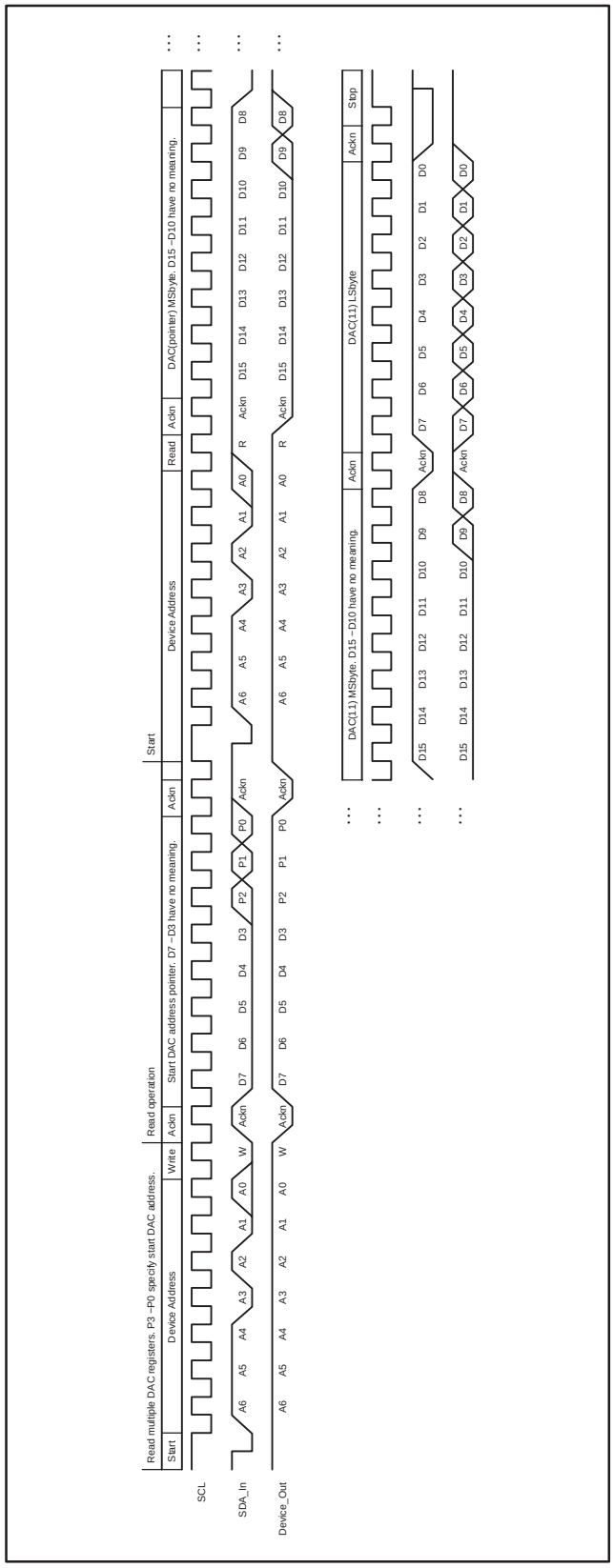


Figure 14. Read Multiple DAC Registers

OUTPUT LATCH

Because the BUF08800 features a double-buffered register structure, updating a DAC register is not the same as updating the DAC output voltage. There are three methods for latching transferred data from the storage registers into the DACs to update the DAC output voltage.

Method 1 requires externally setting the latch pin (LD) = LOW, which updates each DAC output voltage whenever its corresponding register is updated.

Method 2 externally sets LD = HIGH to allow all DAC output voltages to retain their values during data transfer and until LD = LOW, which simultaneously updates the output voltages of all DACs to the new register values.

Method 3 uses software control. LD is maintained HIGH, and all DACs are updated when the master writes a '1' in bit 15 of any DAC register. The update occurs after receiving the 16-bit data for the currently-written register.

Use methods 2 and 3 to transfer a future data set into the first bank of registers in advance to prepare for a very fast update of DAC output voltages.

The General Call Reset and the power-up reset update the DACs regardless of the state of the latch pin (LD).

REPLACEMENT OF TRADITIONAL GAMMA BUFFER

Traditional gamma buffers rely on a resistor string (often using expensive 0.1% resistors) to set the gamma voltages. During development, the optimization of these gamma voltages can be time-consuming. Programming these gamma voltages with the BUF08800 can significantly reduce the time required for gamma voltage optimization. The final gamma values can be written into the internal OTP memory to replace a traditional gamma buffer solution. Figure 16a shows the traditional resistor string; Figure 16b shows the more efficient alternative method using the BUF08800.

The BUF08800 uses the most advanced high-voltage CMOS process available today, allowing it to be competitive with traditional gamma buffers.

Programmability offers the following advantages:

- Shortens development time significantly.
- Increases reliability by eliminating more than 18 external components.
- Eliminates manufacturing variance between panels.
- Allows a single panel to be built for multiple customers, with loading of customer-dependent gamma curves during final production. This method significantly lowers inventory cost and risk, and simplifies inventory management.
- Allows demonstration of various gamma curves to LCD monitor makers by simply uploading a different set of gamma values.
- Allows simple adjustment of gamma curves during production to accommodate changes in the panel manufacturing process or end-customer requirements.
- Decreases cost and space.

V_{COM} ADJUSTMENT

The output of the V_{COM} digital-to-analog converter (DAC) is internally connected to the input of the V_{COM} buffer. As a result of the high 10-bit resolution, the V_{COM} voltage can directly be adjusted without the need for external circuitry. The integrated V_{COM} driver can deliver up to 400mA of peak current. In addition, the negative input is brought out as a separate pin on the package to facilitate V_{COM} compensation or equalization of the V_{COM} voltage across the panel (see Figure 17).

Traditional V_{COM} adjustment uses a mechanical potentiometer and a voltage divider for adjustment, as shown in Figure 15. The programmable V_{COM} channel integrated in the BUF08800 is also able to use an external voltage divider connected to +IN. It can be used to set the initial V_{COM} voltage as well as the adjustment range (see Figure 17). Using this method, even at power-on the initial V_{COM} setting is close to the optimized V_{COM} value, without any programming. The external voltage divider also limits the adjustment range that typically leads to a smaller number of adjustment steps. In addition, the V_{COM} output voltage is limited only to the adjustment range, thereby protecting the panel from undesirable V_{COM} voltages.

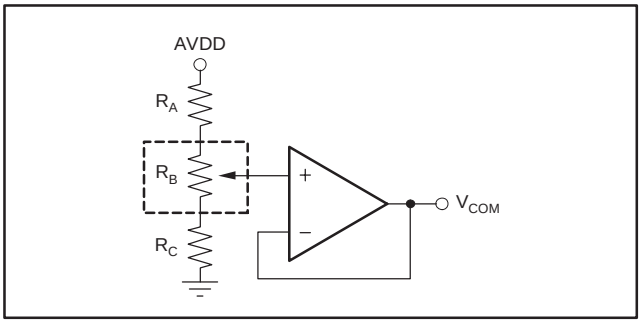


Figure 15. Traditional V_{COM} Adjustment. External voltage divider sets initial V_{COM} voltage as well as adjustment range.

The 10-bit DAC acts as a voltage source with a nominal 250kΩ output impedance; see Figure 17. For example, at code 000h, the lowest V_{COM} voltage is achieved because the 250kΩ impedance is now in parallel with R_2, which lowers the impedance of the lower side of the voltage divider. Consequently, code 3FFh results in the highest adjustable V_{COM} voltage.

However, an external voltage divider is not required for correct function of the V_{COM} channel integrated in the BUF08800. Once the desired output level (that is, minimum flicker) is obtained, the corresponding code can be stored in the external EEPROM memory.

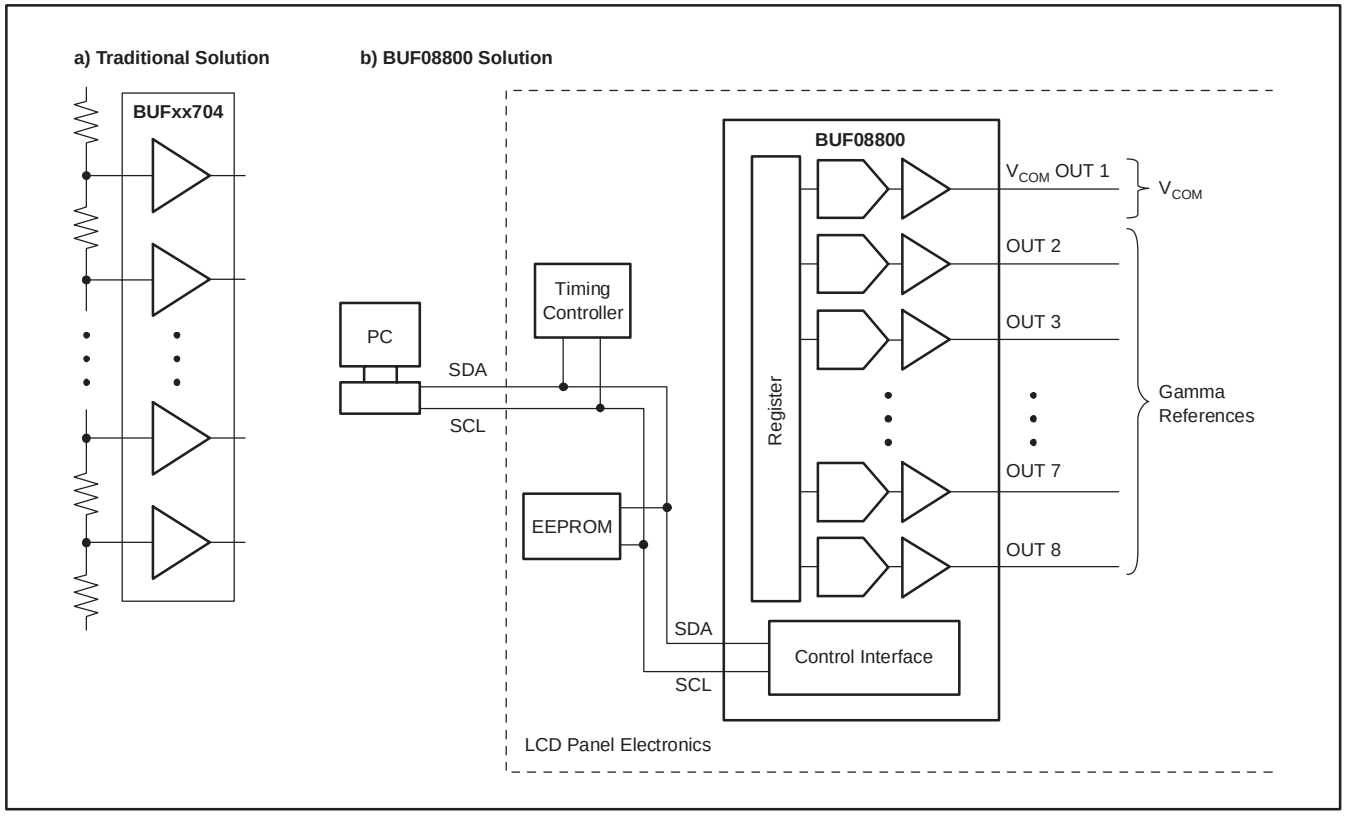


Figure 16. Replacement of the Traditional Gamma Buffer

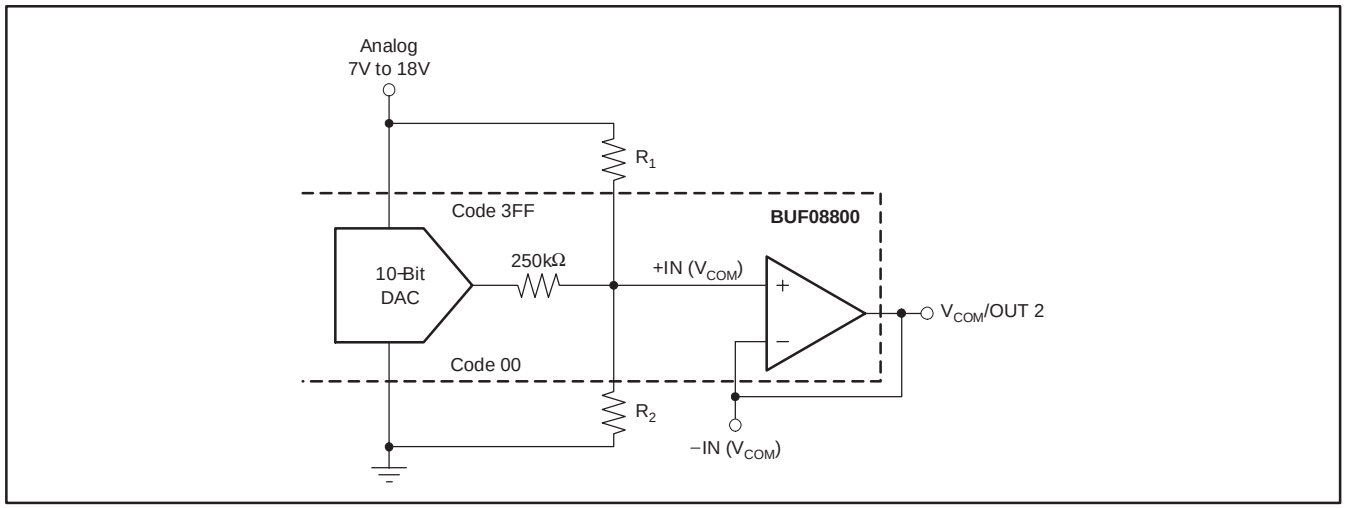


Figure 17. Simplified Block Diagram for V_{COM} Adjustment Using the BUF08800

DIGITAL GATE-VOLTAGE (V_{GH}, V_{GL}) ADJUSTMENT

Different panel sizes and manufacturing technology often require different gate-high (V_{GH}) and gate-low (V_{GL}) voltages. Optimizing the gate-high and -low voltages for best panel performance can be time consuming. Using channels 7 and 8, which are capable of swinging close to GND, allows a wide range of programmable adjustment of both V_{GL} and V_{GH}. This procedure of optimizing V_{GH} and V_{GL} is greatly simplified and the LCD power-supply solution can readily be used in other panels without modification to the hardware.

TYPICAL APPLICATIONS FOR BUF08800

1. **All eight channels are used for gamma correction.** The V_{COM} channel swings very close to V_S. It can therefore be used to generate the highest gamma voltage. V_{COM} (OUT 1) together with OUT 2 and OUT 3 would then form the four upper gamma references and OUT 4 through OUT 8 would be used for the four lower gamma references.
2. **Five-channel gamma reference, two-channel gate voltage adjust, one-channel V_{COM}.** For applications that can accept a total of five gamma references, the BUF08800 can be used to digitally adjust the gate voltages. Two channels would be used to adjust V_{GH} and V_{GL}. In this case, the suggested use of channels would be to use OUT 2 through OUT 6 for generating the gamma references and OUT 7 and OUT 8 for generating the V_{GH} and V_{GL} references. OUT 1 would be used as the V_{COM} channel.
3. **Six-channel gamma, one V_{COM} channel.** For applications requiring one V_{COM} channel and an even number of gamma channels, the BUF08800 would still be a very cost-competitive solution. Channels 2 through 7 would be used to generate the gamma references.

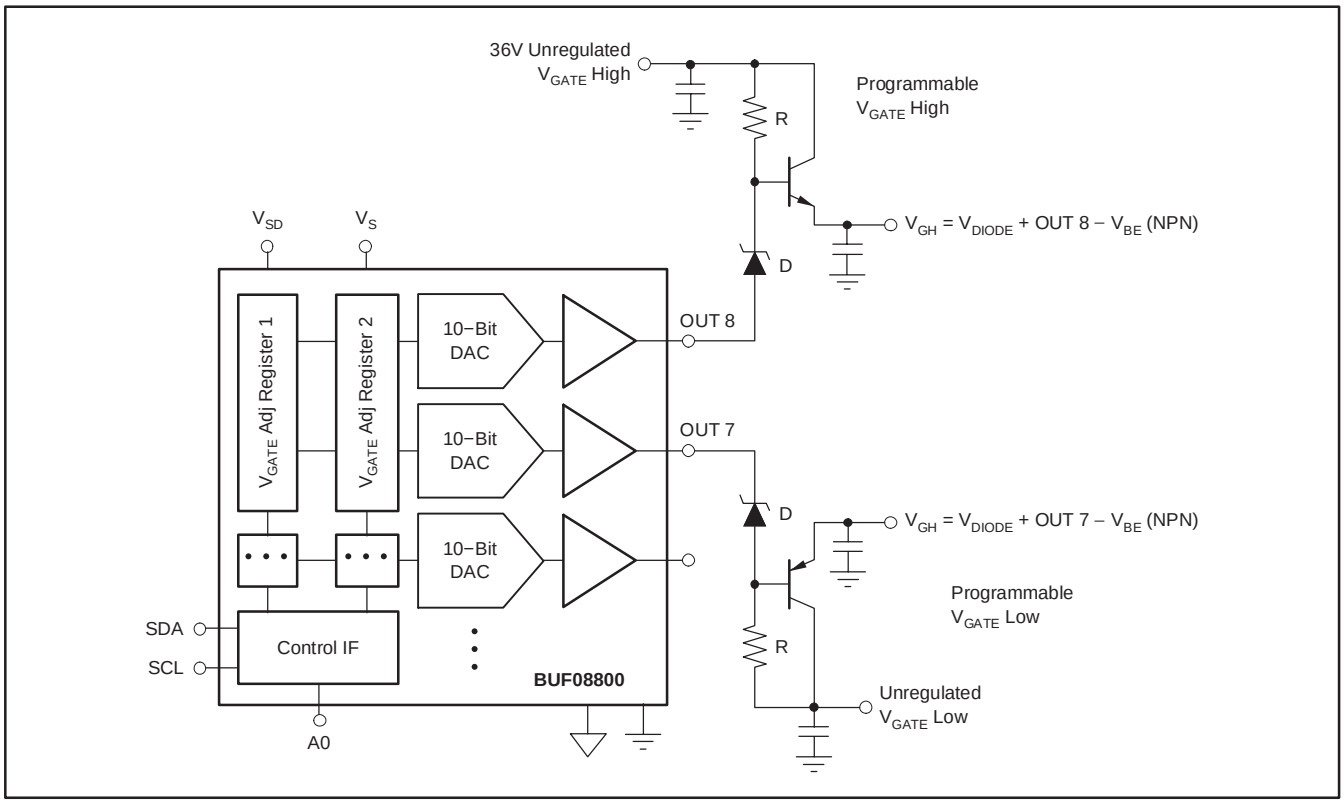


Figure 18. Using the BUF08800 to Digitally Adjust the V_{GH} Voltage

GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF08800 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted; see Figure 19(a) and Figure 19(b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 19(c). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This process provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns (2×4) for the HTSSOP-20 DAP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. The vias help dissipate the heat generated by the BUF08800 IC. The additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF08800 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its ten holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF08800 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

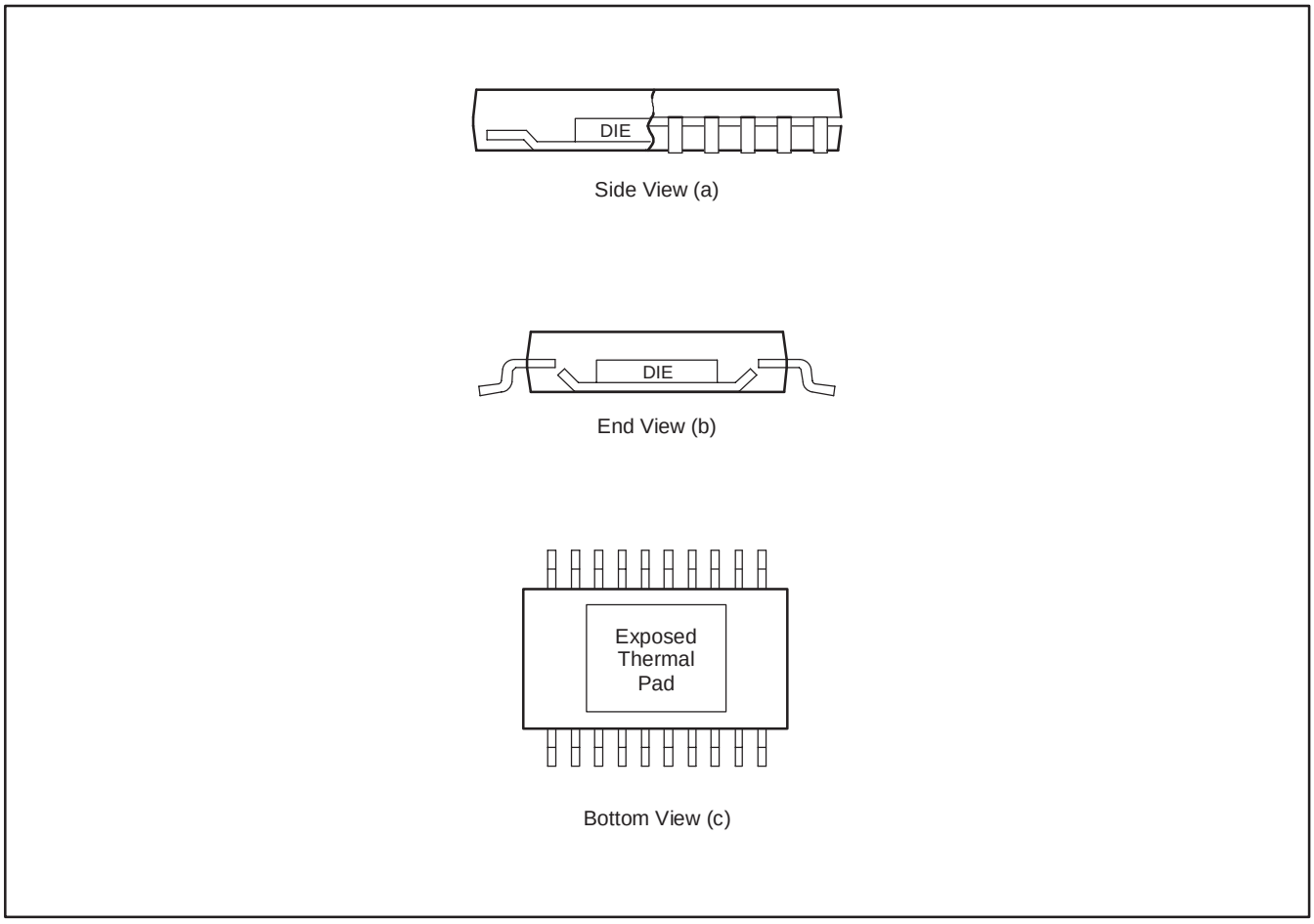


Figure 19. Views of Thermally-Enhanced DCP Package

For a given θ_{JA}, the maximum power dissipation is shown in Figure 20, and is calculated by Equation 3:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (2)$$

Where:
P_D = maximum power dissipation (W)
T_{MAX} = absolute maximum junction temperature (+125°C)
T_A = ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = thermal coefficient from junction-to-case (°C/W)
θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

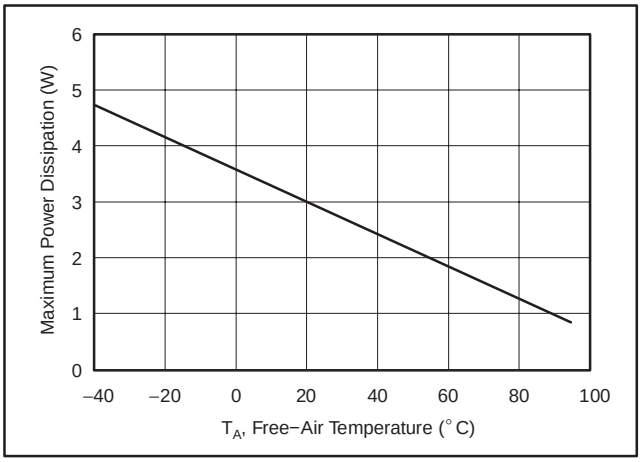


Figure 20. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

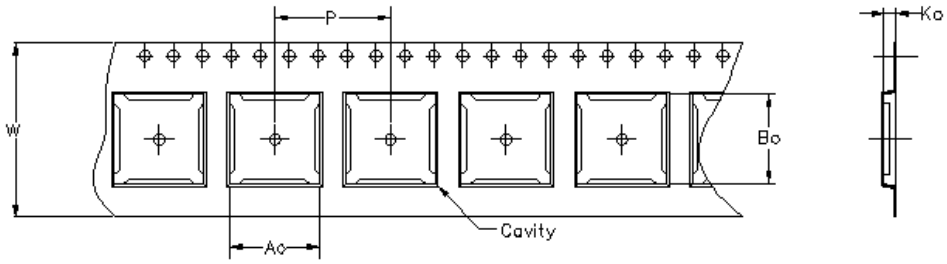
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BUF08800AIPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BUF08800AIPWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

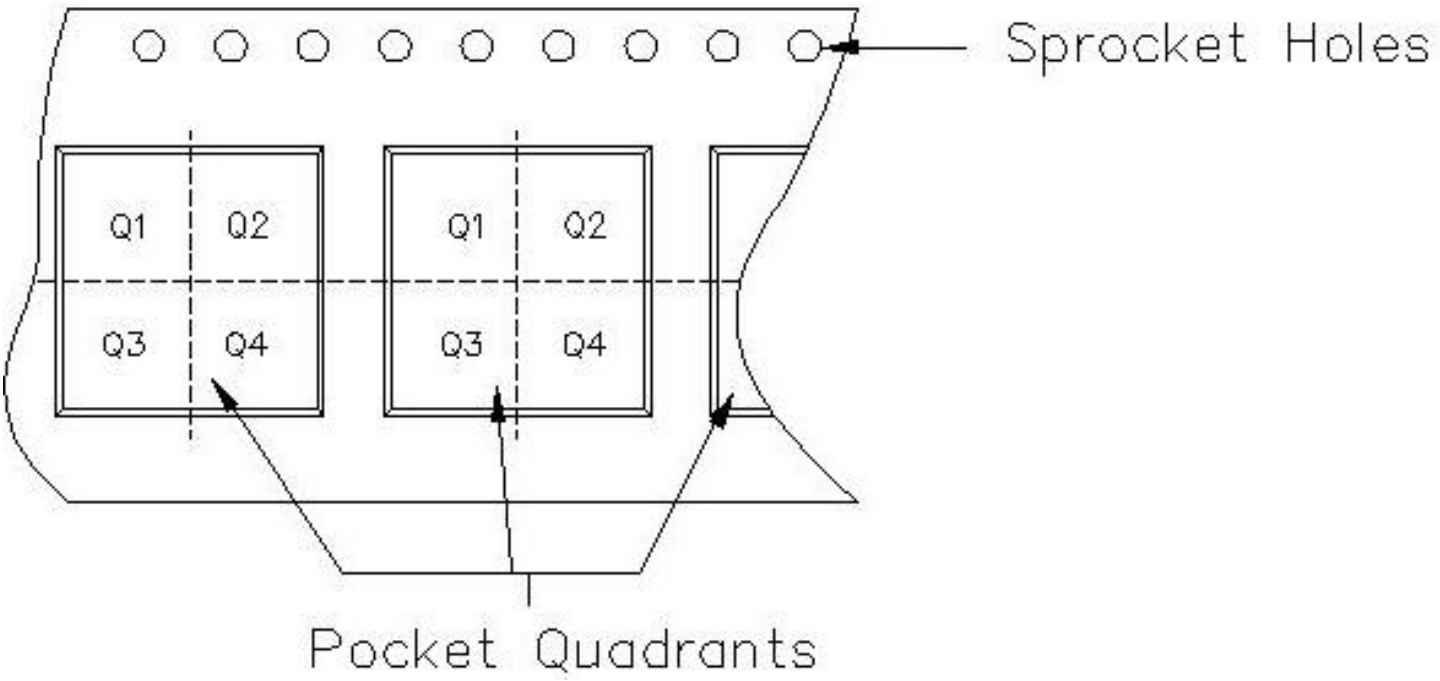
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



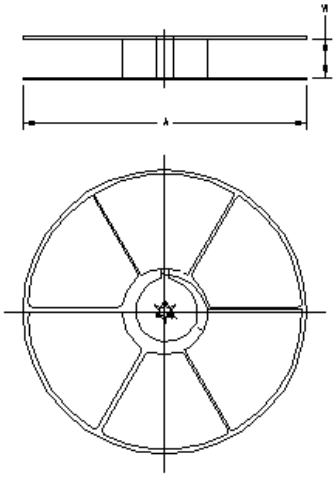
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



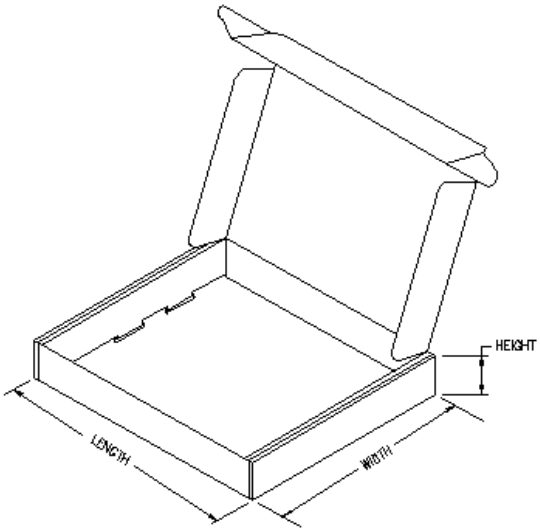
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF08800AIPWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1



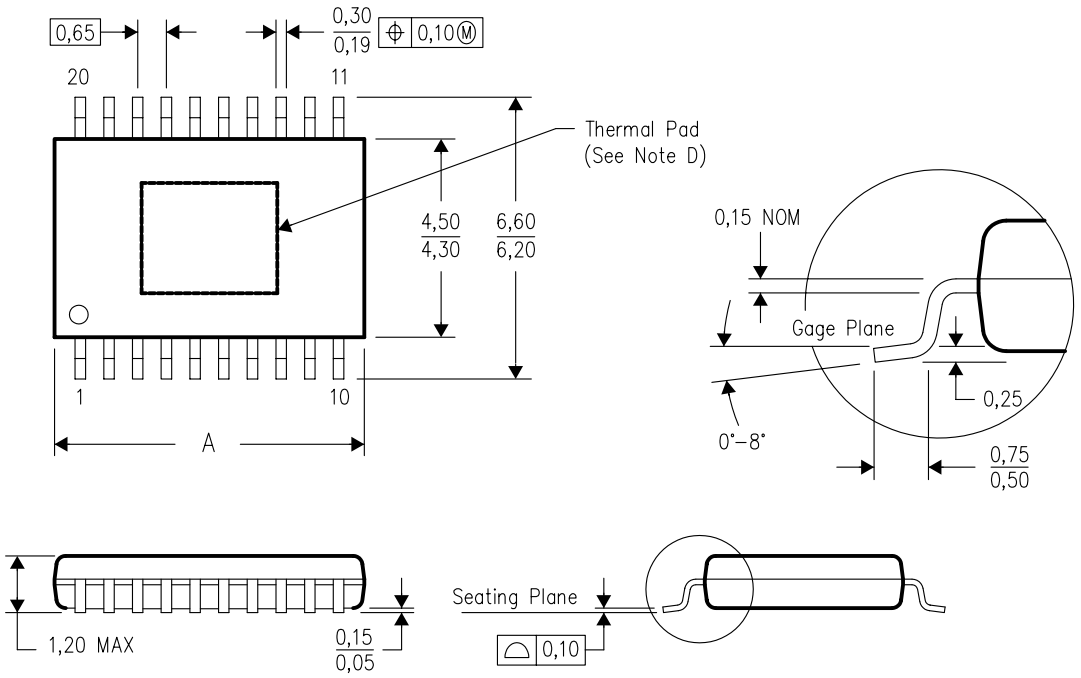
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
BUF08800AIPWPR	PWP	20	TAI	346.0	346.0	33.0



PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

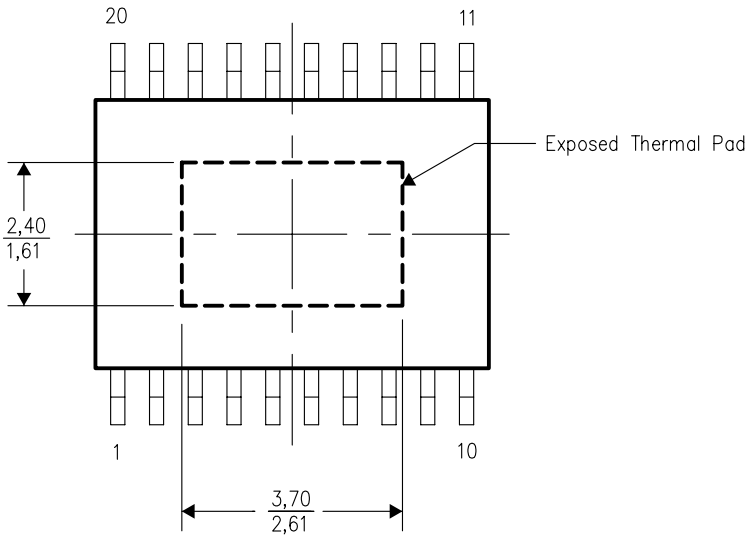
PWP (R–PDSO–G20)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

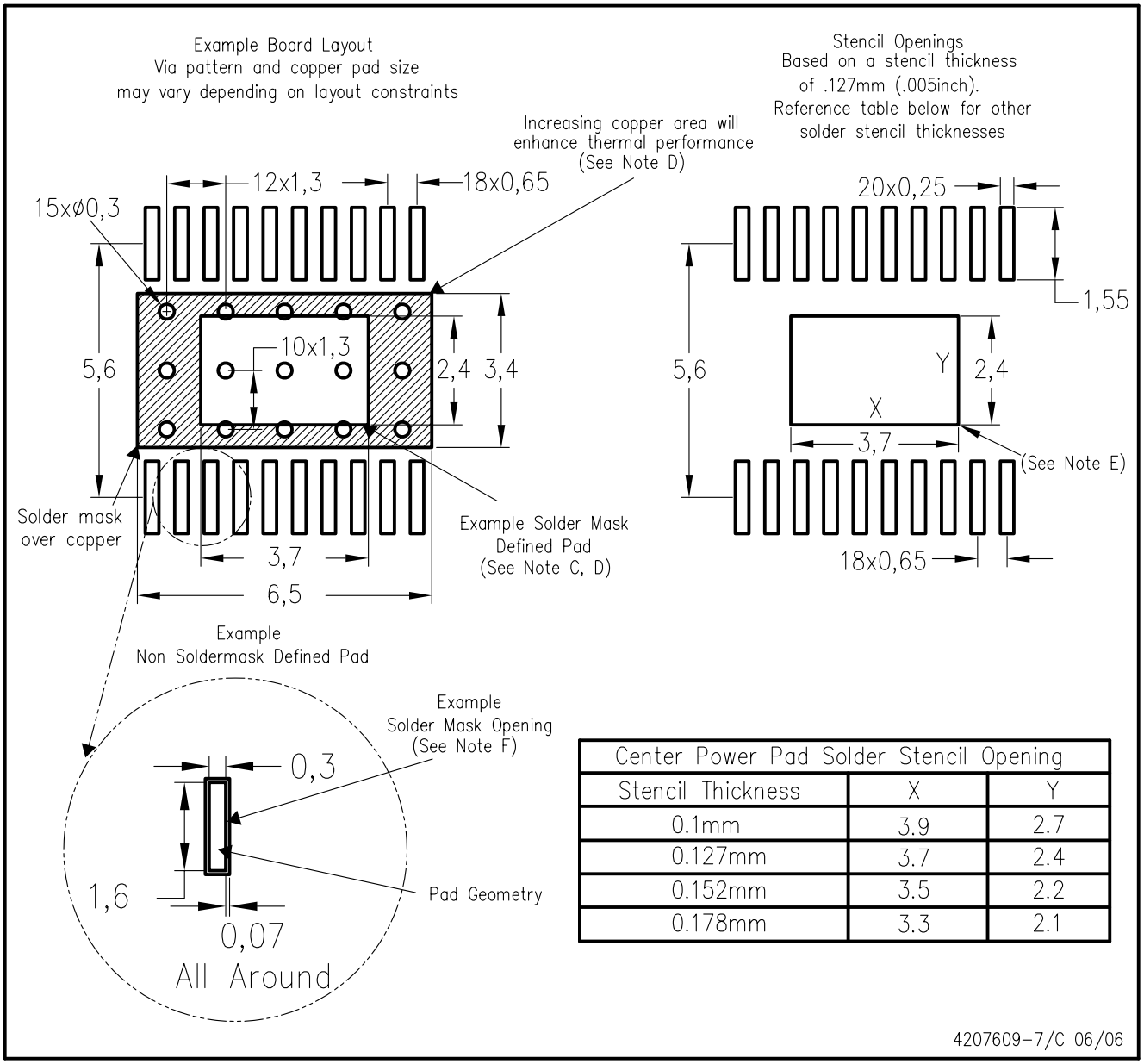


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–7/C 06/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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