SGS-THOMSON MICROELECTRONICS

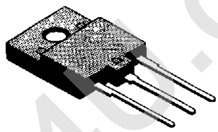
BUH313D

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

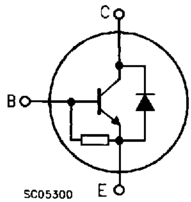
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage ($I_E = 0$)	1300	V
V_{CEO}	Collector-Emitter Voltage ($I_B = 0$)	600	V
V_{EBO}	Emitter-Base Voltage ($I_C = 0$)	10	V
I_C	Collector Current	5	A
I_{CM}	Collector Peak Current ($t_p < 5$ ms)	8	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current ($t_p < 5$ ms)	5	A
P_{tot}	Total Dissipation at $T_c = 25$ °C	50	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

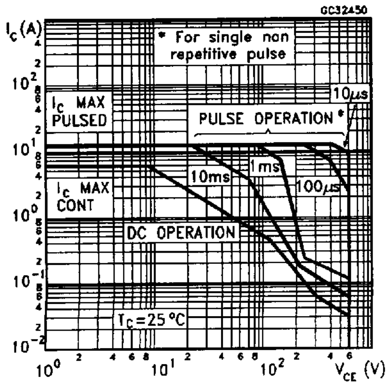
$R_{thj-case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

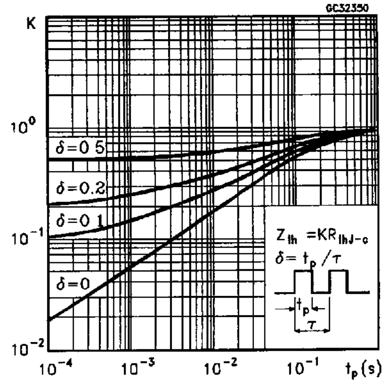
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1300 V V_{CE} = 1300 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			300	mA
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 5 V I_C = 3 A V_{CE} = 5 V T_j = 100 °C	5 3			
 t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 3 A I_{B1} = 1 A I_{B2}= 1.5 A		 1.8 200	 2.7 300	 µs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 15625 Hz I_{B1} = 1 A I_{B2} = 1.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		 2.7 350		 µs ns
V_F	Diode Forward Voltage	I_F = 3 A			2.5	V

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

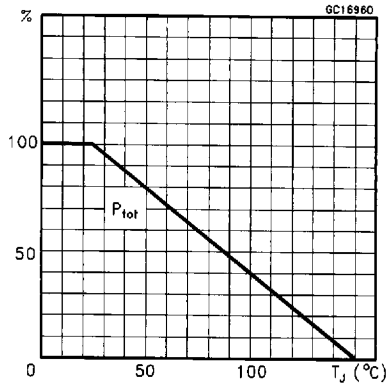
Safe Operating Areas



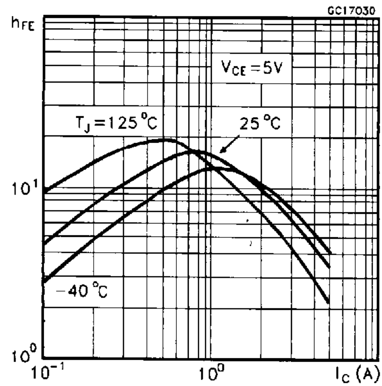
Thermal Impedance



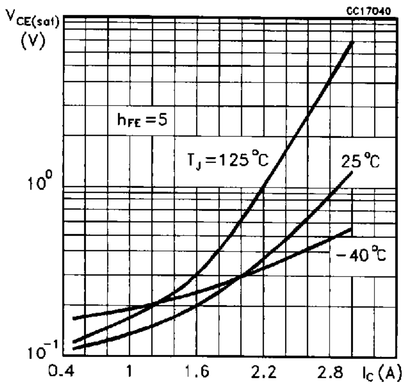
Derating Curves



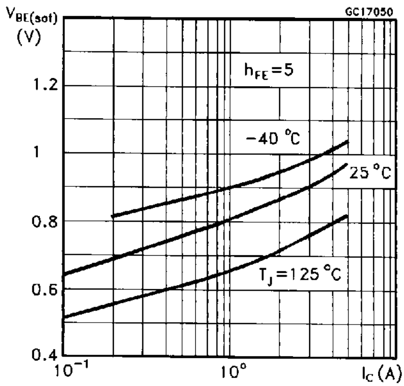
DC Current Gain



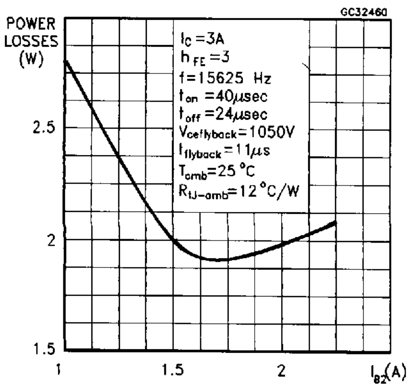
Collector-Emitter Saturation Voltage



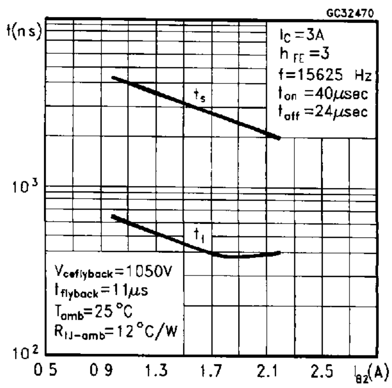
Base-Emitter Saturation Voltage



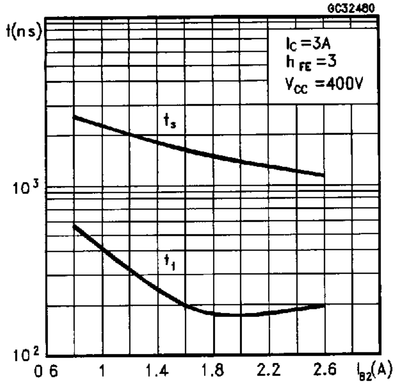
Power Losses at 16 KHz



Switching Time Inductive Load at 16 KHz (see figure 2)



Switching Time Resistive Load



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature Tj, which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at T_j = 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided for the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.

The values of L and C are calculated from the following equations:

$$\frac{1}{2} L\,(I_C)^2 = \frac{1}{2} C\,(V_{CEfly})^2$$

$$\omega = 2\,\pi f = \frac{1}{\sqrt{L\,C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Test Circuits for Dynamic Characterization.

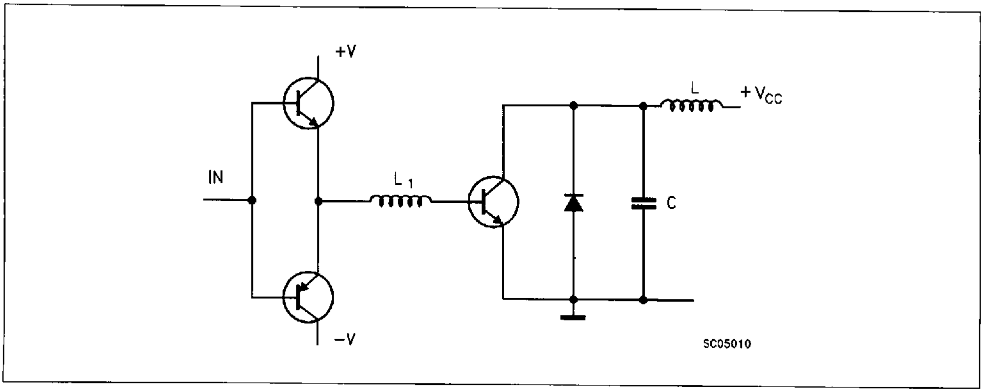


Figure 2: Switching Waveforms in a Deflection Circuit