PowerMOS transistor
Fast recovery diode FET

BUK638-500B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
FREDFET with fast recovery reverse diode, particularly suitable for motor control applications, eg. in full bridge configurations for which faster recovery characteristics simplify design for inductive loads.

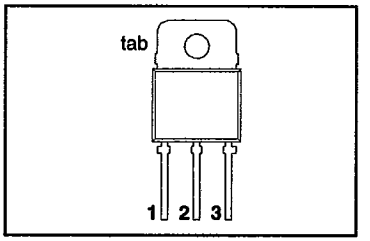
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (DC)	13	A
P_{tot}	Total power dissipation	220	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.6	Ω
t_{rr}	Diode reverse recovery time	250	ns

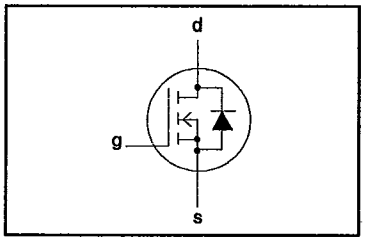
PINNING - SOT93

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	500	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	13	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	8.2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	52	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	220	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.57	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	45	-	K/W

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STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	-	5	50	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 8 A	-	0.5	0.6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 8 A	5.0	10.0	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	2400	2800	pF
C_{oss}	Output capacitance		-	270	420	pF
C_{rss}	Feedback capacitance		-	110	200	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2.8 A;	-	30	60	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	90	130	ns
$t_{d\,off}$	Turn-off delay time	R_{gen} = 50 Ω	-	300	400	ns
t_f	Turn-off fall time		-	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-		-	-	14.6	A
I_{DRM}	Pulsed reverse drain current	-		-	-	58	A
V_{SD}	Diode forward voltage	I_F = 14.6 A ;	V_{GS} = 0 V	-	1.1	1.5	V
t_{rr}	Reverse recovery time	I_F = 14.6 A;	T_j = 25 °C	-	200	250	ns
		-dI_F/dt =	T_j = 125 °C	-	250	350	ns
Q_{rr}	Reverse recovery charge	100 A/µs;	T_j = 25 °C	-	1.3	2.0	µC
		V_{GS} = 0 V;	T_j = 125 °C	-	3.5	5.0	µC
I_{rrm}	Reverse recovery current	V_R = 100 V	T_j = 125 °C	-	15	-	A

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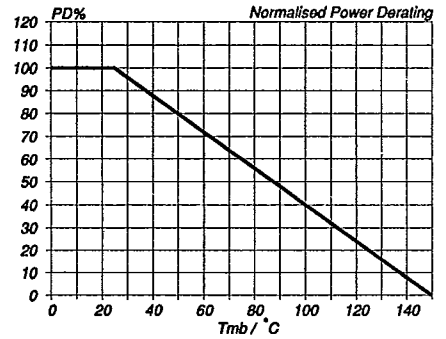

Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

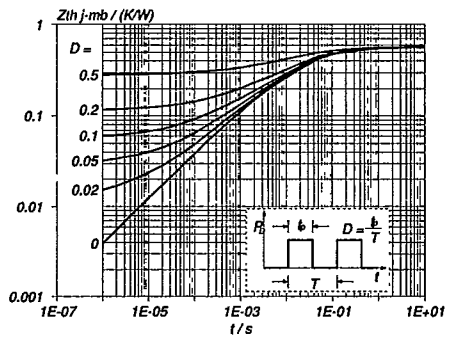

Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

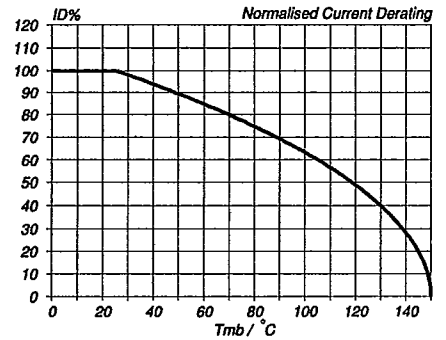

Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

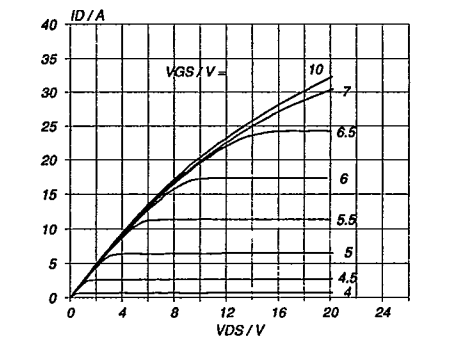

Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

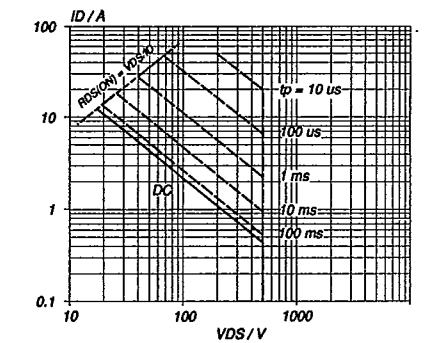

Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

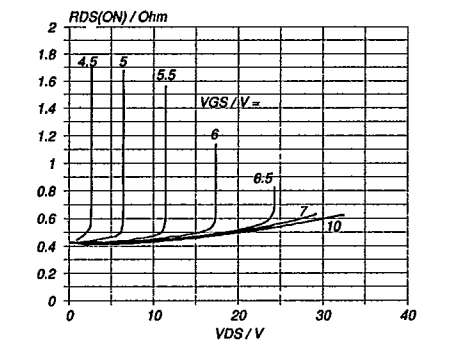

Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

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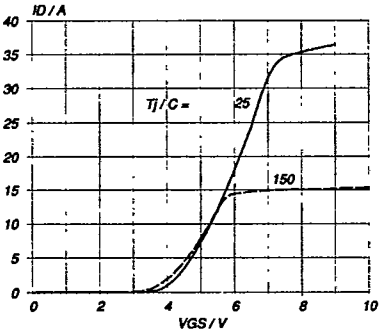

Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

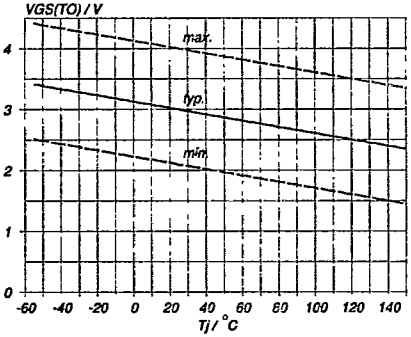

Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

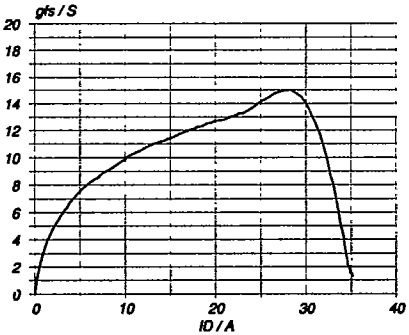

Fig.8. Typical transconductance, $T_j = 25$ °C.
$g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

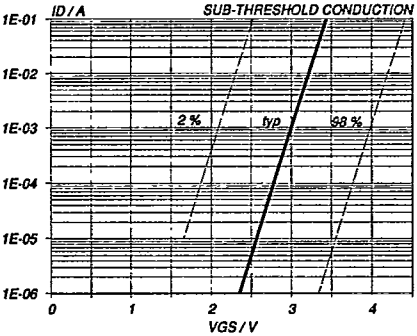

Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

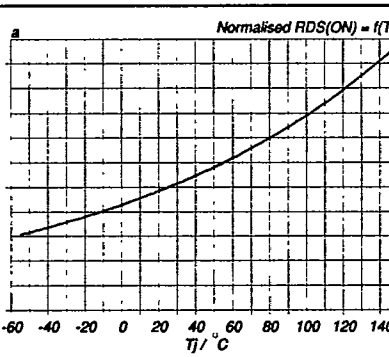

Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D = 8$ A; $V_{GS} = 10$ V

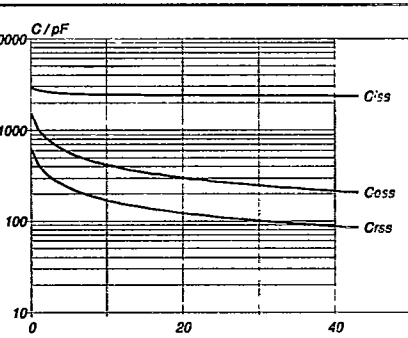

Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

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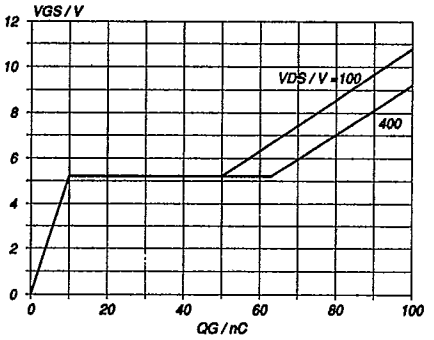

Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: I_D = 14 A; parameter V_{DS}

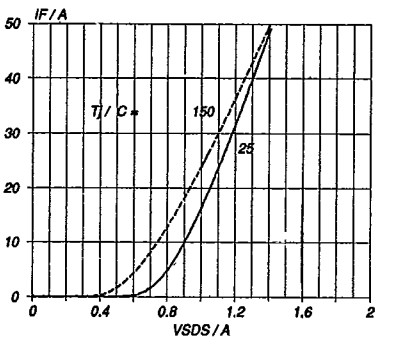

Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j