



# BUK6C3R3-75C

N-channel TrenchMOS intermediate level FET

Rev. 3 — 18 January 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high-performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- High current handling capability, up to 320 A
- Low conduction losses due to very low on-state resistance
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V and 24 V automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoids
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	75	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a>	-	-	181	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	300	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 90\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	-	2.85	3.4	mΩ

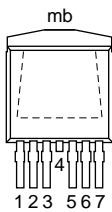
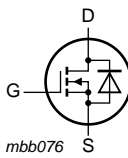


**Table 1. Quick reference data ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 60\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	76	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$ ; $V_{sup} < 75\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^\circ\text{C}$ ; unclamped	-	-	560	mJ

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>SOT427 (D2PAK)</b></p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	S	source		
3	S	source		
4	D	drain <sup>[1]</sup>		
5	S	source		
6	S	source		
7	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to connect to pin 4 of the SOT427 package.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK6C3R3-75C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)	SOT427

## 4. Limiting values

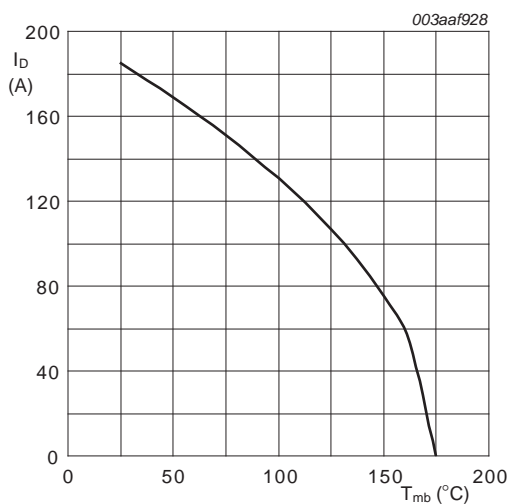
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

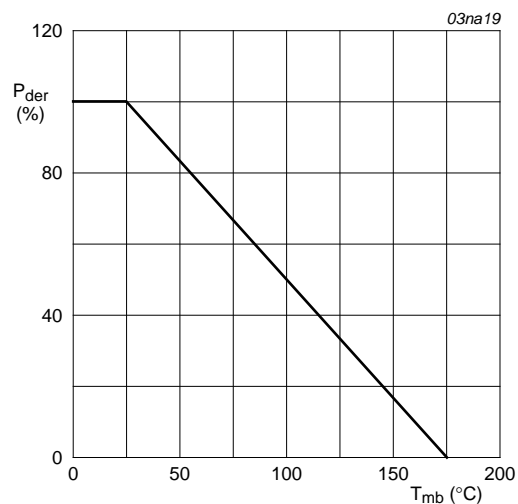
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	75	V
V <sub>GS</sub>	gate-source voltage	Pulsed	[1] -20	20	V
		DC	[2] -16	16	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	-	181	A
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	-	128	A
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; see <a href="#">Figure 3</a>	-	723	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	300	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	181	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	723	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> < 75 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped	-	560	mJ

[1] Accumulated pulse duration not to exceed 5mins.

[2] -16V accumulated duration not to exceed 168 hrs.

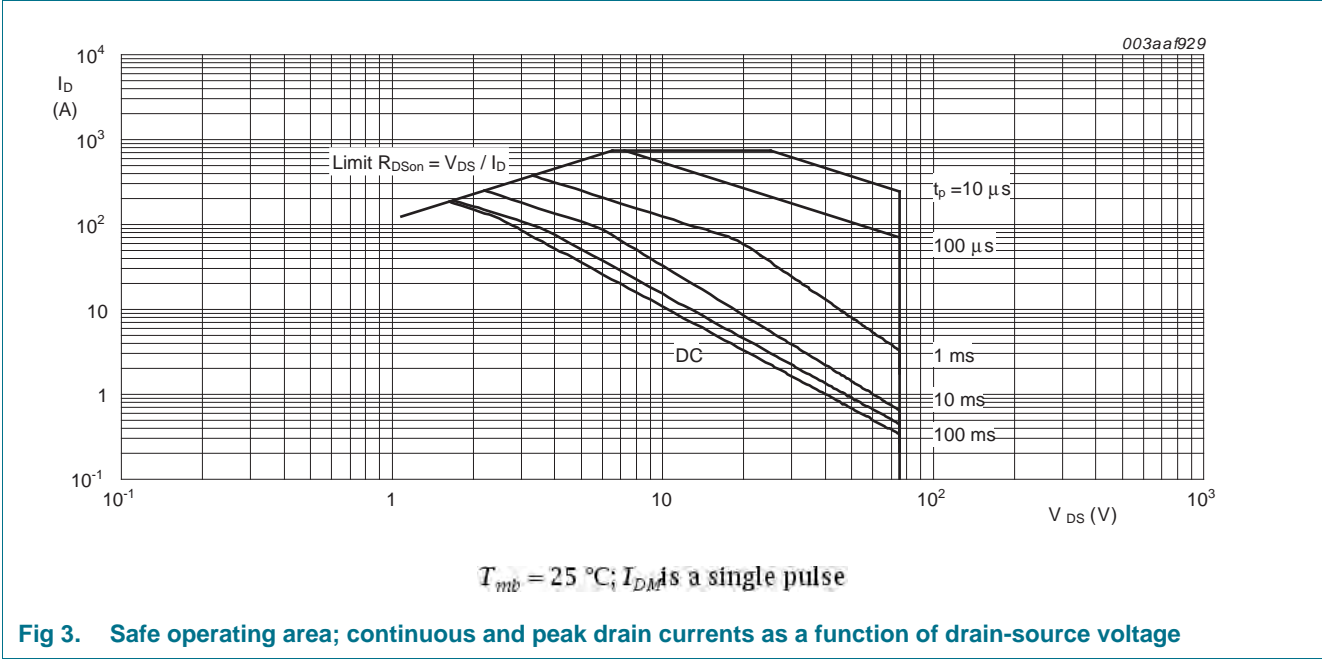


**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

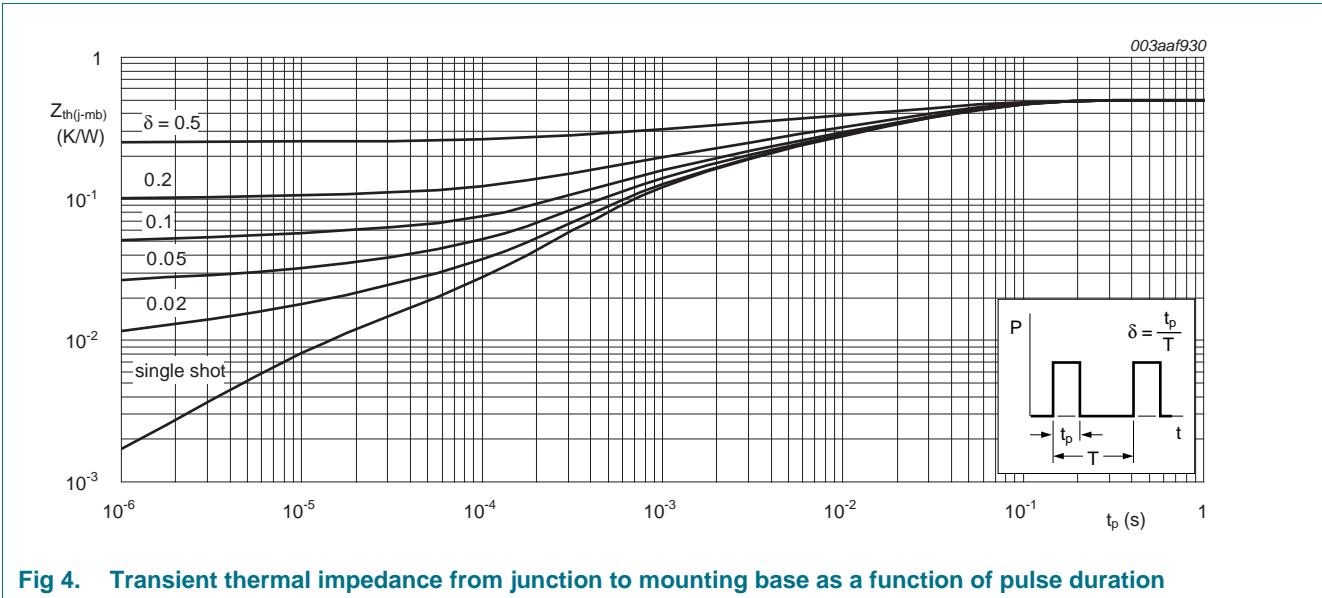
**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



## 5. Thermal characteristics

**Table 5. Thermal characteristics**

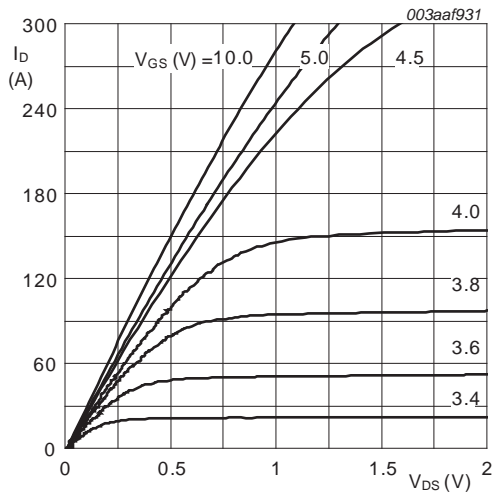
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.5	K/W



## 6. Characteristics

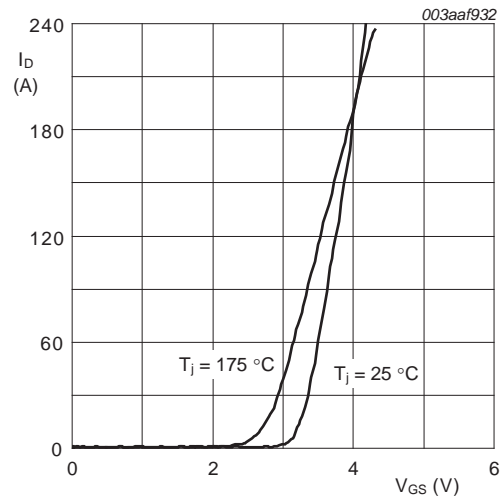
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	75	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	68	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	1.8	2.3	2.8	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 2.5 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	0.8	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	-	-	3.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.04	1	$\mu A$
		$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 90 \text{ A}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	2.85	3.4	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 90 \text{ A}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	3.35	4.3	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 90 \text{ A}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	3.7	5.1	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 90 \text{ A}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-	9.2	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	253	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 5 \text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	140	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	45	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	76	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 15</a>	-	11840	15800	pF
$C_{oss}$	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 15</a>	-	873	1050	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 15</a>	-	546	750	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 0.4 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega$	-	45	-	ns
$t_r$	rise time	$V_{DS} = 40 \text{ V}; R_L = 0.4 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega$	-	217	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 40 \text{ V}; R_L = 0.4 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega$	-	384	-	ns
$t_f$	fall time	$V_{DS} = 40 \text{ V}; R_L = 0.4 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega$	-	165	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 80 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 16</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V}; V_{DS} = 40 \text{ V}$	-	63	-	ns
$Q_r$	recovered charge	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V}; V_{DS} = 40 \text{ V}$	-	165	-	nC



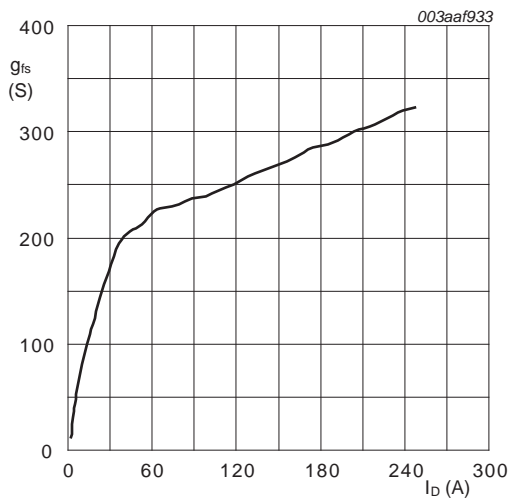
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



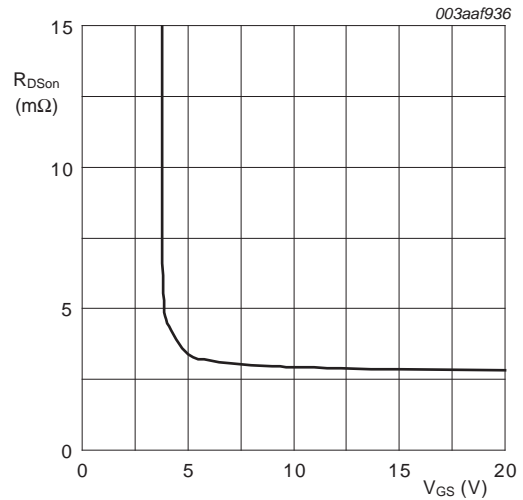
$$V_{DS} > I_D \times R_{DS(on)}$$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



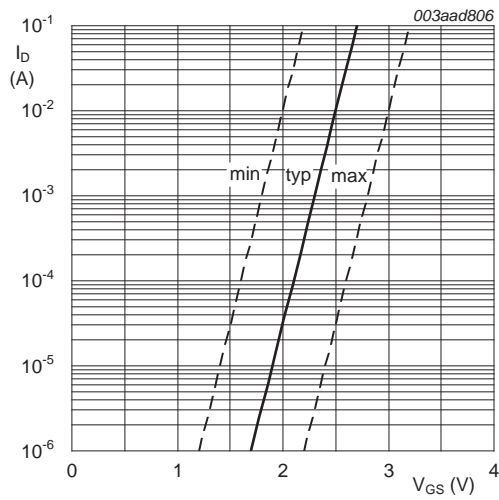
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

**Fig 7. Forward transconductance as a function of drain current; typical values**



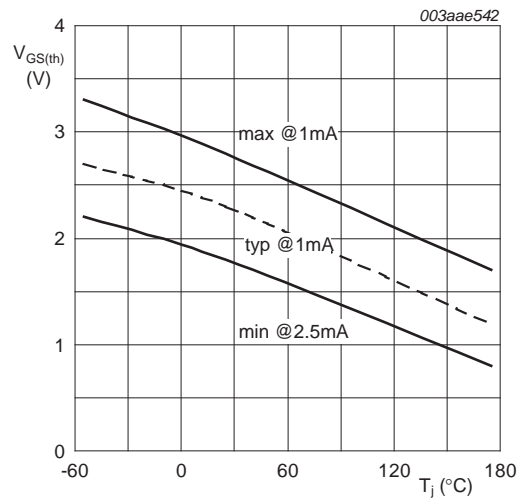
$T_j = 25\text{ }^\circ\text{C}; I_D = 90\text{ A}$

**Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



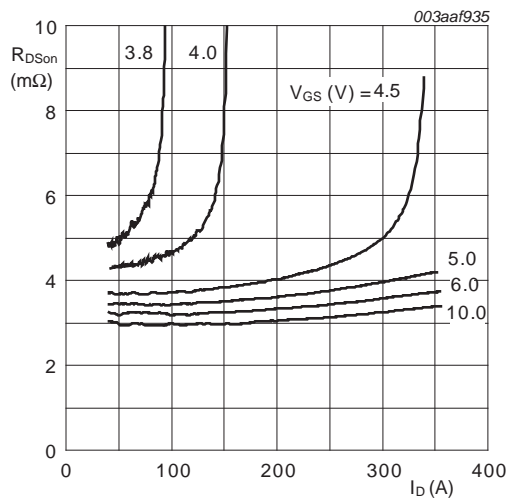
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

**Fig 9. Sub-threshold drain current as a function of gate-source voltage**



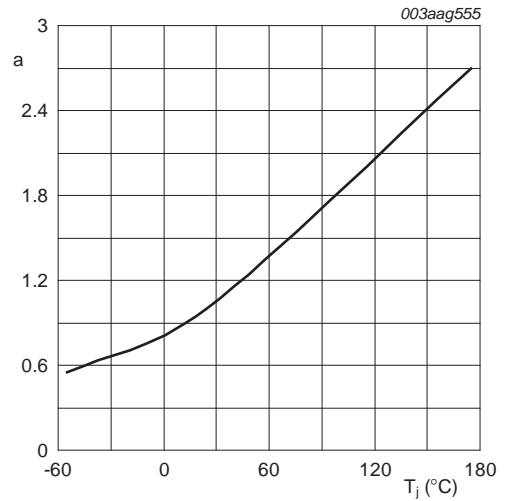
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



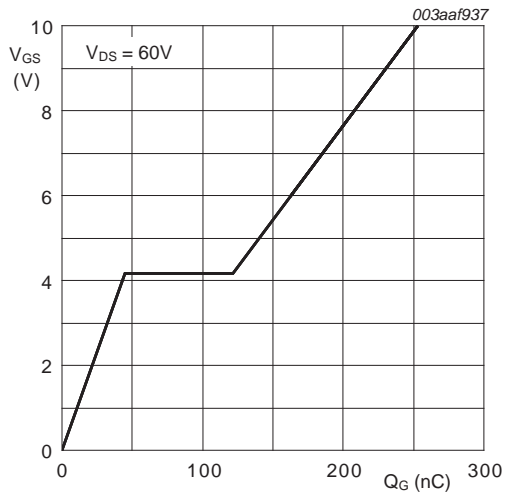
$T_j = 25^\circ\text{C}$

**Fig 11. Drain-source on-state resistance as a function of drain current; typical values**



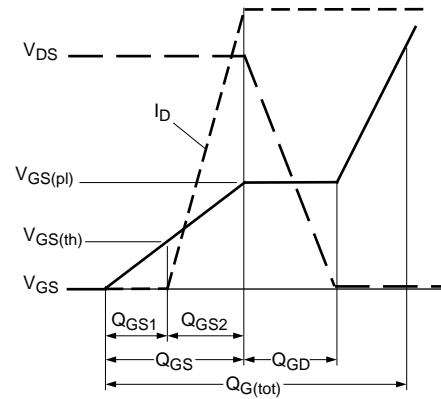
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

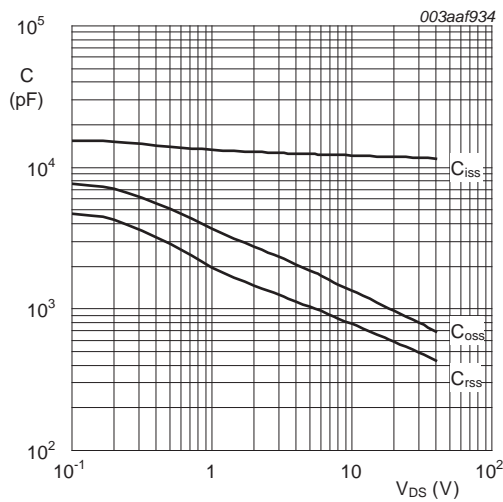


$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values**

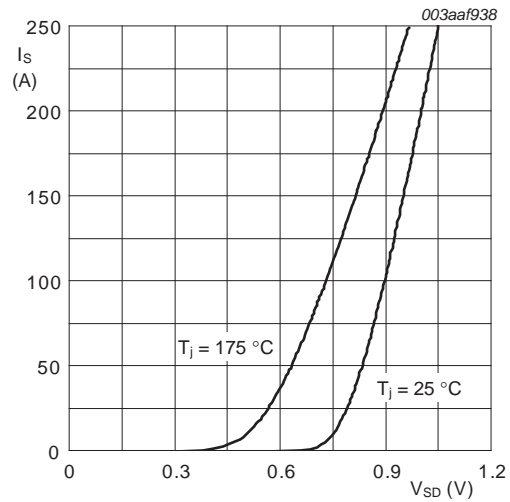


**Fig 14. Gate charge waveform definitions**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{GS} = 0\text{ V}$

**Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)

SOT427

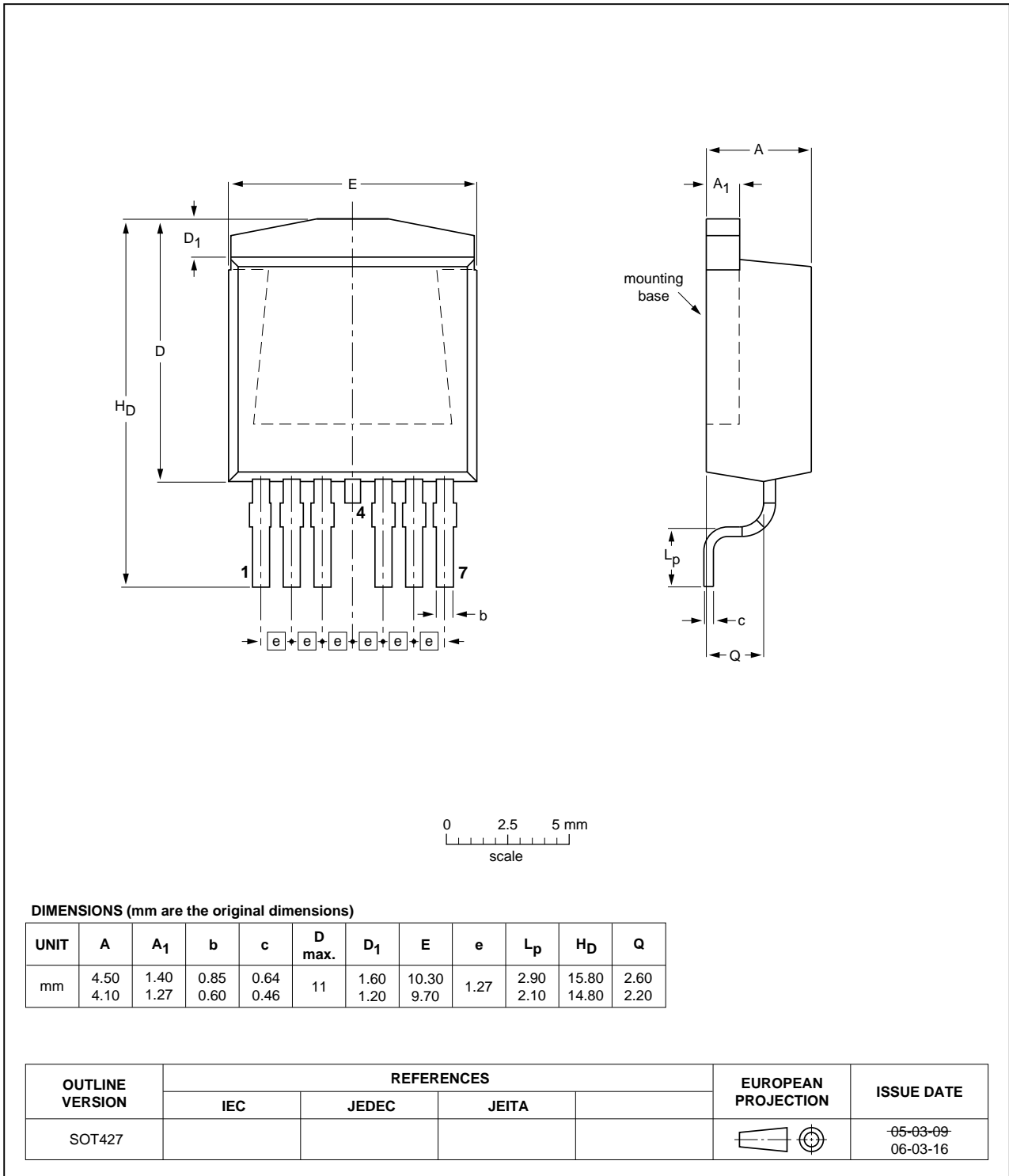


Fig 17. Package outline SOT427 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6C3R3-75C v.3	20120118	Product data sheet	-	BUK6C3R3-75C v.2
Modifications:	• Status changed from preliminary to product.			
BUK6C3R3-75C v.2	20111221	Preliminary data sheet	-	BUK6C3R3-75C v.1

## 9. Legal information

### 9.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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**11. Contents**

**1 Product profile . . . . .1**

1.1 General description . . . . .1

1.2 Features and benefits . . . . .1

1.3 Applications . . . . .1

1.4 Quick reference data . . . . .1

**2 Pinning information . . . . .2**

**3 Ordering information . . . . .2**

**4 Limiting values . . . . .3**

**5 Thermal characteristics . . . . .4**

**6 Characteristics . . . . .5**

**7 Package outline . . . . .9**

**8 Revision history . . . . .10**

**9 Legal information . . . . .11**

9.1 Data sheet status . . . . .11

9.2 Definitions . . . . .11

9.3 Disclaimers . . . . .11

9.4 Trademarks . . . . .12

**10 Contact information . . . . .12**

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